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IBM®

Customer Engineering

Manual of Instruction

Standard Modular System

Component Circuits

This edition, Form 223-6875-1, is a minor revision of the preceding edition but does not obsolete Form 223-6875. Principal changes in this edition are:

Contents

Foreword

Advanced IBM technology has resulted in increased use of solid state circuitry in data processing equipment. This manual contains information about the available Standard Modular System component circuit cards, the way they are packaged, and the logic block representation used for each. The component circuit cards are described in such a way that this manual may aid in learning the circuitry of any equipment using these standard component cards.

The manual assumes that the reader has a basic background in transistor fundamentals and electronic circuits. Information is presented from the standpoint of the circuit understanding required for servicing, and not from the standpoint of circuit design. When design information is considered necessary, it is included. All the material included was prepared from information relative to production at a given level. Engineering changes may alter exact timings, voltages, logic blocks or component values; therefore the customer engineer is advised not to use this information alone as a reference manual or service aid.

The text is divided into five general sections all relating to the component circuit cards.

The first section (page 5) contains a brief introduction to the manual, its organization and purpose.

The second section (pages 6-11) contains information on the Standard Modular System of packaging used in new data processing equipment. Description, nomenclature and location numbering are detailed for both the Module I and Module II type of building block packaging and the standard component circuit cards.

The third section (pages 12-16) contains information about the Automated Logic Diagrams used in designing and servicing of the data processing equipment.

The fourth and major section (pages 17-179) contains the SMS card descriptions, arranged alphabetically by card code and cap connection.

Finally, the Appendix (pages 180-187) contains cross-reference charts according to part number and function for all SMS cards in the fourth section, and a list of logic symbols used in the automated logic pages.

Pages 189-233 include SMS service information and additional card descriptions.

Standard Modular System Component Circuits

Advanced IBM technology has developed several programs to standardize and expedite the design and manufacturing of new data processing equipment. Notable among these are component circuit cards using solid state circuitry, automation of design, and the standard modular system (SMS) of packaging. This manual deals mainly with the component circuit cards but also includes sections on automation of design and the standard module system of packaging.

Organization and Purpose

This manual describes in text and chart form all SMS component cards now available for use in IBM equipment. Its purpose is to give the customer engineer sufficient understanding of circuits to service the IBM 7000 systems and all other IBM equipment that uses the cards. The description of each card also relates the circuit to its automated logic block configuration.

The component circuit descriptions are arranged alphabetically by card code and cap connection. This dictionary arrangement permits quick reference to the general information for any pluggable circuit cards now available. In addition, the Appendix gives several cross reference charts that make it possible to locate card descriptions by part number or function.

SMS Card Description Format

At the top of each SMS card description is the logic block (or blocks) used to represent the circuit in the automated logic diagrams. In most cases one block configuration is shown for each circuit on a card; however, one circuit could be used in several ways and would then be represented by more than one logic block. To assist in circuit understanding, typical logic applications are also included near the top of the schematic. Dashed lines around the input or output loading blocks distinguish these blocks from the logic block being described. In like manner, additional circuitry is also illustrated in dashed lines.

Logic flow through the blocks and the circuit is always from left to right across the page. The circuits are drawn so that the most positive voltages are at the top of the schematic and most negative voltages are at the bottom of the drawing. Electron flow is then from the bottom to the top of the schematic for both PNP and NPN transistor circuits. In fact in this manual all references to the flow of current are from minus to plus. The shading of a transistor symbol indicates that the transistor is in a conducting status.

Waveforms are included to aid in circuit explanations. Pulses are usually shown as square waves, even though a perfect square wave does not exist. The actual rise and fall times are a function of the transistors used and the loading conditions. Waveforms are shown on the logic block as well as on the circuit diagram, and show the phase relationship between the input and output signals. Nominal (nom) voltage levels are shown for most circuits.

At the bottom of the schematic is found additional information pertaining to the circuit. It may include:

1. Card code, cap connection and the part number of the SMS card.
2. Minimum and maximum voltage swings for the input and output signals.
3. Delay timings, or rise and fall times of the signals.
4. Functional symbols used in line 1 of the ALD block to indicate that the card is capable of performing several logical functions. For example, both positive and negative logic are used in solid-state switching circuits. That is, a +AND circuit may also be used to perform a −OR function and a +OR circuit can also perform a −AND function. Several circuits can share a common load and provide a second level of logic in the output circuit. These DOT OR or DOT AND functions are also indicated by the symbol on line 1. Finally, cards are connected together to form triggers (or latch circuits) and are so indicated by appropriate functional symbols.
5. Types of outputs and loading conditions. Whenever possible, the SMS cards using the same basic card, but having different loading conditions, are grouped and treated as a family of cards. For example, in the CG- - family, four cards are listed with different cap connections. Circuit operation for each card is similar, but internal collector loading of the circuits on the card is determined by the particular cap connection.

Below the diagram is the card title followed by a brief description of:

1. The purpose or use of the circuit
2. Circuit operation
3. Particular or special applications

Indexing Arrangement

The SMS card descriptions are arranged in alphabetical order according to the card code and cap connections assigned each card. This alphabetical code is found in the upper right corner of the SMS card description page. Cross reference charts are provided for quickly locating or identifying a card as to part number, usage, or card code and cap connection.

Modes of Operation

Card descriptions that follow pertain to the following modes of operation: current mode transistor circuits, diffused junction transistor circuits, complemented transistor diode logic (CTDL) circuits, magnetic core logic circuits, or special purpose circuits.

Current Mode Transistor Circuits

Current mode transistor logic is characterized by the use of small-signal swings that switch well-defined currents from one part of a circuit to another. The collectors of the transistors used in these circuits are reverse-biased by approximately 6 volts to avoid saturation operation, and

the inherent delay due to carrier storage. Operational speeds of one megacycle are possible with this mode of operation by using alloy junction transistors. All logic must be performed by the transistors because the voltage swings are insufficient to operate additional resistor or diode logic. Current mode circuits are especially useful for line-drive functions, sensing and control circuits.

Line Terminology and Voltage Swings. Voltage swings of at least ±0.4 volts about ground are referred to as N lines and are used to drive N-type transistor bases. Voltage swings of at least ±0.4 volts, about −6 volts, are called P lines and are used to drive P-type transistor bases. The −6v and ground potentials are the transistor reference voltages used for NPN and PNP transistor blocks, respectively.

Outputs. Two outputs are usually available from the current mode logic circuits, an in-phase output and an inverter or out-of-phase output. When used in a system, the P line output of a PNP circuit drives a NPN circuit. The N line output of an NPN circuit always drives a PNP circuit. Convert blocks are used to drive a PNP load with a PNP output or an NPN load with an NPN output. Outputs not used must be terminated to the proper output reference voltage.

Delays. The delays for these circuits are a combination of both the transistor delays and transition times within the circuit. Delays are defined as the elapsed time from the time the input signal has reached the switching threshold of the circuit being driven to the time the output signal of the driven stage has reached the switching threshold of the following stage. Nominal delay values for most logic blocks are about 0.06 microseconds.

Diffused Junction Transistor Circuits

Use of the diffused junction transistors in current switching circuits permits this group of component cards to function at increased speeds above 7.0 megacycles. Circuit operation, line terminology, voltage swings, outputs and delay considerations are similar to those of alloy junction current switching circuits. The delay encountered per stage in these circuits, however, is approximately 0.02 microseconds, and is measured from the 10% input value to the 10% value of the output signal.

Complemented Transistor Diode Logic (CTDL)

Complemented transistor diode logic (CTDL) provides a complete system of solid-state logic for use in intermediate speed systems (near 250 kc). This system of circuitry uses a large number of diodes and large signal swings to control saturating alloy-junction type transistors. Component cards in this group are capable of performing all the necessary logic economically and with a high degree of reliability. This mode of operation uses circuitry designed around existing voltages and is compatible with the standard voltage mode or current mode of operation. Use of the large signal swings (−12 volts) compensates for the diode drops and allows a greater cascading factor. CTDL circuits are also less sensitive to noise than other circuit modes.

Line Terminology and Voltage Swings. Reference voltages used in CTDL circuits are −6 volts and ground. A signal that swings ±6 volts (maximum) about ground is referred to as a T line and is used to drive N-type transistor bases. Signal swings ±6 volts (maximum) about −6 volts are referred to as U lines and drive P-type transistor bases. In order to make sure that the diodes are reverse biased when the transistor is on, the input and output voltage references differ by 6 volts.

Outputs. An inverted output is available from the basic logic blocks. The output from a PNP block is a U line and drives a NPN transistor. The output from a NPN block is a T line and drives a PNP. Convert blocks are used when a PNP block has to be driven by a PNP block or a NPN block by a NPN block. Suitable current mode outputs are also available from some CTDL circuit cards. Because loading conditions greatly affect the output voltage swings of the transistor, minimum and maximum voltage levels are indicated on the diagram for CTDL circuits. Voltage levels used with CTDL card descriptions are usually shown as ±6 volts about a 0 or −6 voltage reference.

Power Supply Voltage. This mode of operation requires five standard voltages, +6, −6, −12, +6M and −12M. The +6M and −12M voltages are used in marginal checking of the circuits.

Delays. The delay of the signal in the basic CTDL logic block is a function of the transistor delays plus the loading effects of the input and output circuits. Delays for several stages in cascade are numerically equal to the sum of individual stages. Unless otherwise stated in the card description, delays are measured from the time the input signal crosses its reference voltage to the time the output signal crosses its reference voltage. Nominal values for basic logic stages are approximately 0.2 microseconds.

Magnetic Core Logic Circuits

Cards in this group contain magnetic core positions and associated circuitry. Line terminology, function and output information are dependent on the use of the particular card. These cards are used in shift registers, and in input-output buffer applications.

Special Purpose Cards

Special purpose cards such as coupling circuits, bias and load resistors, integrator circuits and converting networks, are found in this group. These cards are normally identified with a specific application. E.g., the QS- - load card is used with the drum driver (GS- -) card.

Standard Modular System Packaging

The Standard Modular System (SMS) provides a moderate number of standard building blocks to facilitate the manufacturing of solid-state data processing equipment. Two modular type units and pluggable printed circuit cards are available to provide for flexible packaging of all electronic components required in a system. Some of the more important advantages offered by the use of SMS packaging are:

1. Standardization of circuits and packaging methods, that reduce parts stockage in the field and parts handling in the manufacturing process.
2. Increased serviceability by allowing rapid access to cards and test points and elimination of the cover removal and storage problem.
3. Use of latest production techniques such as Wire-Wrap* and automated production lines.
4. Data processing equipment that requires a reduced amount of space, power and air conditioning.

*Trademark of Gardner-Denver Company.

Figure 1. Stacked Module I Packaging

Module I (Vertical Swinging Gate and Frame Assembly)

The Module I, Vertical Swinging Gate and Frame Assembly, is one type of modular SMS packaging designed for use in smaller data processing systems. The basic module is 29″ wide, 30-5/8″ deep and 31″ high with casters. This basic module may be used independently, or stacked as shown in Figure 1. The latter arrangement is considered to be standard when using more than two modules.

The Module I SMS package houses all the pluggable cards, relays, power supplies, and cables associated with a system. Provision can also be made to mount control panels and indicator panels within the module. Access for servicing is usually from the front and the rear of the module, although power supplies and indicator panels will often be serviced from the sides.

Nomenclature and Physical Description

The stacked Module I units as shown in Figure 2 are called frames. The frames consist of an upper Module, A, and a lower Module, B. Each module contains eight gates, numbered as shown in the figures. Gates 1 to 4 open to the front of the module and gates 5 to 8 open to the rear of the module. The gates in Module B swing up to open while those of Module A swing down to open.

Each gate can accommodate 156 SMS receptacles arranged in six columns and 26 rows (gate open). Normally, the SMS receptacle positions in rows 1 and 2 (lower gate) and 26 and 25 (upper gate) are reserved for cable connectors.

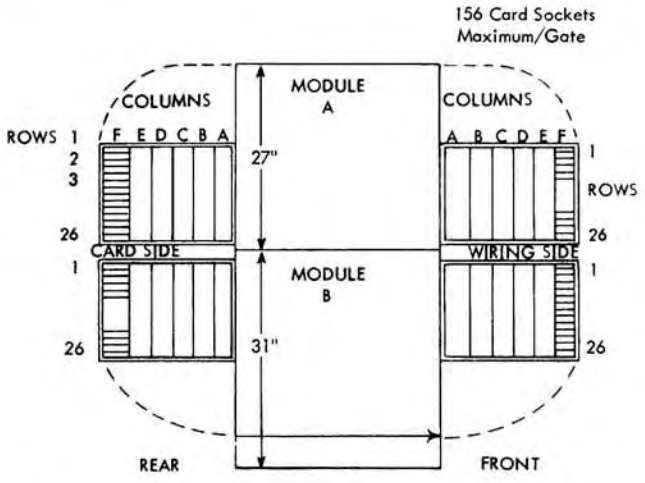


Figure 2. Stacked Module I Nomenclature

Location and Numbering Designation

To properly locate pins, cards or components in a system using the stacked Module I type of packaging, the following identification system is assigned.

	IDENTIFICATION ASSIGNED	EXAMPLE
Machine type	3 or 4 digit numbers	7000
Frame	01-99	02
Module	A (Upper Module) B (Lower Module)	A
Gate	1 through 8	3
Column	A to F	C
Row	1 to 26	20
Pin	A to R (I and O omitted)	E

Module II (Horizontal Sliding Gate and Frame Assembly)

The Module II is another type of SMS packaging normally used in larger data processing systems (Figure 3). This SMS module is 29-1/2" wide, 56" deep and 68-5/8" high (with casters). Each frame consists of four horizontal sliding gates, and two tail gates that house all the pluggable circuit cards, hardware and cabling associated with a system. Space is provided on the back of the sliding gates to mount the power supply components. Access to the power supply is from the front, by opening the gates beyond their 45° limit. To minimize space requirements, the frames are designed so that they may be placed side by side. Access for servicing is from the front or the rear of the frame.

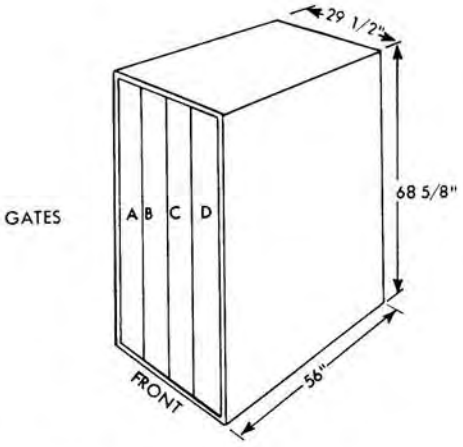


Figure 3. Module II Packaging

Nomenclature and Physical Description

Figure 4 shows the physical locations on the sliding gates.

SLIDING GATES

Within the Module II frame are four gates (A, B, C and D) attached to slides that allow a pair of gates to pull out horizontally and open like the covers of a book. A total of 16 chassis are mounted on the gates, four chassis on each gate. The chassis are numbered 1 through 4 as shown. A chassis consists of ten rows and 28 columns of SMS receptacles that accept the pluggable SMS circuit cards and cable connector cards. The rows are labeled A through K (I omitted) from the top to the bottom of a chassis, and the columns are numbered outward (1 through 28) from the hinge side of the gate. All receptacle positions accept pluggable circuit cards with the exception of the following SMS positions that are reserved for special cable cards used to interconnect chassis and gates (Figure 5).

1. Row A (chassis 1 and 2)
2. Row K (chassis 3 and 4)
3. Columns 1, 2 and 28 (chassis 1 and 3)
4. Column 1 (chassis 2 and 4)

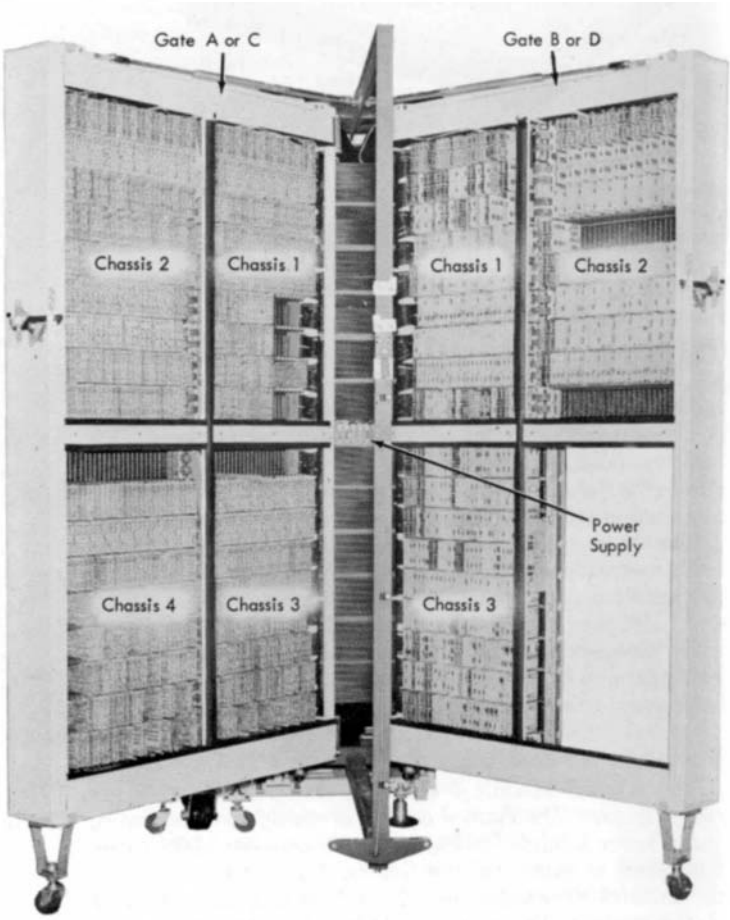


Figure 4. Module II Horizontal Sliding Gate

The coaxial cable or twisted-pair wire assignment to the cable connector sockets is also shown in Figure 5. Two rows of terminal blocks, labeled "T," are used as edge connectors between the upper and lower chassis. Other components, such as relays, special core arrays or indicators, can be mounted in place of the SMS sockets on the chassis, if required.

Tail Gates

The tail gate assembly consists of two T-shaped gates, gate E (top) and gate F (bottom). These gates are used for interconnecting the input-output cables to the various sliding gates. Access to the tailgates is from the rear of the frame. Both gates swing down for servicing.

Each gate has both SMS sockets and special cable sockets, arranged in nine columns labeled A through J (Figure 6). In the top of gate E and the bottom of gate F are located 16 SMS sockets, in each column except column E. These sockets are used for special slide connectors that provide cable connections to the gates. In the bottom part of gate E and the top of gate F are positions for 50 cable connectors used for interconnection between frames. These cable connectors are either the 40- or 20-position type.

For numbering purposes the tail gate is considered a rectangular block nine SMS sockets wide and 56 sockets deep. Rows are numbered 1 through 56 from the hinge up. Because the cable connectors are equivalent to four SMS sockets in width, the numbering on gate E is 1, 5, 9, and so on, and on gate F is 17, 21, 25 and so on.

Location and Numbering Designation

To properly locate pins, cards, or components in a system using Module II type packaging, the following identification system is assigned.

	IDENTIFICATION ASSIGNED	EXAMPLE
Machine type	3 or 4 digit number	7070
Frame	01 to 99	03
Gate	A through D	A
Chassis	1 through 4	2
Column	1 through 28	20
Row	A through K (omitting I)	J
Pin	A through R (omitting I and O)	D

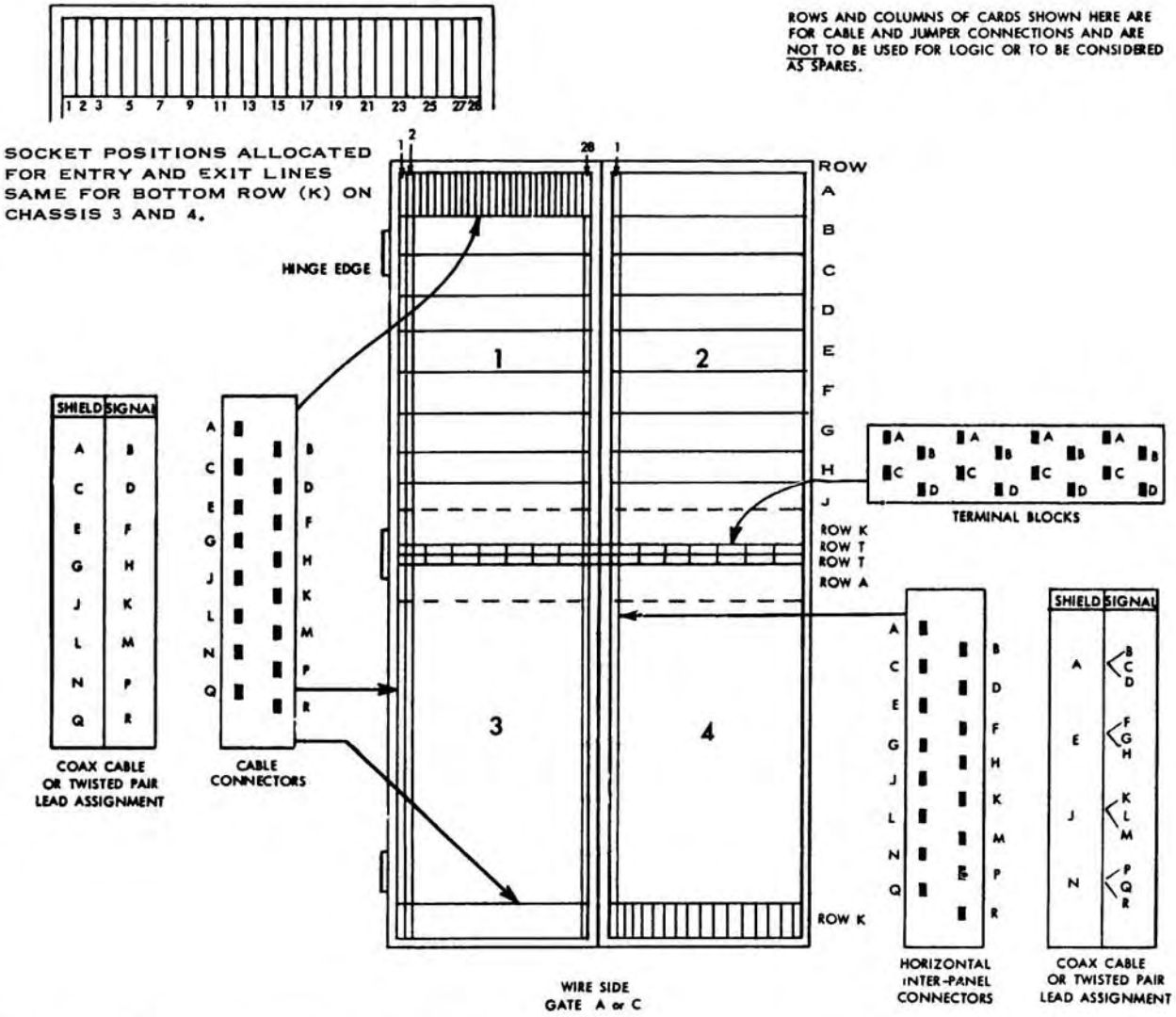


Figure 5. Card Gate Layout (Showing Special Cable Connector)

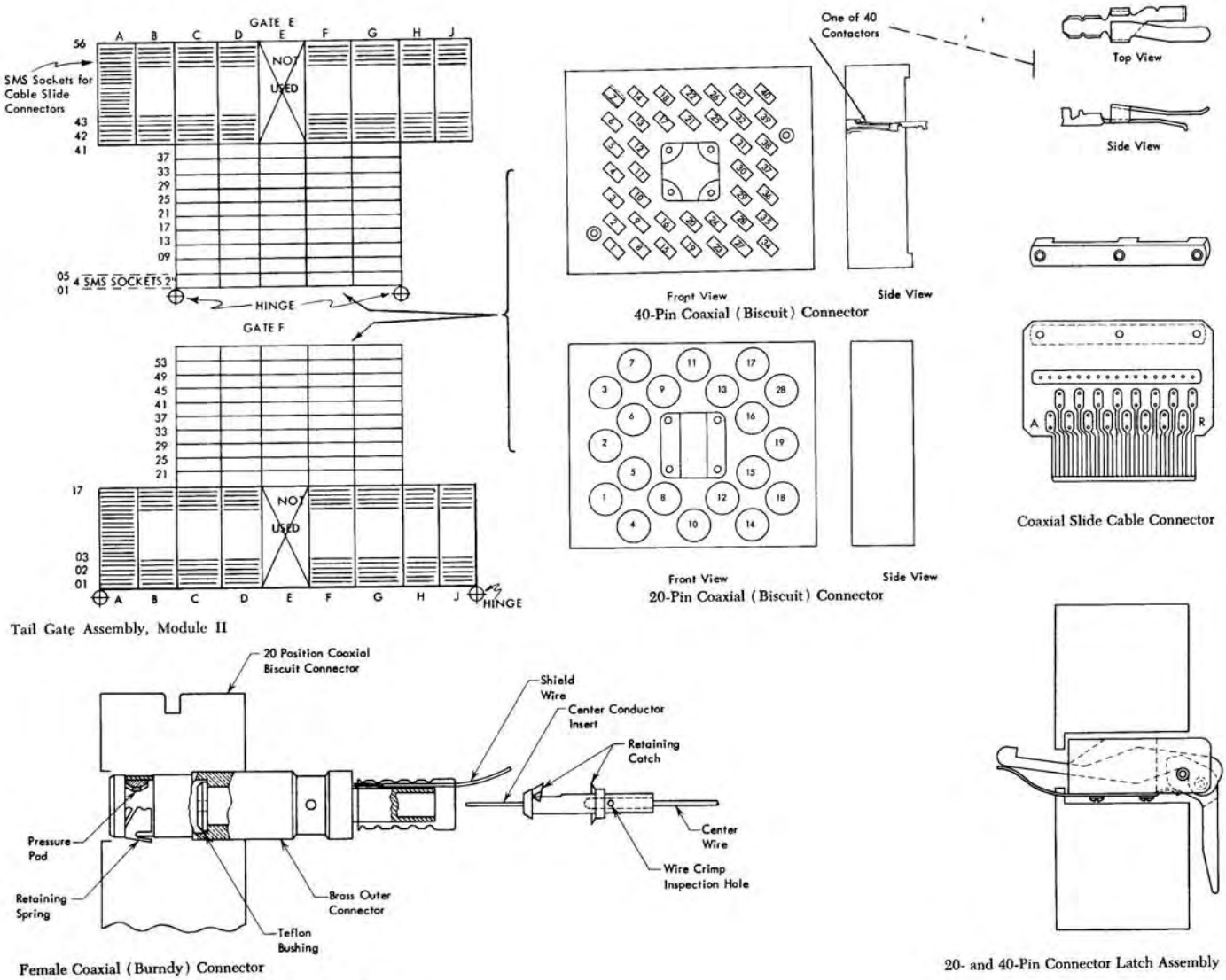


Figure 6. Tail Gate Assembly, Module II

SMS Printed Wiring Cards

Standard printed wiring cards are used in the Module I and Module II types of packaging. These SMS printed wiring cards facilitate the manufacturing process and permit standardization of circuits. The pluggable printed circuit cards contain all the components and printed wiring necessary for a particular electronic function or functions. A special program cap on some SMS printed circuit cards gives additional flexibility to this form of packaging, and reduces the number of component cards required for field servicing. Other printed wiring cards are used as cable connectors and back panel voltage distribution buses.

Description

The SMS circuit card (Figure 7) is made of an epoxy paper laminate material which is 0.056 inches thick, 4-1/2 inches long and 2-1/2 inches wide. All of the electronic components and the program cap, if used, are mounted on the front side of the standard SMS card form. Connections to the components and program cap are made on the back side of the SMS card form by printed wiring patterns which terminate at 16 possible contacts at the bottom of the card. These contacts, labeled A through R as shown, couple the signal and standard service voltages to the circuit components when the card is inserted in the SMS socket. The printed circuit wiring or land pattern is dependent on the circuit configuration of the card.

Program Cap

The program cap located on the front of some of the SMS cards consists of two conductor rails which, in the pre-cut state, connect to 15 tabs on the printed circuit land pattern. By cutting the program cap, various jumpering connections are made to the tabs to allow one SMS card having a definite land pattern to be used in several different circuit configurations. The jumpering of these connections on the program cap are referred to as "cap connections."

Card Identification

A four-letter code is assigned each card to identify the large number of SMS cards required for packaging all the electrical circuits required in data processing equipment. The first two letters designate a card code that is assigned

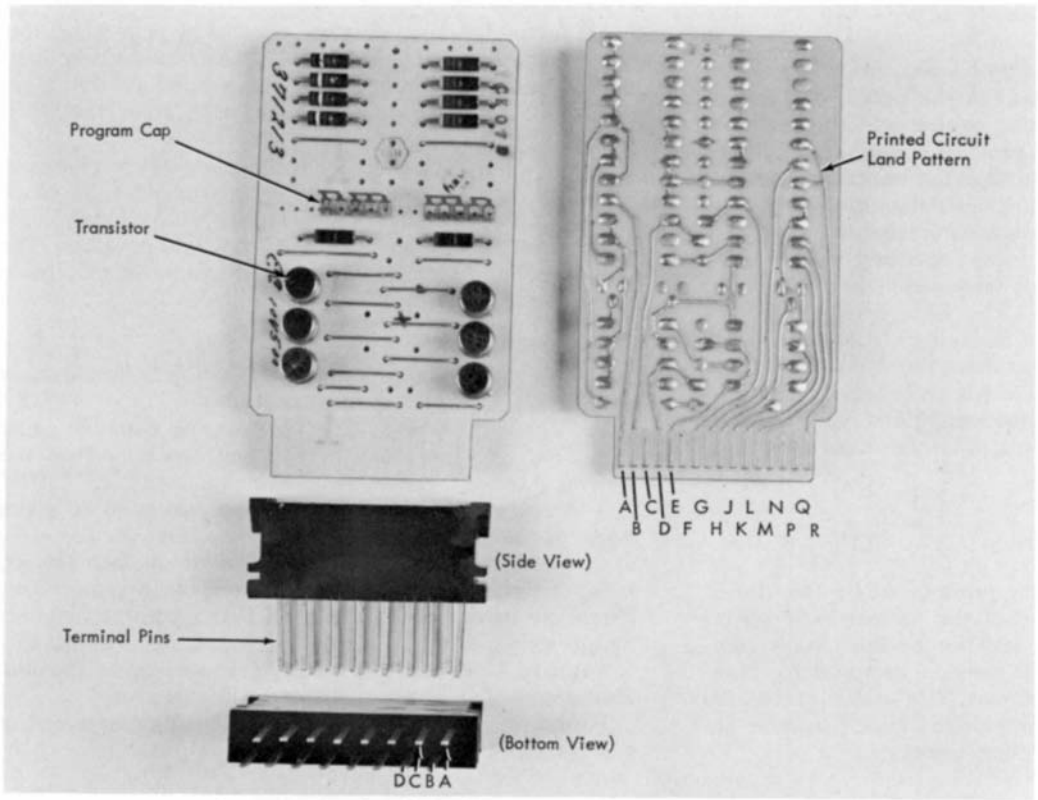


Figure 7. SMS Printed Circuit Card and Socket

from AA to ZZ, in alphabetical order. The last two digits refer to a specific cap connection made on the SMS cards that have program caps. The cap connection code is assigned from ZZ to AA in this order. If all cap connections are cut, or if a card does not have a program cap, — — will be used in place of the code letters for cap connection (e.g., AK- -). Both a card code and a cap connection code are required to identify a card properly. On the component side of each card is stamped the assembly part number.

SMS Card Receptacles

The pluggable printed circuit cards are inserted into SMS receptacles as shown in Figure 7. Although the contacts are all in line on the card insertion side of the SMS receptacle, they pass through the receptacle in a staggered arrangement as noted in the figure. This staggering allows additional room for Wire-Wrap or soldering of signal and voltage wires to the terminal pins. Figure 8 shows an 8-position socket also used in the SMS packages.

Special Printed Wiring Cards

Modified pluggable SMS cards are used as inter-chassis cable connectors. These connectors are inserted into the SMS receptacles and facilitate the manufacturing and servicing process. Back-panel printed circuit cards are also used to distribute the standard supply voltages to groups or rows of cards.

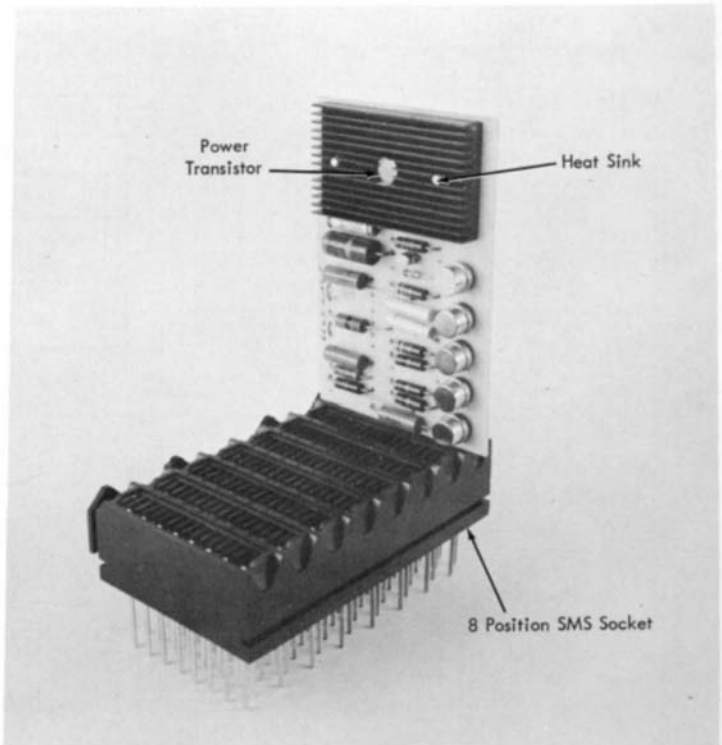


Figure 8. SMS Card and Eight-Position Socket

Automated Logic Diagrams (ALD)

Automation of design was initiated because of the large volume of paper work required in the design and manufacturing of new data processing equipment. This program uses an IBM 704 or 705 to provide a fast and accurate method of preparing and up-dating the information necessary for customer engineering, manufacturing, and engineering. Automation of design eliminates the slow and costly manual drafting procedures previously used.

Figure 9 traces the flow of information from the logic designer to the 704 or 705. The logic designer follows definite rules and procedures in laying out the raw logic on special sketch sheets. From these forms, information is coded and punched into IBM cards and then fed into the computer. Design aids, manufacturing data, reference material, and the printed logic pages are the most important outputs of the computer.

ALD Diagram Format

The automated logic diagrams printed out by the 704 or 705 aid in the understanding of the various logic operations, simplify logic tracing and locate the circuit components. Standard blocks and symbols are used to represent specific circuit configurations. Use of the automated logic diagrams allows for standardized logic diagrams between all personnel and all plant locations.

Page Layout

An automated logic diagram consists of page identification, edge information, logic blocks, their connecting lines, and an area for comments at the bottom of the page. Figure 10 shows a typical logic page from the 7070 system.

The original logic page from the computer is 17 inches wide and 22 inches long, having a possible logic block format of five blocks wide and nine blocks long. Logic blocks may occupy any of the 45 possible positions. The actual machine systems diagrams are reduced to a more convenient size, 11 by 17 inches.

Page Identification

As shown in Figure 10, the following information is found at the top of the systems page:

1. *Page Part Number.* Used for ordering a specific page.
2. *Title.* A description of the logic contained on the systems page.
3. *Machine Number.* The number assigned a given frame or machine (e.g., 7601).
4. *Logic Page Number.* A seven-digit number (xx. xx. xx. x) assigned the logic page. For explanation purposes, letters are used to designate each position in the number: AB. CD. EF. G.

Position A: Primary breakdown according to the machine number (e.g., input-output 7603).

Position B: Secondary breakdown according to a feature group such as the arithmetic circuits.

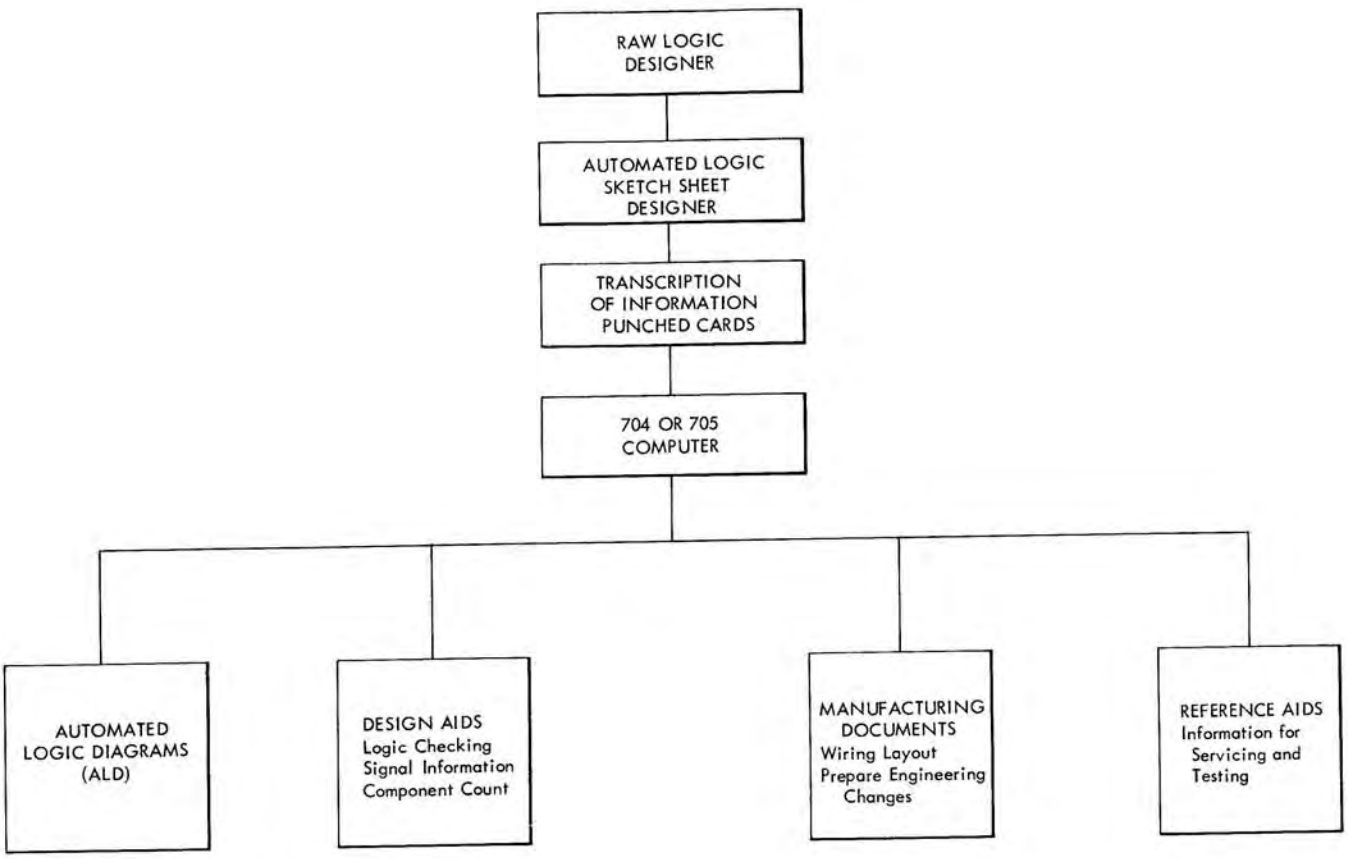


Figure 9. Automation of Design

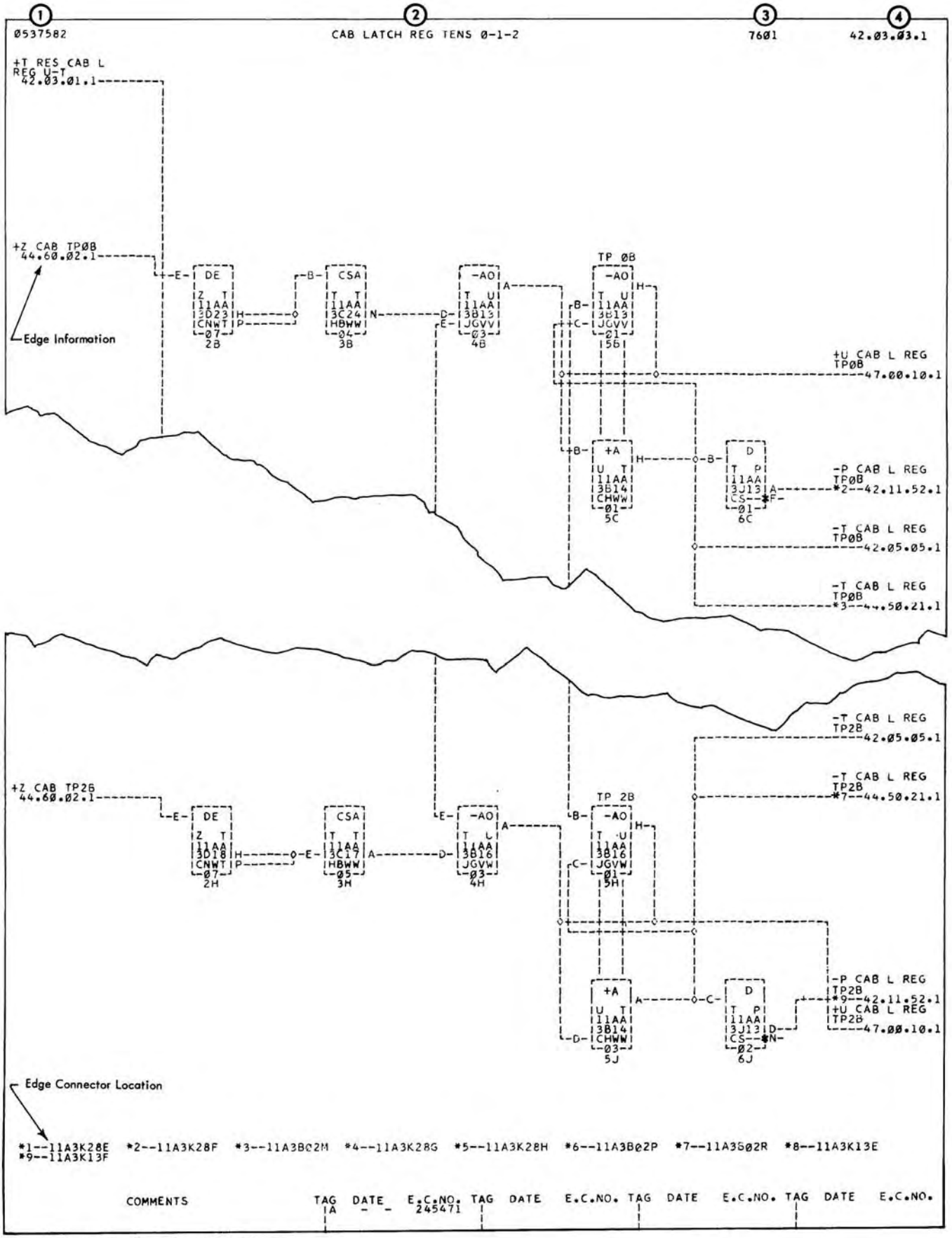


Figure 10. Logic Page for 7070 System

Positions C and D: Major logical group within the feature group, such as the adder drivers or the drum read circuits.

Positions E and F: Page number within the major logical group.

Position G: An insert page number, or reference page notation.

5. *Comments.* At the bottom of the page are listed the edge-connector locations used for the entry and exit lines on the logic page, and an area reserved for comments. Any pertinent information concerning the logic on the systems page is noted here, along with additional data about the various engineering changes affecting the logic page.

Signal Lines, General

1. All lines entering or leaving a systems page are labeled and correspond to the symbol and sign of the logic block they connect.
2. Lines enter on the left side of the systems page and leave on the right side of the page.
3. If a line leaves a systems page and goes to several locations on another page, the line is usually distributed on the TO page and not the FROM page.
4. If a line leaves a page and goes to several pages, but carries the same line name, it can be shown as in Figure 11.
5. When a line performs a function with the UP status as well as the DOWN status the two functions are described in the line name on the FROM page.

Edge Information (Figure 10)

Data shown in the vertical page coordinates 1 and 7 are called edge information. Edge information can consist of three lines of information, each line 15 characters in length. Edge information names input and output lines, and names the logic page the line appears on again.

The first line contains the coding and sign of the line type, followed by the signal name. (On some earlier ALD's the coaxial shield or twisted-pair reference wire of the signal line was also shown entering or leaving a page. Then the letters "cs" for coaxial shield and "tw" for a twisted-pair reference were used to indicate the coaxial shield or twisted-pair line.) The second line is reserved for continuation of the signal name, if required, and the third line lists the logic page number on which the signal appears again. The logic page number is directly opposite the signal line.

Edge Connectors

When a signal or service wire enters or leaves a panel, it may be routed through an edge connector. Signal lines connected to edge connectors are indicated by a symbol and a number or letter located on an entry line or exit line (Figure 10). These notations refer the reader to the bottom of the ALD page for the actual edge-connector location and pin number.

Reference Drawing

All locations that identify core arrays, resistors, and other components mounted on a gate, are given on a reference drawing. Signal lines on the systems pages refer to these drawings for locations. Reference drawings are easily identified by noting the logic page number. The seven-digit number always ends in zero for these drawings (xx. xx. xx. 0).

The Logic Block

To simplify the systems pages, logic blocks are used to represent the basic electronic circuits of the machine. A basic electronic function is usually represented by a single block but some functions (e.g., triggers) may require more than one block. In the case of multiple circuits on one SMS card, each circuit is represented by a separate logic block. The size of the block allows for the printing of four characters across the box and for six vertical lines of printing. The standard format of the logic block is shown in Figure 12, and is explained below.

Title

Over each logical block a ten-character name can be printed. However, only special circuits such as triggers, latches, single shots, and their associated timings, are named. The units of time used in the title are abbreviated as follows:

S Seconds
M Milliseconds
U Microseconds
° Milli-microseconds

Functional Symbol

The symbol that appears on line 1 of the block consists of a sign (where used) and the standard letter(s) that represent the circuit. The Appendix contains a listing of the symbols used.

Machine Feature Index

The machine feature index (MFI) code is shown on line 2 and indicates a circuit not normally used in the standard equipment (e.g., TD=tape drive). Two dots indicate a block used in the basic circuit.

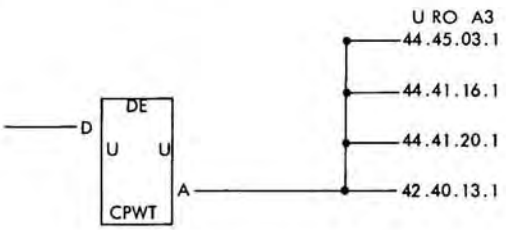


Figure 11. Multiple Outputs—Same Line Name

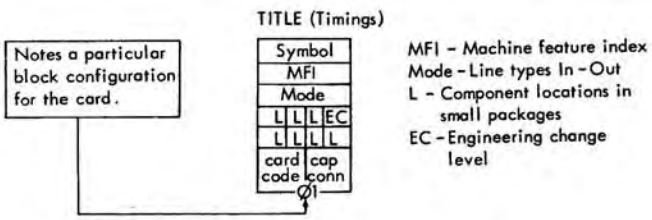


Figure 12. Logic Block Format

Circuit Type	Line Symbol	Voltage Ref.	Voltage Levels (Nom) Positive	Negative
Current Switching (N)	± N	0	+ 0.8	- 0.8
Current Switching (P)	± P	-6	- 5.2	- 6.8
CTRL (N)	± R	+6	12.0	0.0
CTRL (P)	± S	-6	0.0	-12.0
CTDL (N)	± T	0	+ 6.0	- 6.0
CTDL (P)	± U	-6	0.0	-12.0
Indicators	M	-	0.0	-36.0
Relay	± W	-	0.0	±48.0
Tube	± X	-	+10.0	-40.0
Voltage Mode	± Y	-	0.0	- 6.0
Core	± Z	-6	+ 6.0	- 6.0
Special	± V	-		

Figure 13. ALD Line Type Symbols

Mode

The third line contains symbols indicating the mode or type of input and output lines that connect the logic block. Figure 13 is a table listing the alphabetic letters used for the various line types. Each symbol represents a reference voltage with approximate swings for plus and minus line types. In most logic block configurations, the circuit type, voltage reference and swings, and translations are noted in the third printing line.

Input lines (Figure 14). A maximum of eight input lines can be shown entering the left side of the logic block. If the inputs are of the same line type, the appropriate symbol for the line type is indicated in the first printing position of line 3. To indicate multiple inputs of different line types, the input lines are grouped such that the first symbol on line 3 indicates the line type of the upper input(s) and the second symbol on line 3 indicates the lower input(s).

Output lines (Figure 14). A maximum of eight output lines can be shown leaving the right side of the logic block. Outputs from the upper half of the block indicate an out-of-phase signal, while outputs from the lower half of the block indicate an in-phase signal. In many blocks the in-phase and out-of-phase outputs are of the same line type and are indicated by the appropriate symbol in printing position 4. In blocks having multiple outputs of different line types, the symbol in printing position 3 indicates the line type of the upper output and the symbol in printing position 4 indicates the line type of the lower output.

The number, phase, and line types of the outputs are dependent upon the block representation.

Card Location and Engineering Change Level

Positions 1, 2, and 3 on line 4 and positions 1, 2, 3 and 4 on line 5 note the location of the component card in the system (Figure 12). Figure 15 relates the location information found in the logic blocks to the two types of SMS packaging used in a system. To locate the various components in the SMS packages, the numbering system follows two rules: (1) All the numbering starts at the hinge and progresses out. (2) The numbering is from the top to the bottom of the machine. Therefore, a given location can be identified by the same method from either side of a gate.

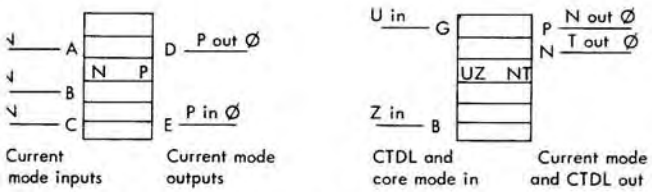


Figure 14. Examples of Line Coding

ALD Block	Line Position	4 1-2	4 3	5 1	5 2	5 3-4
Modular I		Frame	Module	Gate	Column	Row
		01-99	A, B	1-8	A-F	01-26
Modular II		Frame	Gate	Chassis	Row	Column
		01-99	A, B, C, D	1-4	A-K	01-28

Figure 15

The fourth printing position of line four indicates the engineering change level (EC) of the logic block. A "tag" letter (A, B, C) is assigned to indicate the changes in EC level. This 'tag' letter indicates that the block was affected by an engineering change made to that logic page.

Card Code and Cap Connection

The first two letters of line 6 indicate a card code that is assigned to a particular SMS card. The card codes are assigned from AA to ZZ, in that order (omitting the I and O groups). Positions 3 and 4 of line 6 indicate the cap connections used and are assigned from ZZ to AA in that order (again omitting the I and O groups). If cap connections are not used, dashes (- -) are shown in positions 3 and 4. A card code and cap connection designation is required to identify each circuit configuration on that particular card.

Logic Block Terminal Pins

Input, output, and tie-down terminal pins are indicated alphabetically, in the two character spaces between the logic block and the input or output line, as shown in Figure 16. The input and output pins are the terminals that are wired to the signal lines. Tie-down pins are terminals that are jumpered by back panel wiring to the input or the output pins. Coaxial shields or twisted-pair reference wires tied to a terminal pin are also indicated in Figure 16.

Examples of ALD Block Configurations

Basic Blocks

A large variety of logic blocks are used to perform the functions in the systems pages. Some of the most common block configurations used are illustrated in Figure 17.

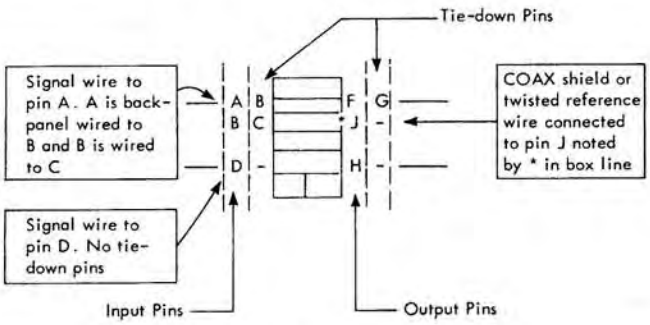


Figure 16. Logic Block Pin Connections

Two-Card Triggers

Trigger circuits are represented by a variety of block configurations and usually consist of two or more cards. The configuration used is dependent on the line type and the number of set and reset lines required. Logic blocks used in a trigger circuit are stacked vertically and are connected by dashed lines. A few typical trigger configurations are illustrated in Figure 18.

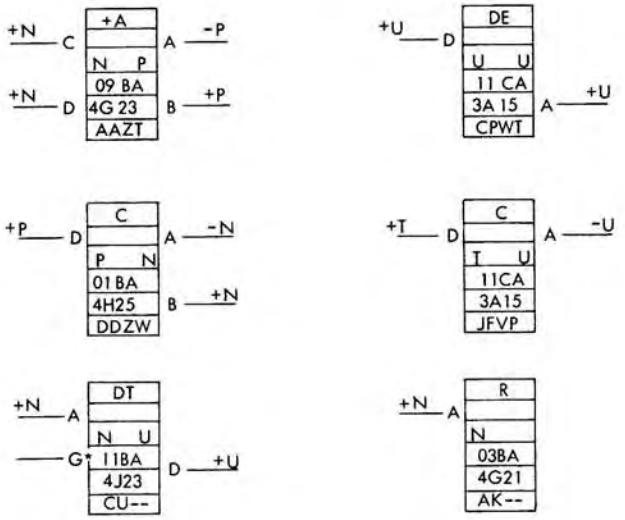


Figure 17. Basic Logic Blocks

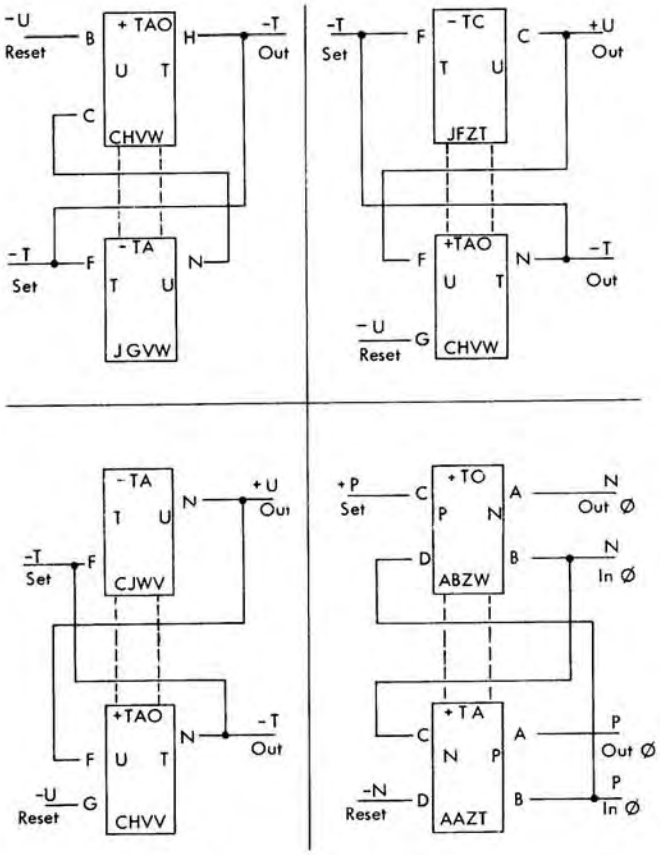


Figure 18. Two-Card Trigger Configurations

Extenders

To provide additional inputs to a logic block, extender cards are used (Figure 19). The symbol "E" is used in the extender block and dashed lines are used to show the connection to the extending block. The extender block is always placed below the extended card.

Limiters and Coupling Networks

The blocks representing coupling networks or clamp diodes that limit or terminate the outputs of a circuit are connected to the driver output as shown in Figure 20. These blocks do *not* have output lines.

DOT Functions

Under certain conditions, outputs of similar levels can be tied together, to share a common load. This connection provides a second level of logic in the output circuits, and is referred to as a DOT function. When the DOT function is performed, an additional letter is shown with the standard functional symbol (line 1) to indicate the logic performed by the output circuit (e.g., +AO, −DEA, −OA). Figure 21 illustrates the block representation of the +AO DOT function.

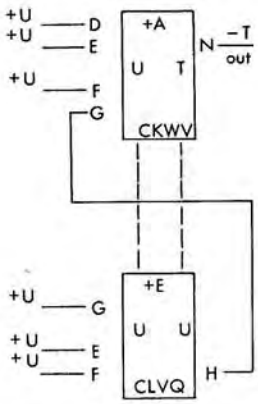


Figure 19. Extender Application

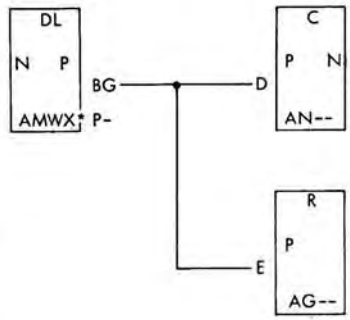


Figure 20. Coupling Network

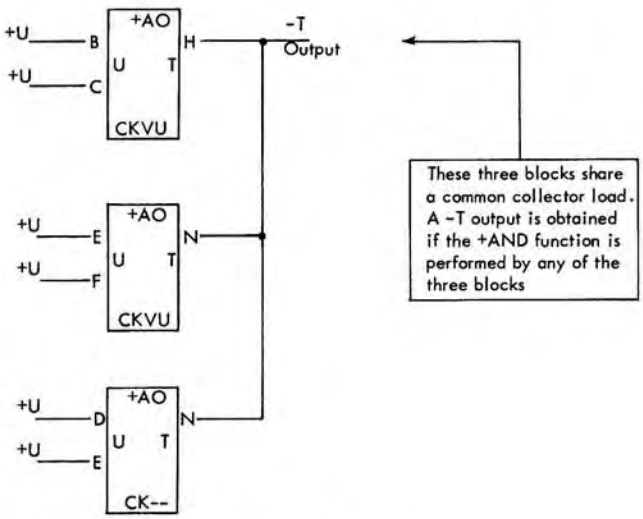
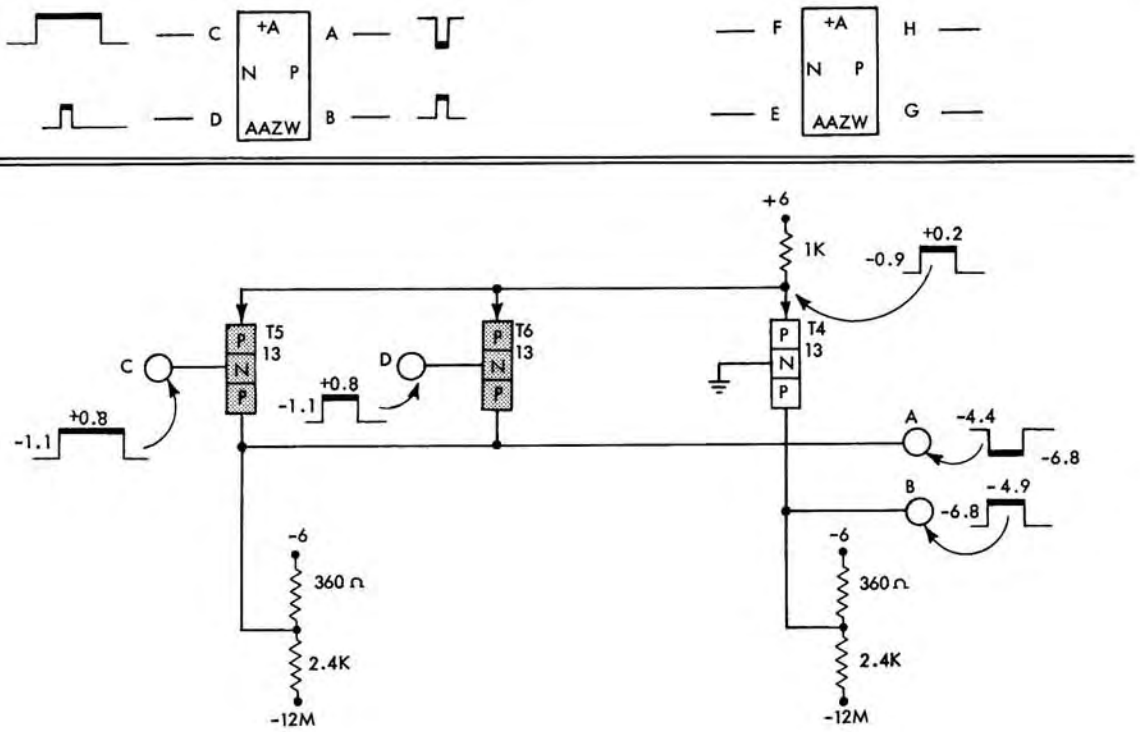


Figure 21. Example of DOT Function



Card Code	Part No 87----	Cplg N'work In Ø	Cplg N'work Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
AAZW	1204	Yes	Yes	+A	-O	+0.4	See driver for max Output Levels	-5.6	-3.5	-5.6	-3.0
AAZV	1205	Yes	No	+AO	-OA	-0.4		-6.4	-7.1	-6.4	-7.1
AAZU	1206	No	Yes	+TA	-TO						
AA- -	1207	No	No								

	Ma. Output In Ø	Ma. Output Out Ø	usec Delay per Block	usec Delay per 100uu Load	usec Delay per Driven Base
Min.	4.82	5.31	.03	.02	.03
Nom	6.0	7.6	.06	.025	.035
Max.	7.3	10.2*	.1	.03	.04

*Plus the number of inputs times .044ma

Current Mode Two-Way AND

The two-way N type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of two +N inputs produces a +P in-phase output and a −P out-of-phase output.

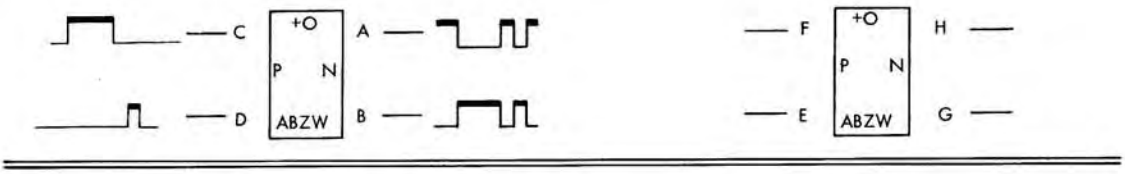
Circuit Description

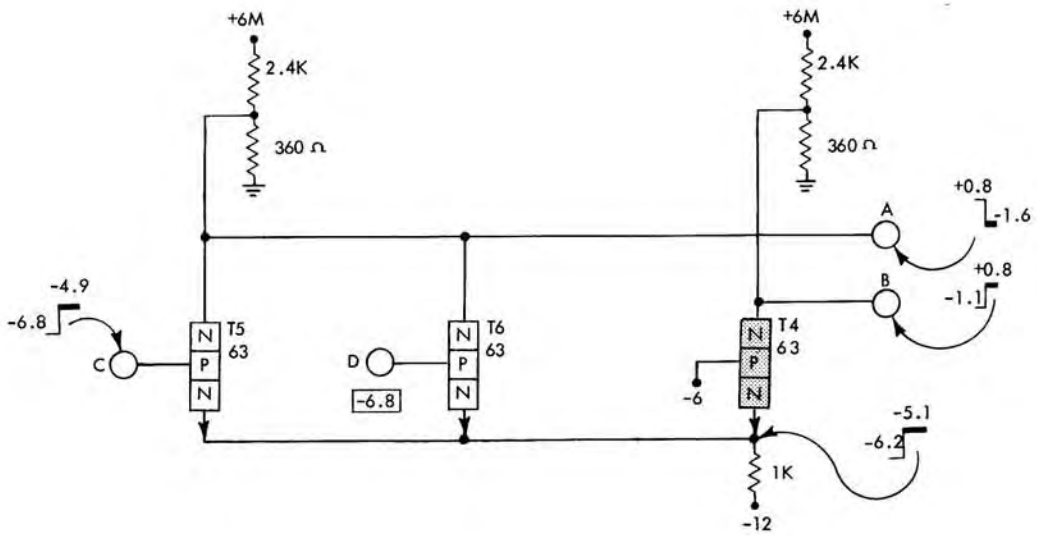
This circuit uses two transistors (T5 and T6) in an AND configuration similar to diode circuitry (the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive, 6v, supply). The emitter output of this AND circuit drives into a grounded base amplifier T4 referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v any −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output B is at a −P level of −6.8v because of divider current through its coupling network, and output A is at a +P level of −4.4v because of current flow (7.6ma) out of its coupling network through T5 and T6 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground. In so doing, it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so output A falls to a −P level and output B rises to a +P level because T4 is on.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases, cap codes ZU, ZV, and ZW - - are used as required (see chart). This circuit is also combined with an OR circuit to make up a trigger and with other AND circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.





Card Code	Part No 37---	Cplg N'work Out Ø	Cplg N'work In Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
ABZW	1213	Yes	Yes	+O	-A	-5.6	See driver for max. Output Level	+0.4	+1.2	+0.4	+1.2
ABZV	1214	Yes	No	+OA	- AO	-6.4		-0.4	-2.5	-0.4	-3.0
ABZU	1215	No	Yes	+TO	-TA						
AB--	1216	No	No								

	Ma. Output In Ø	Ma. Output Out Ø	usec Delay per Block	usec Delay per 100uu Load	usec Delay per Driven Base
Min.	4.82	5.31	.03	.02	.03
Nom.	6.0	7.6	.06	.025	.035
Max.	7.3	10.2*	.1	.03	.04

*Plus the number of inputs times .044ma

Current Mode Two-Way OR

The two-way P type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output.

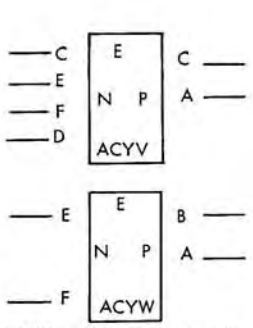
Circuit Description

This circuit uses two transistors (T5 and T6) in an OR configuration similar to diode circuitry; i.e. the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 referenced to −6v. In this state, all inputs are −P as shown, and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −1.1v because of current flow (6ma) through T4 into its coupling network. Output A is at a +N level of +0.8v because of divider current through its coupling network.

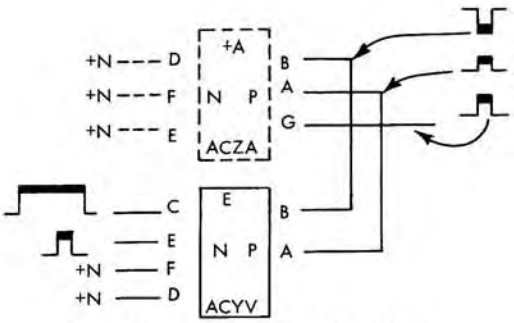
When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. Output B rises to a +N level because of divider current through its coupling network, and output A falls to a −N level of −1.6v because of current flow (7.6ma) through an input transistor into its coupling network.

Application

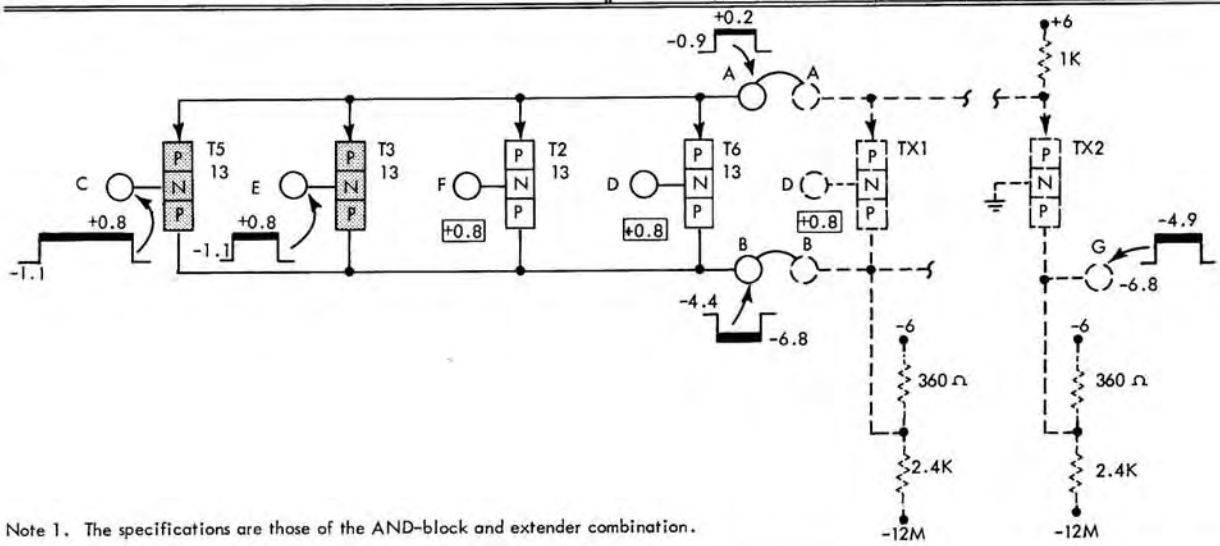
For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases cap codes ZT - -, ZU and ZV are used as required (see chart). This circuit is also combined with an AND circuit to make up a trigger with other OR circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.



2-Way and 4-Way AND Block Extenders



Typical Application of a 4-Way Extender



Note 1. The specifications are those of the AND-block and extender combination.

Card Code	Part No 37----	No of Inputs	Circuit Used as	Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
ACYV	1227	4	AND-Block	+0.4	See driver for max Output Levels	-5.6	-3.5	-5.6	-3.0
ACYW	1226	2	Extender	-0.4		-6.4	-7.1	-6.4	-7.1

	ma. Output In Ø	ma. Output Out Ø	usec Delay Per Block	usec Delay Per 100uu Load	usec Delay Per Driven Base
Min.	4.82	5.31	.03	.02	.03
Nom.	6.0	7.6	.06	.025	.035
Max.	7.3	10.2*	.1	.03	.04

* Plus the number of inputs times .044ma.

Current Mode Two-Way AND Block Extenders

This type of extender card is used in combination with an AND circuit to increase the number of input legs to the AND. As shown above, a three-way AND is increased to a seven-way AND by using the four-way extender ACYV. Had the two-way extender ACYW been used, the three-way AND would be increased to a five-way AND. In its logic, the circuit above works as a seven-way AND: the +AND function is satisfied only when all seven inputs are positive. As in any +AND circuit, the in-phase output (G) follows the sign of the function and is positive when all inputs are positive. If the −OR function is desired, the in-phase output is negative for any negative input.

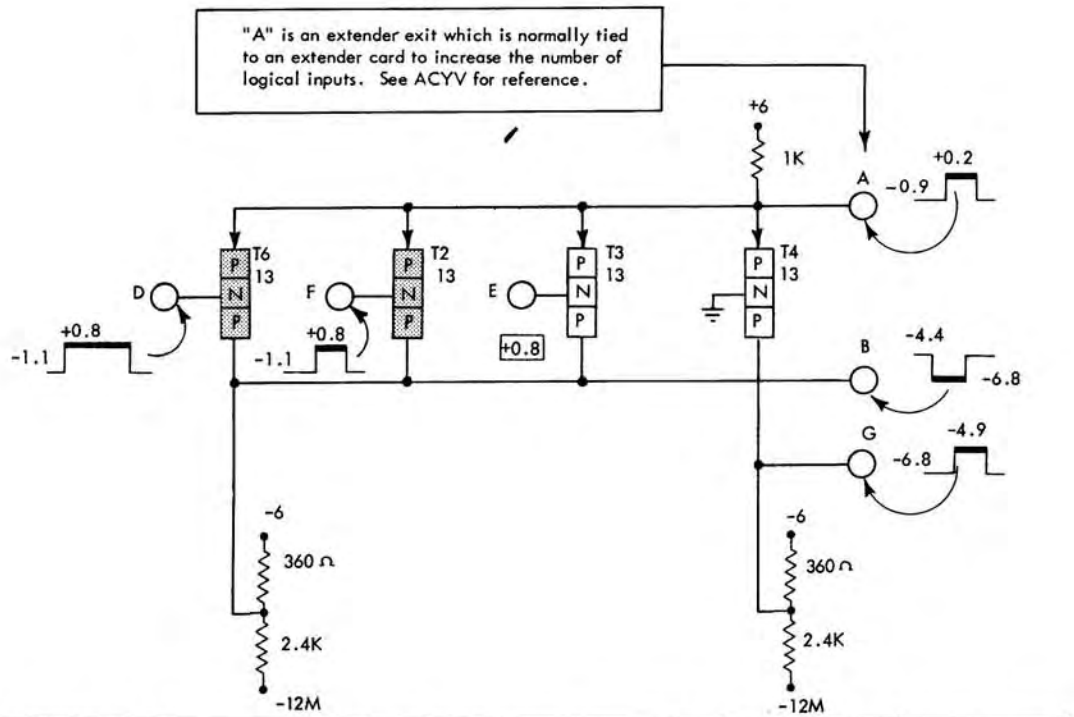
Circuit Description

The extender increases the number of inputs by connecting additional input transistors in parallel with the input transistors of the AND circuit. In the circuit above, back panel wiring A-A and B-B connects T5, T3, T2, and T6 in parallel with TX1 of the AND circuit card ACZA. Any −N input (see input C and E) forward biases an input transistor and the emitter line clamps within 0.2v to the input potential. With the emitter at 0.9v as shown, TX2 is reverse-biased and output G is at a −P level of −6.8v because of divider current through its coupling network and output B is at a +P level of −4.4 because of current flow (7.6ma) out of its coupling network through T5 and T3 to +6v.

When all inputs are positive, the emitter of TX2 attemps to rise above ground. In so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off, so output B falls to a −P level and output G rises to a +P level because TX2 is on.

Application

Extenders are used as +A block extenders or −OR block extenders.



Card Code	Part No 37----	Cplg N'work In Ø	Cplg N'work Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
ACZA	1218	Yes	Yes	+A	-O	+0.4	See driver for max Output Levels	-5.6	-3.5	-5.6	-3.0
ACYZ	1219	Yes	No	+AO	-OA						
ACYY	1220	No	Yes	+TA	-TO	-0.4		-6.4	-7.1	-6.4	-7.1
ACYX	1221	No	No								

	ma Output In Ø	ma Output Out Ø	usec Delay Per Block	usec Delay Per 100uu Load	usec Delay Per Driven Base
Min.	4.82	5.31	.03	.02	.03
Nom.	6.0	7.6	.06	.025	.035
Max.	7.3	10.2*	.1	.03	.04

* Plus the number of inputs times .044 ma

Current Mode Three-Way AND

The three-way N type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of three +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit for extender card use.

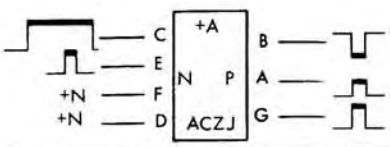
Circuit Description

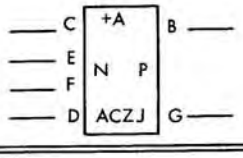
This circuit uses three transistors (T6, T2, and T3) in an AND configuration similar to diode circuitry (the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive, 6v, supply). The emitter output of this AND circuit drives into a grounded base amplifier T4 referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output G is at a −P level of −6.8v because of divider current through its coupling network, and output B is at a +P level of −4.4v because of current flow (7.6ma) out of its coupling network through T6 and T2 to +6v.

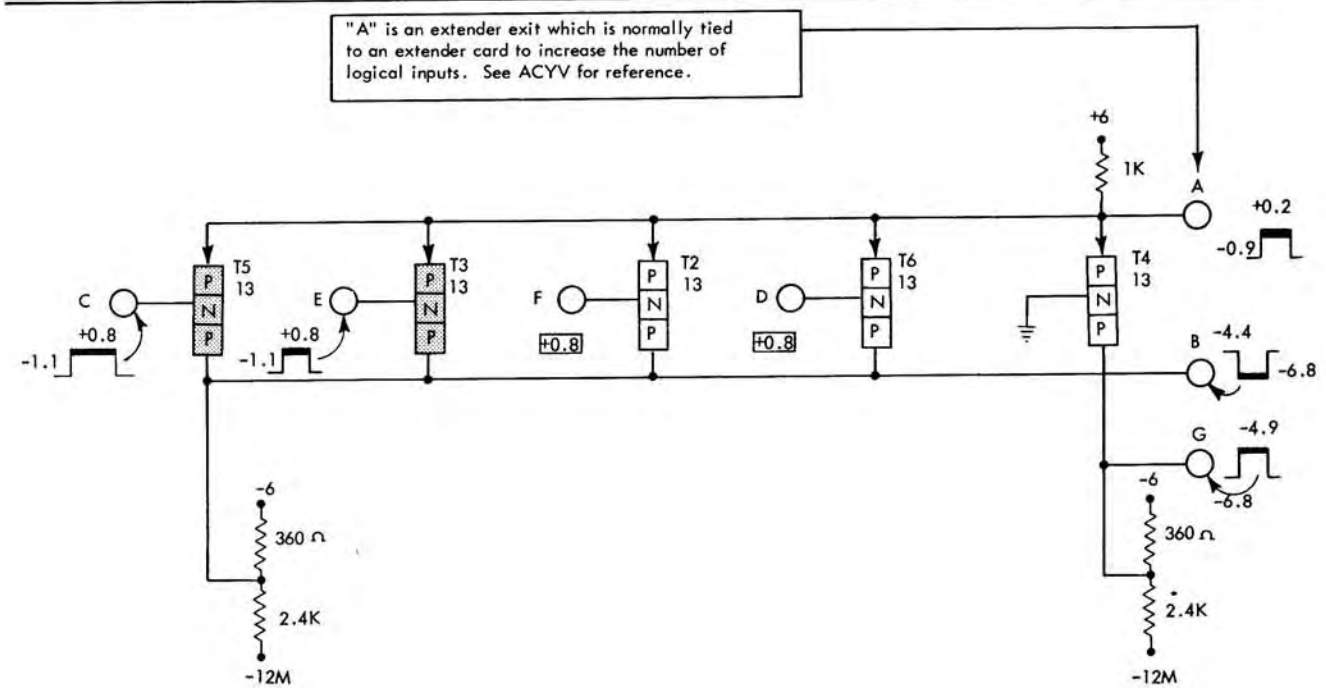
When all inputs are positive, the emitter of T4 attempts to rise above ground. In so doing, it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so output B falls to a −P level and output G rises to a +P level because T4 is conducting.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases cap codes YX, YY, and YZ are used as required (see chart). This circuit is also combined with an OR circuit to make up a trigger and with other AND circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.







Card Code	Part No 37----	Cplg Network		Circuit Used as		Input Levels		In Ø Output		Out Ø Output		ma Output			usec Delay Per		
		In Ø	Out Ø			Min.	Max.	Min.	Max.	Min.	Max.		In Ø	Out Ø	Block	100uu Load	Driven Base
ACZJ	1222	Yes	Yes	+A	-O	+0.4 -0.4	See driver for max Output Levels	-5.6 -6.4	-3.5 -7.1	-5.6 -6.4	-3.0 -7.1	Min.	4.82	5.31	.03	.02	.03
ACZH	1223	Yes	No	+AO	-OA							Nom.	6.0	7.6	.06	.025	.035
ACZG	1224	No	Yes	+TA	-TO							Max.	7.3	10.2*	.1	.03	.04
ACZF	1225	No	No														

* Plus the number of inputs times .044 ma.

Current Mode Four-Way AND

The four-way N type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

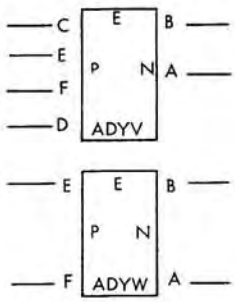
The AND circuit logic block shows that the coincidence of four +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit for extender card use.

Circuit Description

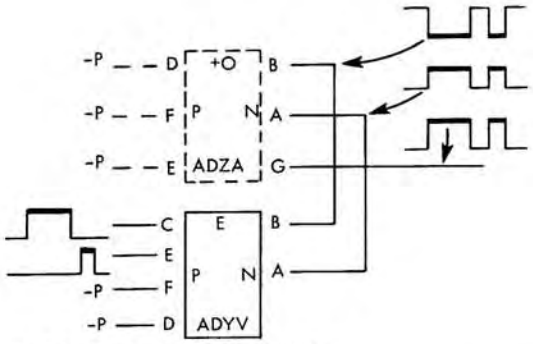
This circuit uses four transistors (T5, T3, T2, and T6) in an AND configuration similar to diode circuitry (the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive, 6v, supply). The emitter output of this AND circuit drives into a grounded base amplifier T4 referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output G is at a −P level of −6.8v because of divider current through its coupling network, and output B is at a +P level of −4.4v because of current flow (7.6ma) out of its coupling network through T5 and T3 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground. In so doing, it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so output B falls to a −P level and output G rises to a +P level because T4 is on.

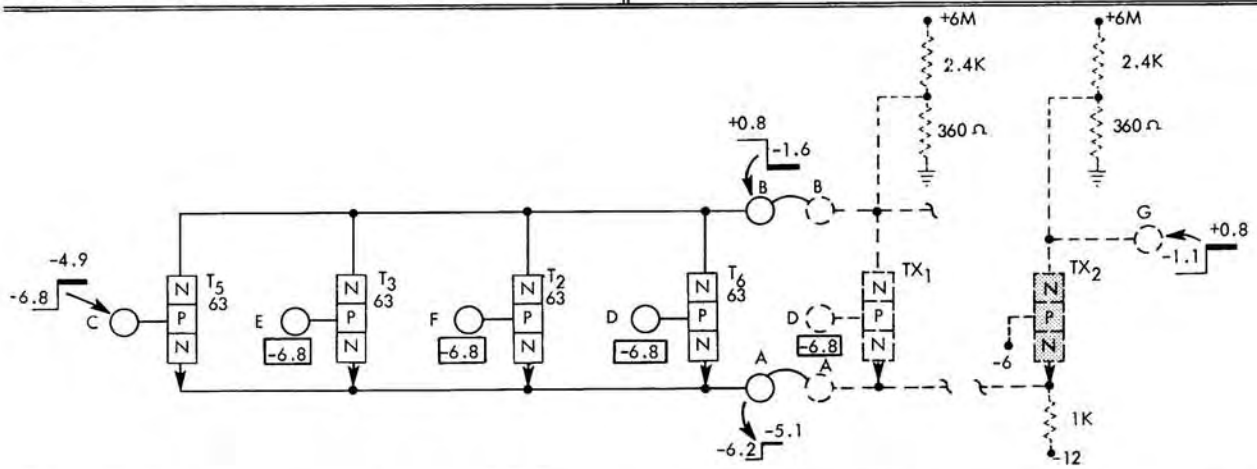
For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases cap codes ZF, ZG, and ZH are used as required (see chart). This circuit is also combined with an OR circuit to make up a trigger and with other AND circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.



2-Way and 4-Way OR-Block Extenders



Typical Application of a 4-Way Extender



Card Code	Part No. 37-----	No. of Inputs	Circuit Used as	Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
ADYV	1237	4	OR-Block Extender	-5.6 / -0.4	See driver for max. Output Levels	+0.4 / -0.4	+1.2 / -2.5	+0.4 / -0.4	+1.2 / -3.0
ADYW	1236	2							

Ma. Output	In Ø	Out Ø	usec Delay Per Block	100uu Load	Driven Base
Min.	4.82	5.31	.03	.02	.03
Nom.	6.0	7.6	.06	.025	.035
Max.	7.3	10.2*	.1	.03	.04

*Plus the number of inputs times .044 ma
Note: The above specifications are those of the OR-Block and extender combination

Current Mode Two-Way and Four-Way OR Block Extenders

This type of extender card is used in combination with an OR circuit to increase the number of input legs to the OR. As shown above, a three-way OR is increased to a seven-way OR by using the four-way extender ADYV. Had the two-way extender ADYW been used, the three-way OR would be increased to a five-way OR. In its logic, the circuit above works as a seven-way OR: the +OR function is satisfied when any of seven inputs is positive. As in any +OR circuit, the in-phase output (G) follows the sign of the function and is positive when any input is positive. If the −AND function is desired, the in-phase output is negative when all inputs are negative.

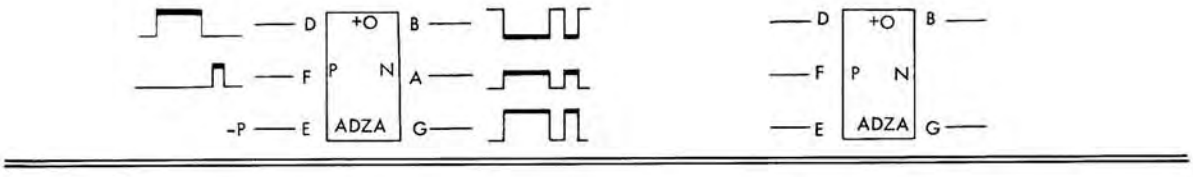
Circuit Description

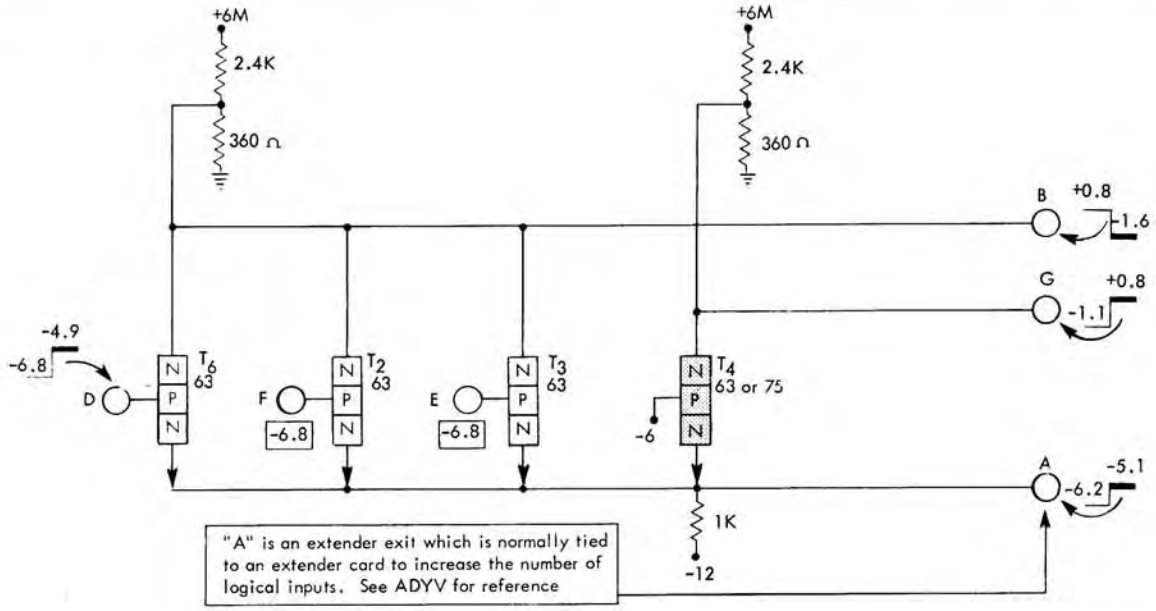
The extender increases the number of inputs by connecting additional input transistors in parallel with the input transistors of the OR circuit. In the circuit above back panel wiring A-A and B-B connects T5, T3, T2, and T6 in parallel with TX1 of the OR circuit card ADZA. When all inputs are at a −P as shown, the emitter line attempts to fall to the −P level. When the emitter of TX2 falls below −6v it becomes forward-biased and clamps to its base potential of −6v. Output G is at a −N level of −1.1v because of current flow (6ma) through TX2 into its coupling network. Output B is at a +N level of +0.8v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and TX2 is reverse biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network, and output B falls to a −N level of −1.6v because of current flow (7.6ma) through an input transistor into its coupling network.

Application

Extenders are used as +OR block extenders or −AND block extenders.





Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma Output	In Ø	Out Ø	usec Delay Per Block	usec Delay Per 100uu Load	usec Delay Per Driven Base
ADZA	1228	Yes	Yes	+O	-A	-5.6	See driver for max. Output Levels	+0.4	+1.2	+0.4	+1.2	Min.	4.82	5.31	.03	.02	.03
ADYZ	1229	Yes	No	+OA	-AO												
ADYY	1230	No	Yes	+TO	-TA	-6.4		-0.4	-2.5	-0.4	-3.0	Nom.	6.0	7.6	.06	.025	.035
ADYX	1231	No	No									Max.	7.3	10.2*	.1	.03	.04

*Plus the number of inputs times .044ma.

Current Mode Three-Way OR

The three-way P type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output. Output A is an extender exit for extender card use.

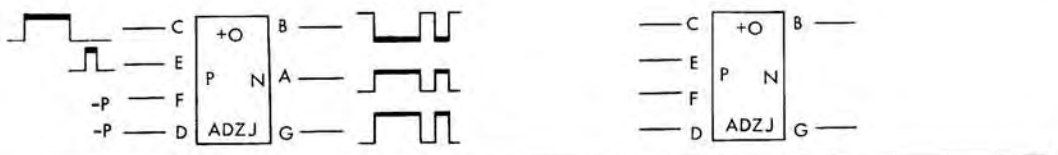
Circuit Description

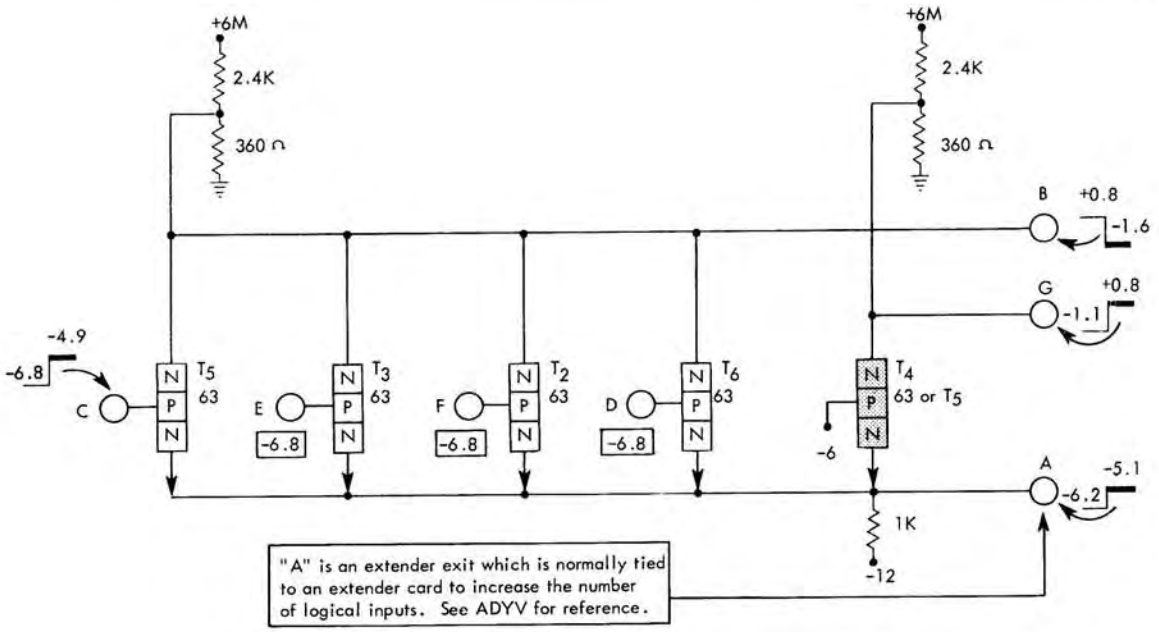
This circuit uses three transistors (T6, T2, and T3) in an OR configuration similar to diode circuitry (the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply, −12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. In this state, all inputs are −P as shown, and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v, it becomes forward biased and clamps to the base potential of −6v. Output G is at a −N level of −1.1v because of current flow (6ma) through T4 into its coupling network. Output B is at a +N level of +0.8v because of divider current through its coupling network.

When any input rises above −6v (see input D), the emitter line follows it, and T4 is reverse biased and cuts off. Output G rises to a +N level because of divider current through its coupling network, and output B falls to a −N level of −1.6v because of current flow (7.6ma) through an input transistor into its coupling network.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than 360 ohm and 2.4K resistors shown. In such cases cap codes YX, YY, and YZ are used as required (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.





Card Code	Part No. 37[1]----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma Output	In Ø	Out Ø	usec Delay Per Block	usec Delay Per 100uu Load	usec Delay Per Driven Base
ADZJ	1232	Yes	Yes	+O	-A	-5.6	See driver for max. Output Levels	+0.4	+1.2	+0.4	+1.2						
ADZH	1233	Yes	No	+OA	-AO			-0.4		-0.4		Min.	4.82	5.31	.03	.02	.03
ADZG	1234	No	Yes	+TO	-TA	-6.4			-2.5		-3.0	Nom.	6.0	7.6	.06	.025	.035
ADZF	0235	No	No									Max.	7.3	10.2*	.1	.03	.04

* Plus the number of inputs times .044 ma

Current Mode Four-Way OR

The four-way P type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output. Output A is an extender exit for extender card use.

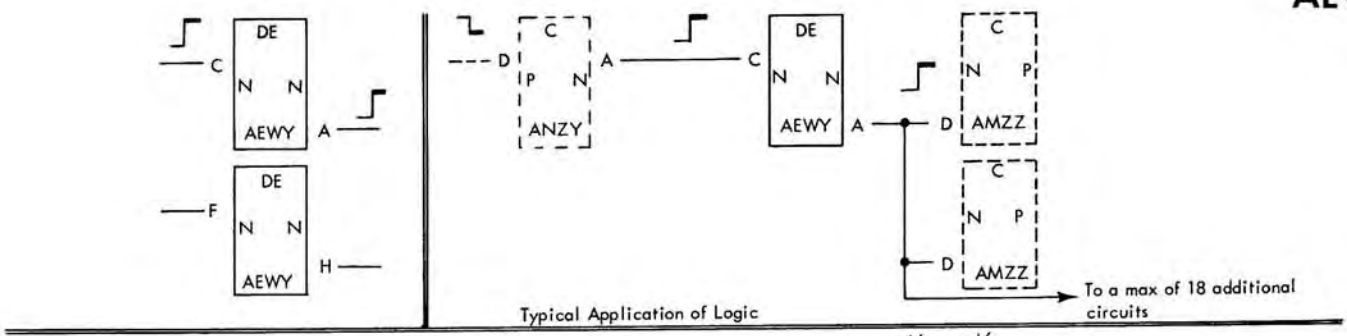
Circuit Description

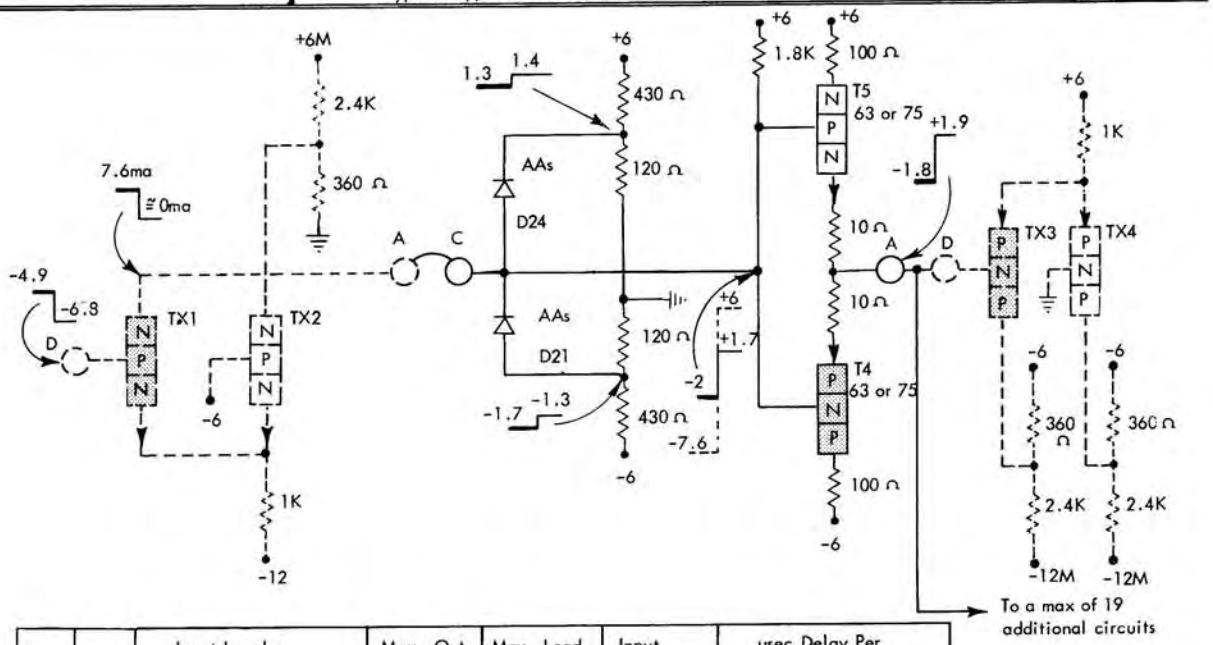
This circuit utilizes four transistors (T5, T3, T2, and T6) in an OR configuration similar to diode circuitry (the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply, −12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 referenced to −6v. In this state, all inputs are −P as shown and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v, it becomes forward-biased and clamps to the base potential of −6v. Output G is at a −N level of −1.1v because of current flow (6ma) through T4 to its coupling network. Output B is at a +N level of +0.8v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it, and T4 is reverse-biased and cuts off. Output G rises to a +N level because of divider current through its coupling network, and output B falls to a −N level of −1.6v because of current flow (7.6ma) through an input transistor into its coupling network.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases cap codes ZF, ZG, and ZH are used as required (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.





Card Code	Pt. No 37----	Input Levels Min.	Input Levels Max.	Max. Output Current	Max. Load Back Current (I_{bo}'s) Allowed	Input Current Levels (ma)		usec Delay Per C Block and DE Block	usec Delay Per 100uu Load	usec Delay Per Driven Base
AEWY	1238	+1 / -1	See driver for max. Output Levels	5ma to drive 20 bases	2.5ma	Min.	4.82	.05	.01	.012
						Nom.	7.6	.1	.01	.015
						Max.	10.8	.16	.01	.018

Current Mode N-Line Complemented Emitter Follower

This complemented emitter follower is designed to receive an N line input and to provide an in-phase N line output to drive large branching circuits. Although it can drive into twenty local logic blocks, it is not designed to drive large capacitive loads. Such loads are normally driven by line drivers. The circuit shown has a special input coupling network which converts a current input into the signal levels necessary to drive the complemented transistor configuration used. Because complemented transistors are used, the output signal has about equal rise and fall characteristics.

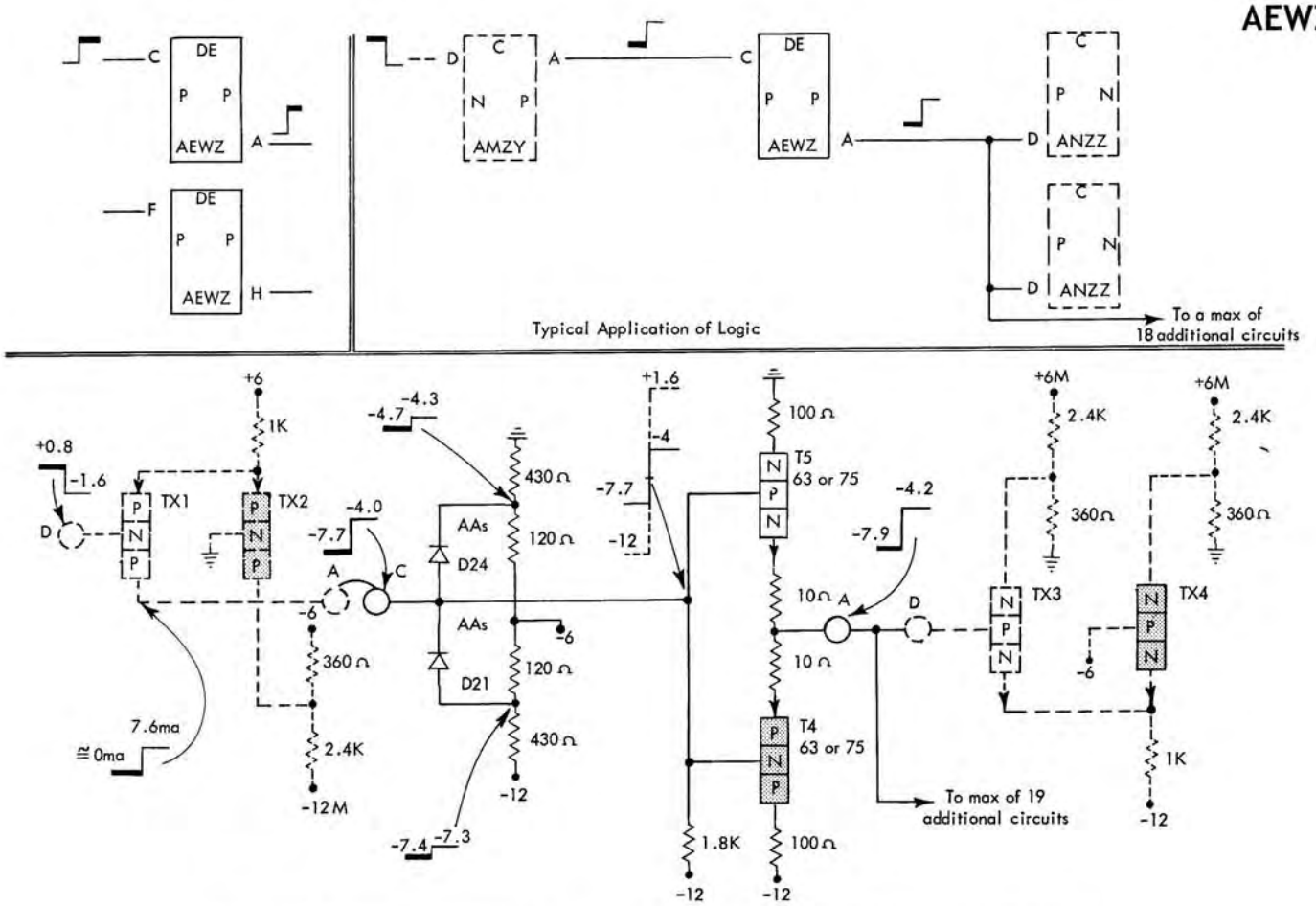
Circuit Description

As shown, TX2 is cut off and input current to C is 7.6 ma. This current seeks a plus return through 1.8K to + 6v.

This input current cannot all flow through the 1.8K because this would drop the input level to −7.6v. When the input falls below −1.3v, D21 becomes forward-biased, and some input current flows through it and 120 ohms to ground. This combination sets the input level at −2v which forward biases T4 because its emitter looks at the emitter level of TX3 which is about 0v. T4 conducts and supplies input current for a maximum of 20 TX3's.

When the input to TX1 falls below −6v it cuts off and the input current to C falls to zero. Input C attempts to rise to +6v but never reaches this level because D24 becomes forward-biased and clamps the input to +1.7v. As input C rises above zero, T4 is cut off and T5 is forward-biased.

T5 provides a low impedance for discharging line capacity and as a return for the back current of 20 TX3's.



Card Code	Part No. 37----	Input Levels Min.	Input Levels Max.	Max Output Current	Max Load Back Current ($I_{bo's}$) Allowed	Input Current Levels (ma)		usec Delay Per C Block and DE Block	usec Delay Per 100uu Load	usec Delay Per Driven Base
AEWZ	1239	-5 / -7	See driver for max Output Levels	5ma to drive 20 bases	2.5ma	Min.	4.82	.05	.01	.012
						Nom.	7.6	.1	.01	.015
						Max.	10.8	.16	.01	.018

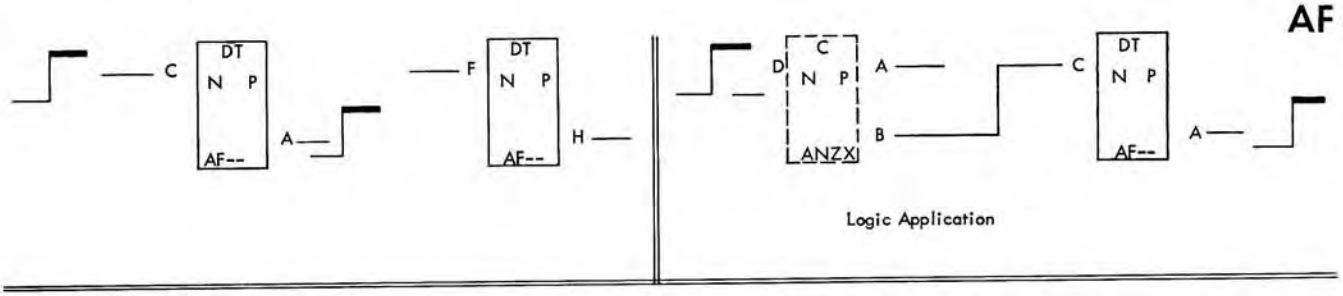
Current Mode P-Line Complemented Emitter Follower

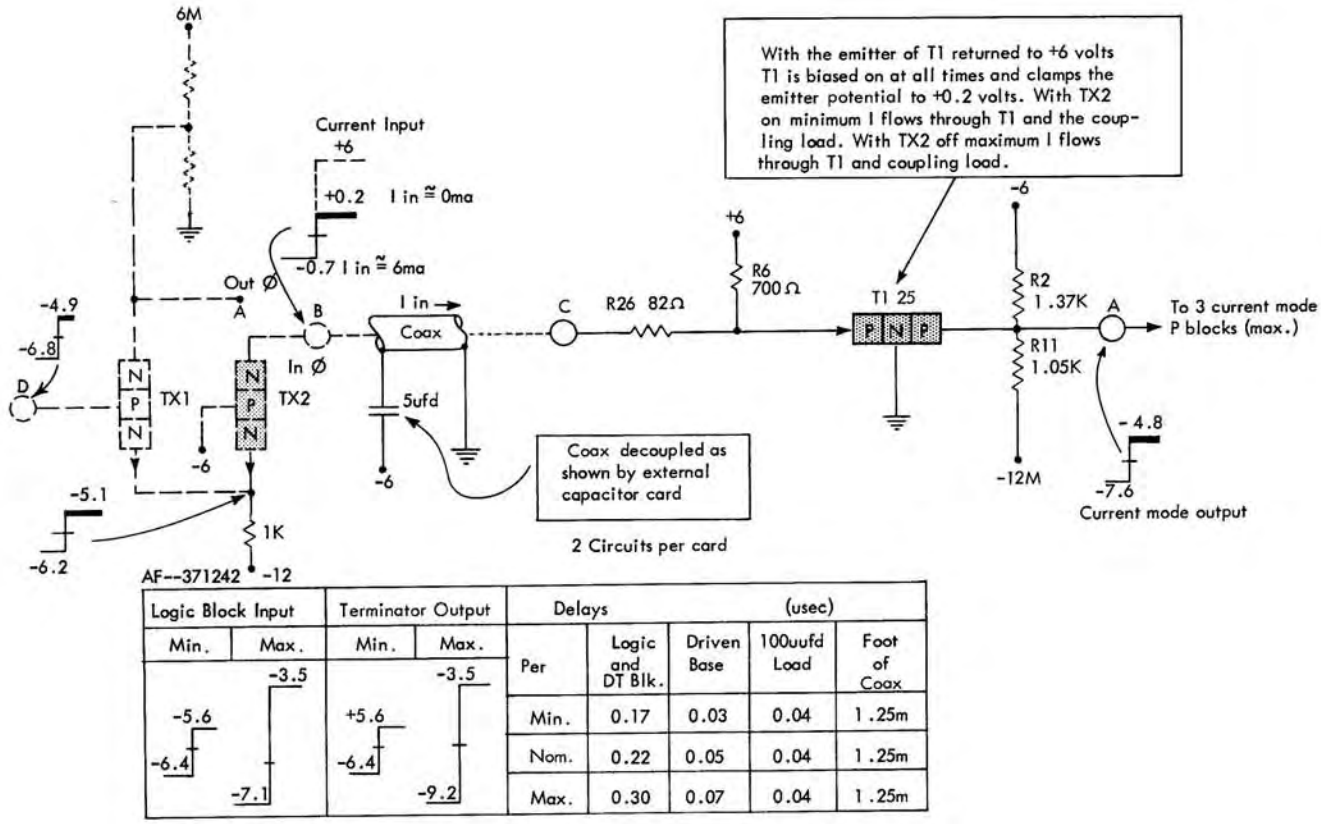
This complemented emitter follower is designed to receive a P line input and to provide an in-phase P line output to drive large branching circuits. Although it can drive into twenty local logic blocks, it is not designed to drive large capacitive loads. Such loads are normally driven by line drivers. The circuit shown has a special input coupling network which converts a current input into the signal levels necessary to drive the complemented transistor configuration used. Because complemented transistors are used, the output signal has about equal rise and fall characteristics.

Circuit Description

In the state shown, TX1 is cut off and the input current to C is zero. The input attempts to fall to −12v but never reaches this level because D21 becomes forward-biased and clamps the input to −7.7v. At this time, T4 is forward-biased because its emitter looks at the emitter level of TX3 which is about −6v. T4 conducts and provides a low impedance to charge line capacity and supplies the back current of 20 TX3's.

When the input level to TX1 falls below ground, it conducts and draws 7.6ma out of input C. Part of the current is drawn from −12v through the 1.8K to input C. All the current is not supplied through the 1.8K because this would raise the input level to +1.6v. When the input rises above −4.7v, D24 becomes forward-biased. Thus, input current is also supplied from −6v through 120 ohms and D24. Current flow through this combination sets the input level at −4v. When the input level rises above −6v, T4 cuts off and T5 conducts. Conduction through T5 supplies input current for a maximum of 20 TX3's.





Logic Block Input		Terminator Output	
Min.	Max.	Min.	Max.
-5.6	-3.5	+5.6	-3.5
-6.4	-7.1	-6.4	-9.2

Delays (usec)				
Per	Logic and DT Blk.	Driven Base	100uufd Load	Foot of Coax
Min.	0.17	0.03	0.04	1.25m
Nom.	0.22	0.05	0.04	1.25m
Max.	0.30	0.07	0.04	1.25m

Current Mode N-Type Transmission Line Terminator

This card has two PNP transmission line terminator circuits used to terminate a coaxial cable in its proper impedance match and reference voltages. The 93 ohm coaxial cable is driven by the in-phase output of a P type logic block or an equivalent driving circuit. This terminator is used only with the in-phase output of the logic block. Each circuit accepts a N input and translates the signal to an in-phase P output.

The shield of the coaxial cable is tied to the base potential of the line terminator transistor and is decoupled to −6 volts by a 5μfd capacitor at the driving end.

Circuit Description

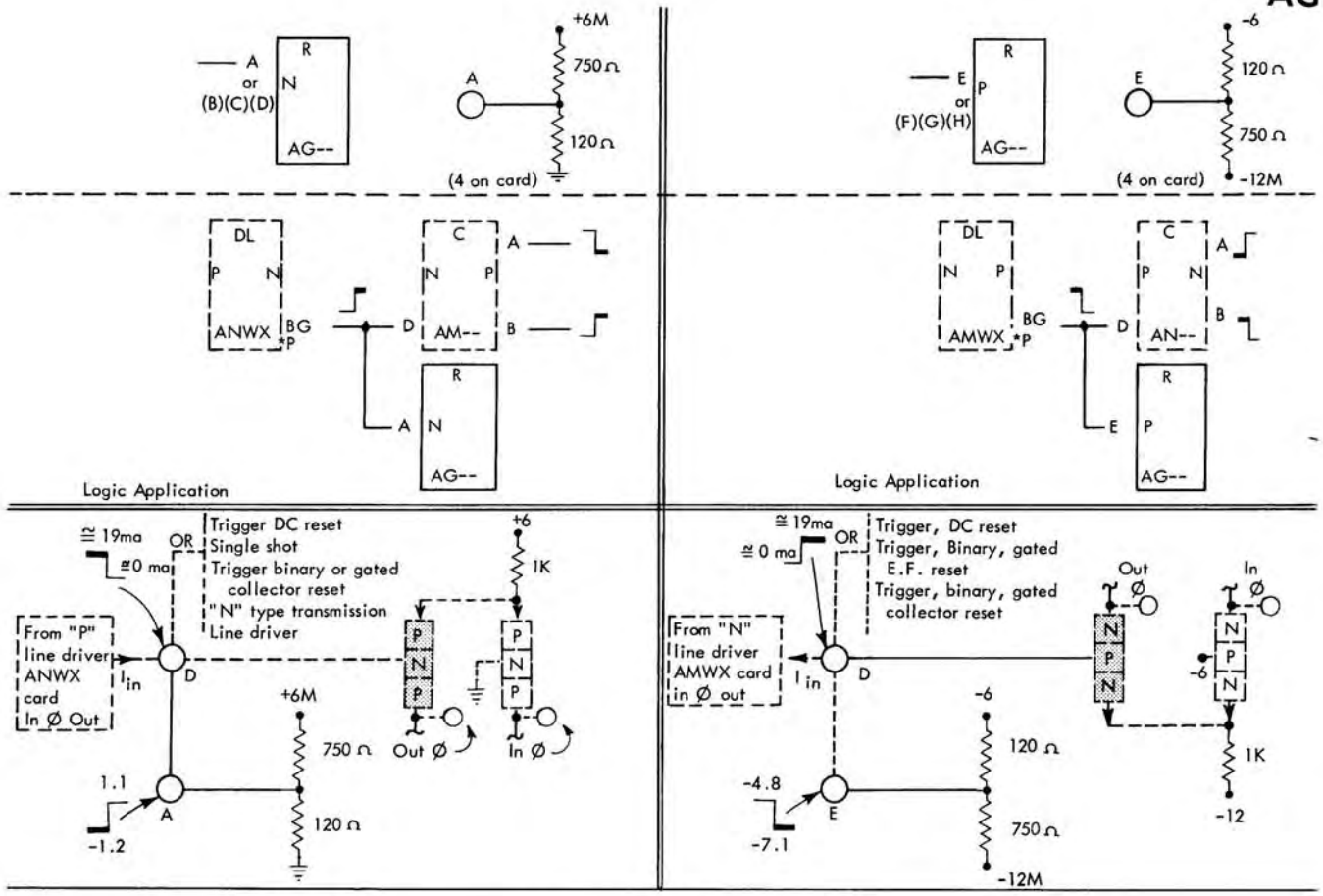
A typical use of the PNP transmission line terminator is shown. T1 is operated class A with at least 0.5ma of emitter current flowing at all times. The 82 ohm input resistor in series with the base-emitter impedance of the common base amplifier (T1) provides the optimum impedance match for the 93 ohm coaxial cable and the line terminator circuit.

With a −P input to the driver circuit, TX2 is forward-biased on and supplies about 6ma to the cable, R26, and R6 to the +6 volt supply. Minimum current of at least 0.5ma flows from the load through T1 to R6 and the +6v supply. The output at pin H of the line terminator is a −P level.

When a +P input appears at pin D, TX2 is reverse-biased off and current ceases to flow from the driver into the cable. Conduction from the coupling load through T1 to R6 and the +6v supply increases to approximately 8.5ma. The output at pin H of the line terminator increases to a +P output level.

Application

The output from each PNP transmission line terminator can drive into a maximum of three current mode P blocks.



AG-- 371240

Current input when driven by			Max Load Back Current (I_{bo}'s) Allowed	N In Ø O'put		N Out ØO'pt		P In Ø O'put		P Out Ø O'pt		Loading No of Bases Driven	
	Output			Min.	Max.	Min.	Max	Min.	Max.	Min.	Max.		
	In Ø	Out Ø										In Ø	Out Ø
Min.	15.9	17.5		+0.6	+1.2	+0.6	+1.2	-5.4	-4.5	-5.4	-3.0		
Nom.	19.0	23.0	1.01 ma	-0.6	-1.5	-0.6	-3.0	-6.6	-7.2	-6.6	-7.2	4	4
Max.	23.7	32.1											

Current Mode Transmission Line Driver Coupling Network

The AG - - card has eight resistor networks used to terminate the current mode transmission line drivers and cable output to their proper reference voltage. These coupling networks are located at the load end of the cable. Four of the coupling loads, with outputs at pins A, B, C, and D, terminate NPN transmission line driver circuits that are loaded by N type logic blocks.

The four coupling networks with outputs at pins E, F, G, and H terminate PNP transmission line driver circuits that are loaded by P type logic blocks.

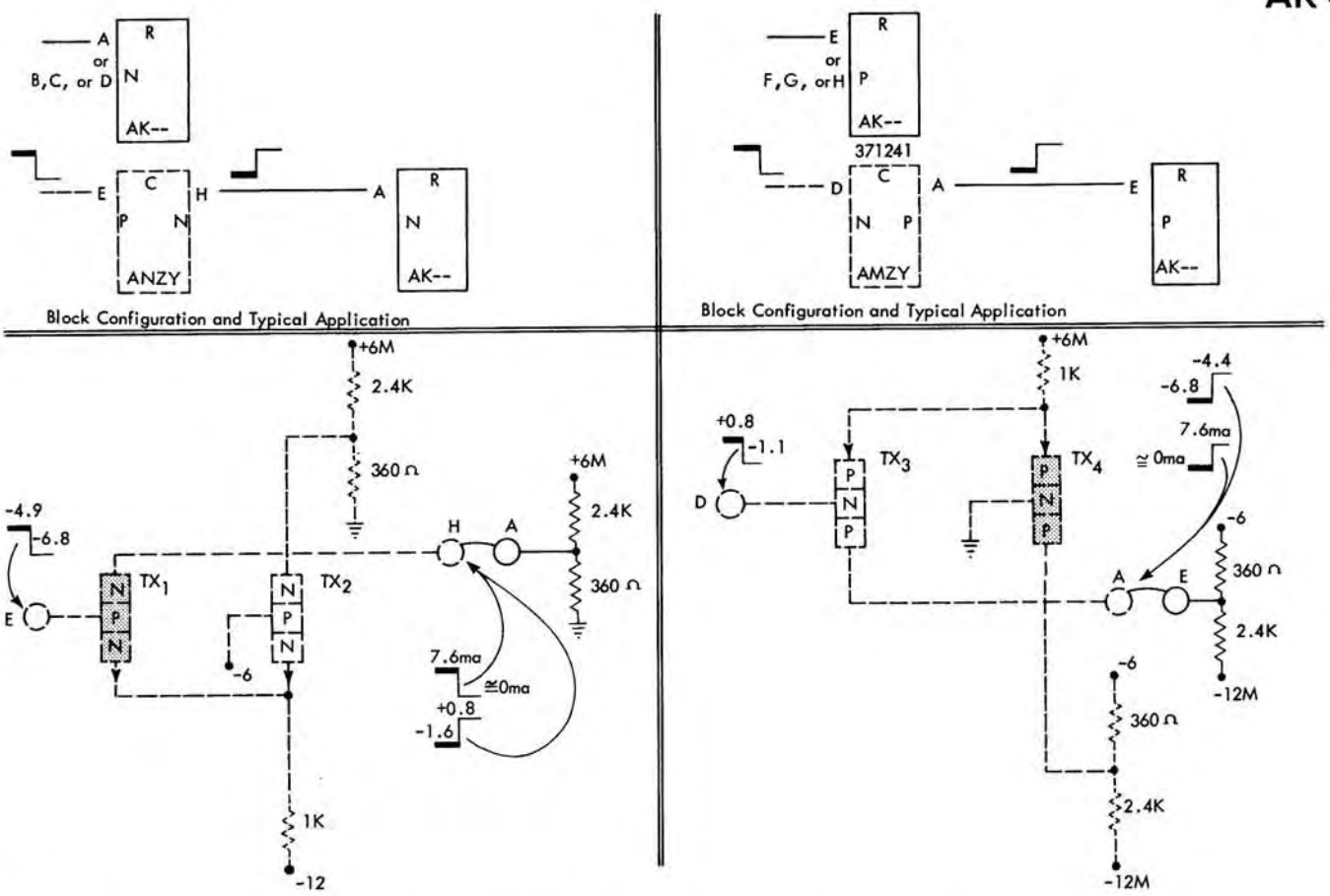
Circuit Description

The schematic above showing a P-type line driver is terminated by a N-type coupling network. When the driver is on, about 19ma flows from the driver into the coupling network which results in a −N output. When the driver is off, current ceases to flow to the coupling network and a +N output is obtained from the driver.

Circuit operation is similar for a N type line driver terminated by a P type coupling load.

Application

These coupling networks are used to properly terminate both the in-phase and out-of-phase outputs of the line drivers.



AK--, 371241

Current Input When Driven by			Max Load Back Current (I_{bo}'s) Allowed	N in Ø Output		N Out Ø Output		P In Ø Output		P Out Ø Output		Max. No of Bases Driven by Network (Pyramiding Factor)						
	In Ø	Out Ø		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	No. of Inputs to Logic Block	3	6	9	12	15	30
Min.	4.82	5.31		+0.4 / -0.4	+1.2 / -2.5	+0.4 / -0.4	+1.2 / -3.0	-5.6 / -6.4	-3.5 / -7.2	-5.6 / -6.4	-3.0 / -7.2	In Ø	4	4	4	4	4	4
Nom.	6.0	7.6										Out Ø	5	4	3	2	1	-
Max.	7.3	10.2	.926 ma															

Current Mode N and P Block Coupling Network

This card provides eight networks; four to terminate N lines and four to terminate P lines. Their purpose is to provide an acceptable collector load for either an in-phase or an out-of-phase output which has no termination.

To understand why such networks are necessary, look at the typical application of an N line coupling network shown above left. Note that the out-of-phase output H of ANZY is tied to a coupling network. Such a connection is required when this output is not used to drive other circuits. The network is not located on the ANZY card because the out-of-phase output of this card provides a current output designed to drive into circuits requiring a current input. Examples of current input circuits are line drivers, line terminators and power drivers. The same reasoning applies to the ANZY card above, which has a P line coupling network tied to its output A.

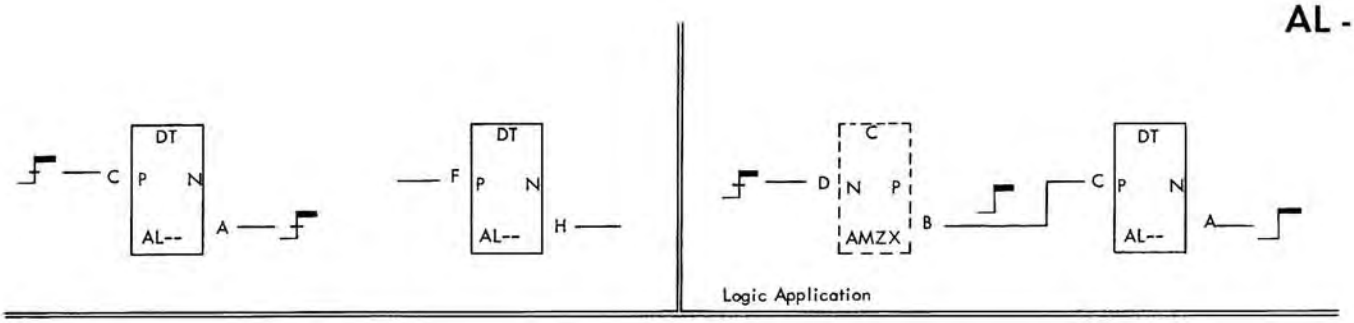
Circuit Description

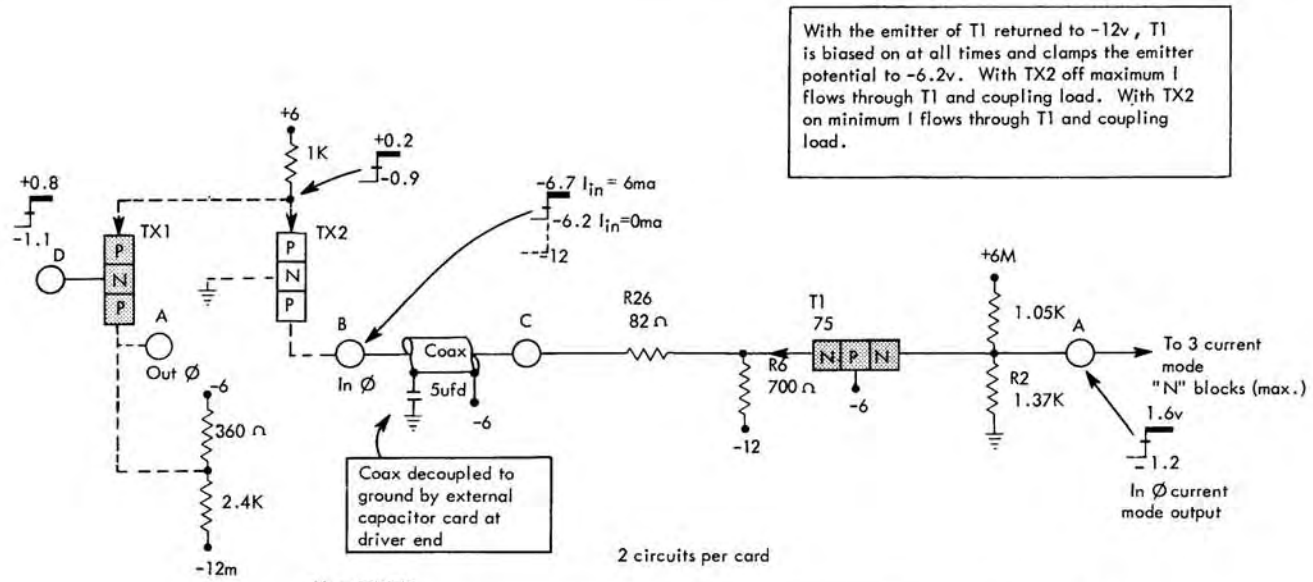
The N line coupling network provides a collector load for TX1. The load is necessary to accept the nominal 7.6ma of current flow through TX1 when the input is at −4.9v. Without this termination, the collector would be open circuited and the emitter-to-base diode would draw heavy input current and load down the driving circuit. The same reasoning applies to the P line coupling network; it acts as a suitable collector load for TX3.

The specification chart above also contains pyramiding factor information which describes the load that can be placed on this network when it is used as a voltage source.

Application

This card is used to terminate a circuit which has no termination.





AL-- 371243

Logic Block Input		Terminator Output		Delays (usec)				
Min.	Max.	Min.	Max.	Per	Input and DT Block	Driven Base Loading	100uufd Load	Foot of Coax
+0.4 / -0.4	+1.1 / -2.5	0.4 / -0.4	3.2 / -2.5	Min.	0.17	0.03	0.04	1.25m
				Nom.	0.22	0.05	0.04	1.25m
				Max.	0.30	0.07	0.04	1.25m

Current Mode P Type Transmission Line Terminator

This card has two NPN transmission line terminator circuits used to terminate a coaxial cable in its proper impedance match and reference voltages. The 93 ohm coaxial cable is driven by the in-phase output of a N type logic block or an equivalent driving circuit. This terminator is used only with the in-phase output of the logic block. Each circuit accepts a P input and translates the signal to an in-phase N output.

The shield of the coaxial cable is tied to the base potential (−6v) of the line terminator transistor and is decoupled to ground by a 5μfd capacitor at the driving end.

Circuit Description

A typical use of the NPN transmission line terminator is illustrated above. T1 is operated class A with at least 0.5ma of emitter current flowing at all times. The 82 ohm input resistor in series with the base-emitter impedance of the common base amplifier (T1) provides the optimum impedance match for the 93 ohm coaxial cable and the line terminator circuit.

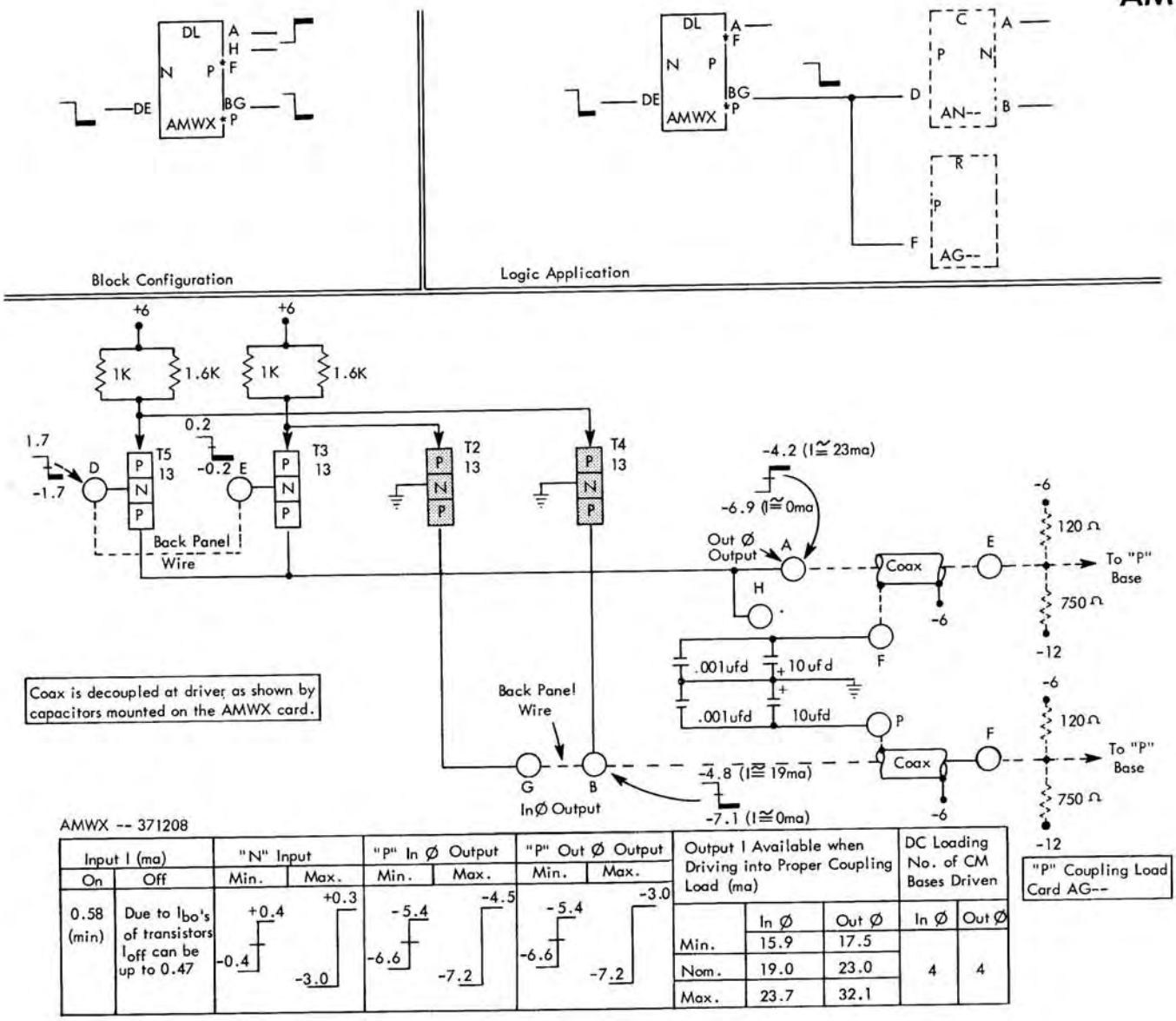
With a −N input to the driver circuit, TX2 is reverse-biased off and prevents the flow of drive current from the terminator and the cable. At this time, however, about 8.5ma flows from the −12 volt supply through R6 and T1 into the coupling network and load. This conduction provides a −N output at pin A of the line terminator.

When a +N input appears at pin D, TX2 is forward-biased on. Conduction from the −12 volt supply and R6 now supplies 6ma to the cable and TX2.

At least 0.5ma flows through T1 into the coupling load and provides a +N output at pin A of the line terminator.

Application

The output from each NPN transmission line terminator can drive into a maximum of three current mode N blocks.



AMWX -- 371208

Input I (ma)		"N" Input		"P" In Ø Output		"P" Out Ø Output		Output I Available when Driving into Proper Coupling Load (ma)			DC Loading No. of CM Bases Driven	
On	Off	Min.	Max.	Min.	Max.	Min.	Max.		In Ø	Out Ø	In Ø	Out Ø
0.58 (min)	Due to I_{bo}'s of transistors I_{off} can be up to 0.47	+0.4 / -0.4	+0.3 / -3.0	-5.4 / -6.6	-4.5 / -7.2	-5.4 / -6.6	-3.0 / -7.2	Min.	15.9	17.5	4	4
								Nom.	19.0	23.0		
								Max.	23.7	32.1		

Current Mode N Transmission Line Driver

This card has a transmission line driver circuit and a capacitor decoupling network used to power signals into coaxial cables. The circuit accepts an N input and provides in-phase and out-of-phase P outputs which drive into 93 ohm coaxial cables terminated in their proper resistor coupling networks. Use of coaxial cable eliminates stray pickup, decreases transmission line delays due to cabling, and connects two different reference levels when driving between distant points.

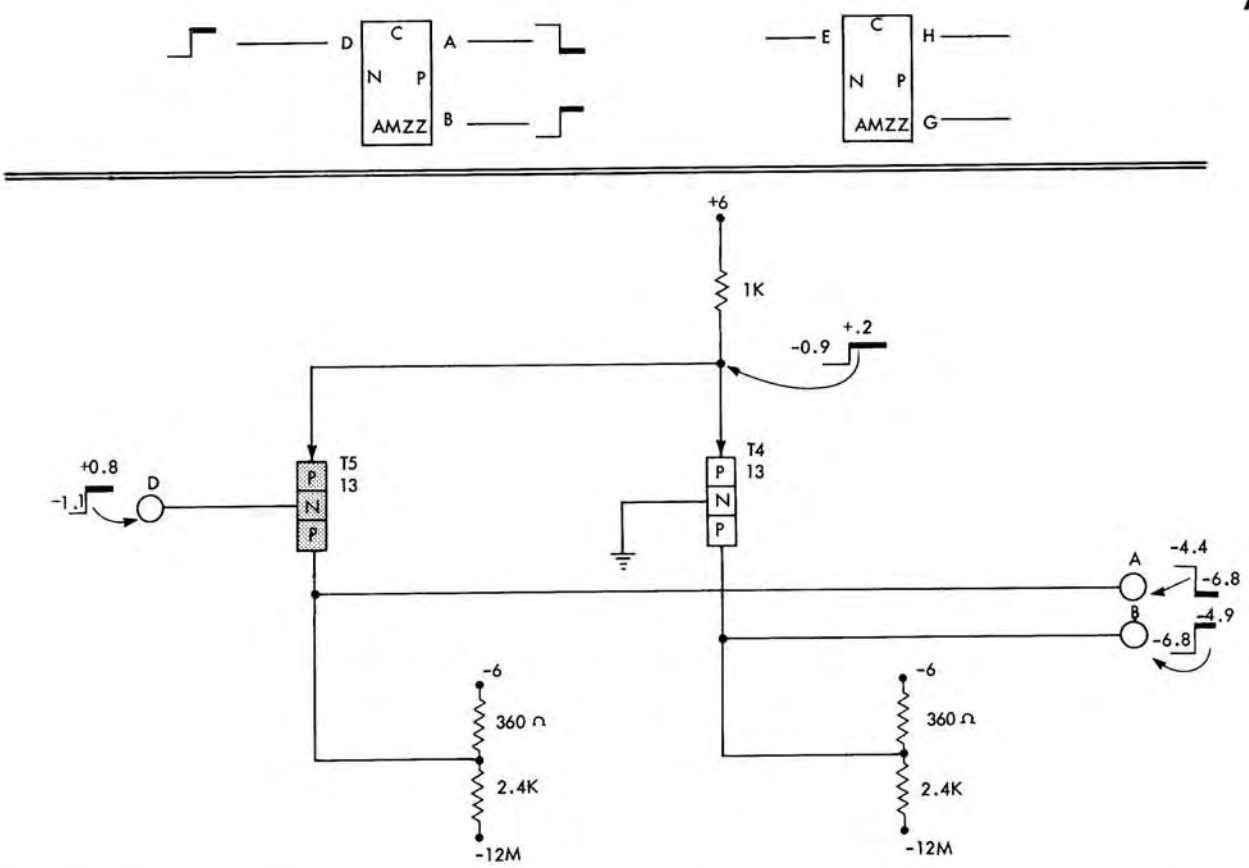
The circuit is basically two single input logic blocks with their collectors tied together for higher output drive currents. The coaxial cable shields are tied directly to −6 volts at the loading end of the transmission lines and are decoupled at the driving end of the line by the capacitor decoupling networks on the card.

Circuit Description

A typical line driver application is shown above. Assume a starting condition of T4 and T2 conducting and the common emitter voltages of the transistors at +0.2v. A +N input at pin D reverse biases T5 and T3 off, giving a −P inverted output at pin A. Conduction of about 19ma from the in-phase load and the coupling networks through T4 and T2 gives a +P output at pin B. When the input to the driver decreases to −1.7v, T5 and T3 are forward-biased, and T2 and T4 are biased off. Conduction from the out-of-phase coupling network and load increases to near 23ma and gives a +P level at pin A. The in-phase output drops to a −P level because no current flows from its coupling network.

Application

When properly terminated, a maximum of four current-mode P bases can be driven by the in-phase or the out-of-phase outputs of this line driver. Back-panel wiring is required as noted above.



Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
AMZZ	1200	Yes	Yes	C	CO	+0.4	See driver for max. Output Levels	-5.6	-3.5	-5.6	-3.0
AMZY	1201	Yes	No	TC							
AMZX	1202	No	Yes			-0.4		-6.4	-7.1	-6.4	-7.1
AM--	1203	No	No								

	Ma Input In Ø	Ma Input Out Ø	usec Delay per Block	usec Delay per 100 uu Load	usec Delay per Driven Base
Min.	4.82	5.31	.03	.02	.03
Nom.	6.0	7.6	.06	.025	.035
Max.	7.3	10.2	.1	.03	.04

Current Mode N-to-P Converter

The N-to-P converter is a single input logic block. It is fed by an N line and produces both an in-phase and out-of-phase output. For a −N line input, a −P in-phase output and a +P out-of-phase output result. It is used:

1. To translate from an N to a P line.
2. To obtain a P line inversion of the input sign, i.e., a +N to a −P or a −N to a +P.
3. As a current amplifier to drive other logic blocks.

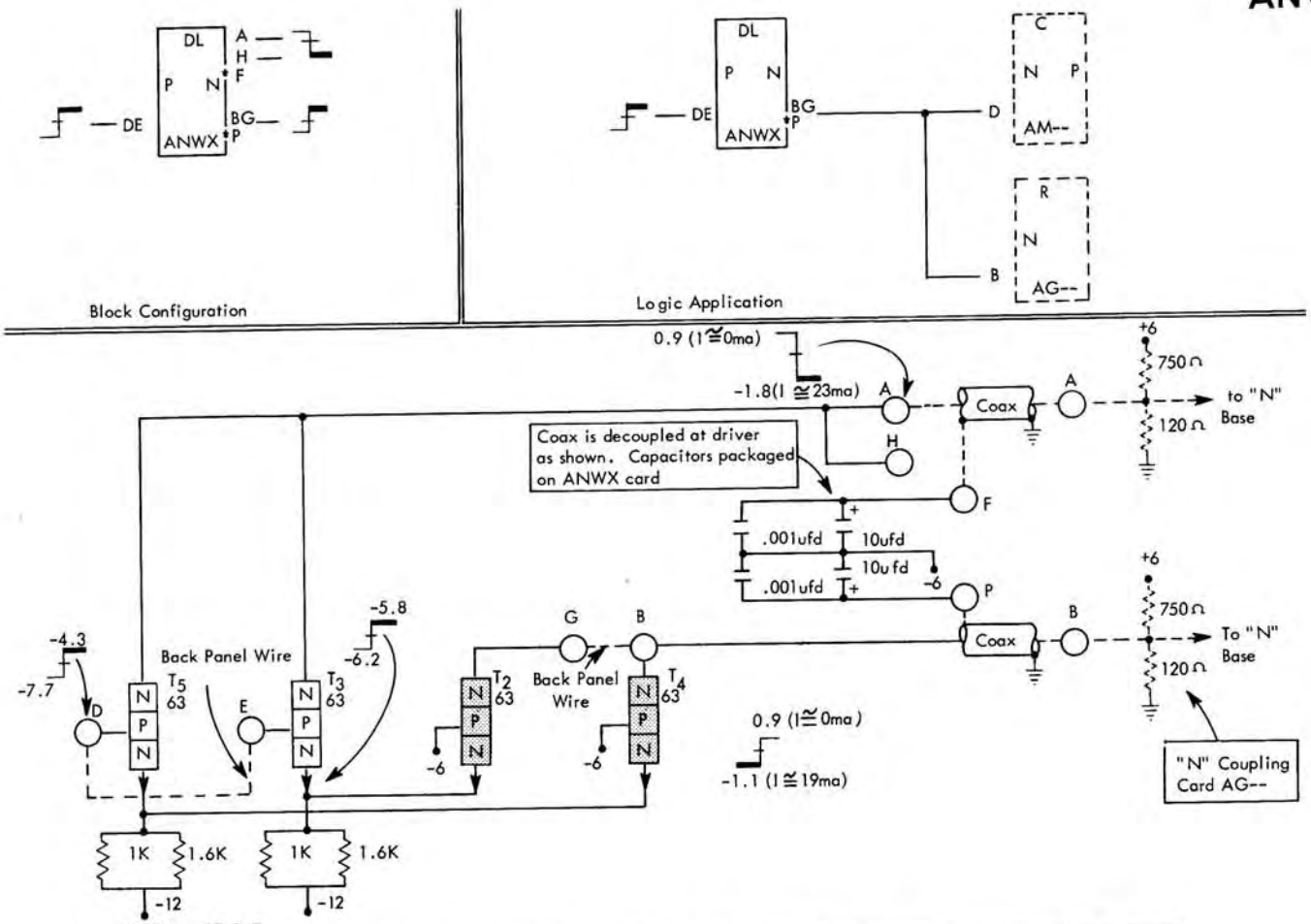
Circuit Description

This circuit configuration is that of a one-way AND circuit (the input transistor T5 has its base-to-emitter NP diode returned to a positive supply). Its emitter output drives into a grounded base amplifier T4 referenced to ground. T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output B is at a −P level of −6.8v because of divider current through its coupling network, and output A is at a +P level of −4.4v due to current flow (7.6ma) out of its coupling network through T5 to +6v.

When the input to T5 rises to a +N level the emitter of T4 attempts to rise above ground. In so doing it becomes forward-biased and clamps to its base potential. In this state, output B rises to a +P level because of current flow (6ma) out of its coupling network through T4 to +6v and output A falls to a −P level because of divider current through its coupling network.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases, cap codes ZX, ZY, and -- are used as required (see chart). This circuit is also used as a converter within a trigger (93) and in DOT functions as a CO.



Input I (ma)		"P" Input Level		"N" In Ø Output		"N" Out Ø Output		Output (I) Available When Driving Proper Coupling Load (ma)			DC Loading Possible. No of CM Bases Driven	
On	Off	Min.	Max.	Min.	Max.	Min.	Max.		In Ø	Out Ø	In Ø	Out Ø
0.58 (min)	Due to I_{bo}'s of transistors I_{off} can be up to 0.47	-6.4 to -5.6	-9.0 to -3.0	-0.6 to +0.6	-1.5 to +1.2	-0.6 to +0.6	-3.0 to +1.2	Min.	15.9	17.5	4	4
								Nom.	19.0	23.0		
								Max.	23.7	32.1		

Current Mode P Transmission Line Driver

This card has a transmission line driver circuit and a capacitor decoupling network used to power signals into coaxial cables. The circuit accepts a P input and provides in-phase and out-of-phase N outputs that drive into 93 ohm coaxial cables terminated in their proper resistor coupling networks. Use of coaxial cable eliminates stray pickup, decreases transmission line delays due to cabling, and connects two different reference levels when driving between distant points.

The circuit is basically two single input logic blocks with their collectors tied together for higher output drive currents. The coaxial cable shields are tied directly to ground at the loading end of the transmission lines and are decoupled at the driving end of the line by the capacitor decoupling networks on the card.

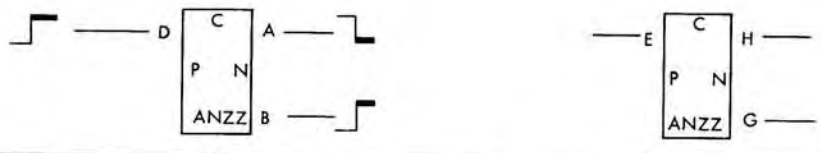
Circuit Description

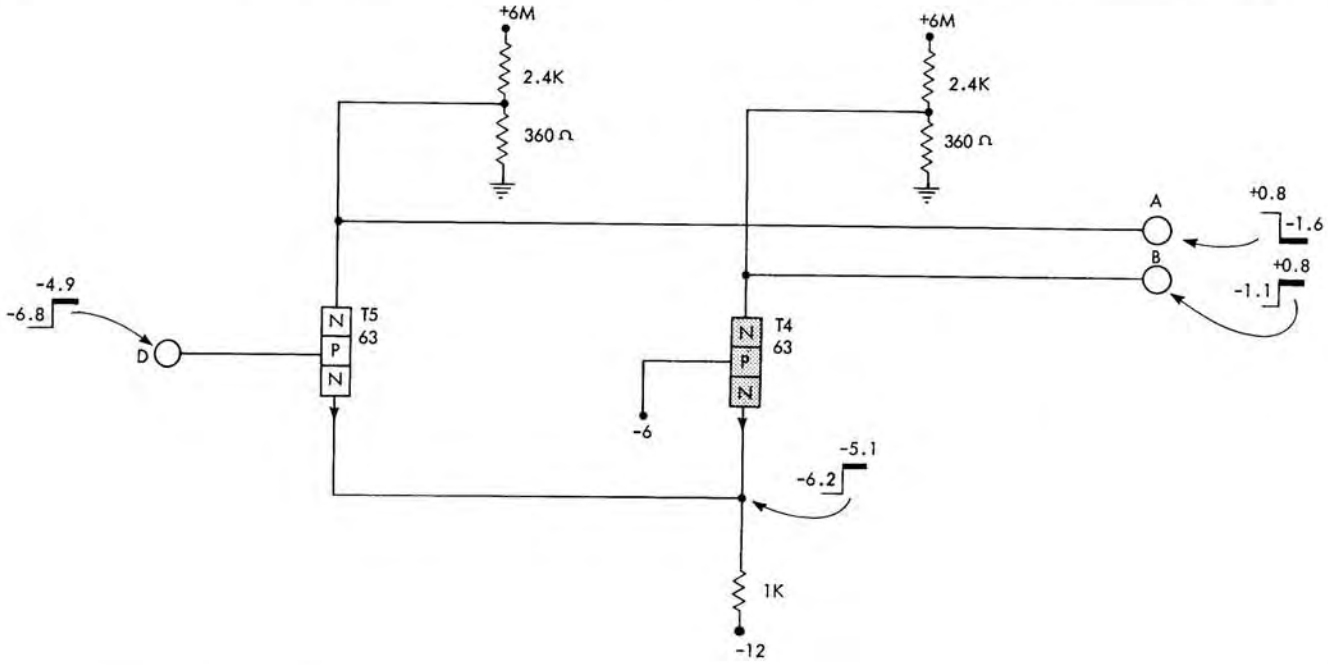
A typical line driver application is shown above. Assume a starting condition of T4 and T2 conducting and common emitter voltages of the transistors at –6.2 volts. A –P input at pin D holds T5 and T3 off. With T3 and T5 off, no current flows into their coupling load and gives a +N out-of-phase output. Conduction of about 19ma through T2 and T4 into the cable and their coupling network gives a –N in-phase output at this time.

When a +P input appears at pin D of the line driver, T5 and T3 are forward-biased on and T2 and T4 are reverse-biased off. Conduction of near 23ma into the out-of-phase coupling network now results in a –N output at pin A. With T2 and T4 off, the in-phase output increases to the +N level.

Application

When properly terminated, a maximum of four current-mode N bases can be driven by the in-phase or the out-of-phase outputs of this line driver. Back-panel wiring is required as noted above.





Card Code	Part No 37----	Cplg Network		Circuit Used as		Input Levels		In Ø Output		Out Ø Output		Ma Input			usec Delay Per		
		In Ø	Out Ø			Min.	Max.	Min.	Max.	Min.	Max.		In Ø	Out Ø	Block	100uu Load	Driven Base
ANZZ	1209	Yes	Yes	C	CA	-5.6 / -6.4	See driver for max Output Levels	+0.4 / -0.4	+1.2 / -2.5	+0.4 / -0.4	+1.2 / -3.0	Min.	4.82	5.31	.03	.02	.03
ANZY	1210	Yes	No	TC								Nom.	6.0	7.6	.06	.025	.035
ANZX	1211	No	Yes									Max.	7.3	10.2	.1	.03	.04
AN--	1212	No	No														

Current Mode P-to-N Converter

The P-to-N converter is a single-input logic block. It is fed by a P line and produces both an in-phase and out-of-phase output. For a −P line input, a −N in-phase output and a +N out-of-phase output results. It is used:

1. To translate from a P to an N line.
2. To obtain an N line inversion of the input sign, i.e., a +P to a −N or a −P to a +N.
3. As a current amplifier to drive other logic blocks.

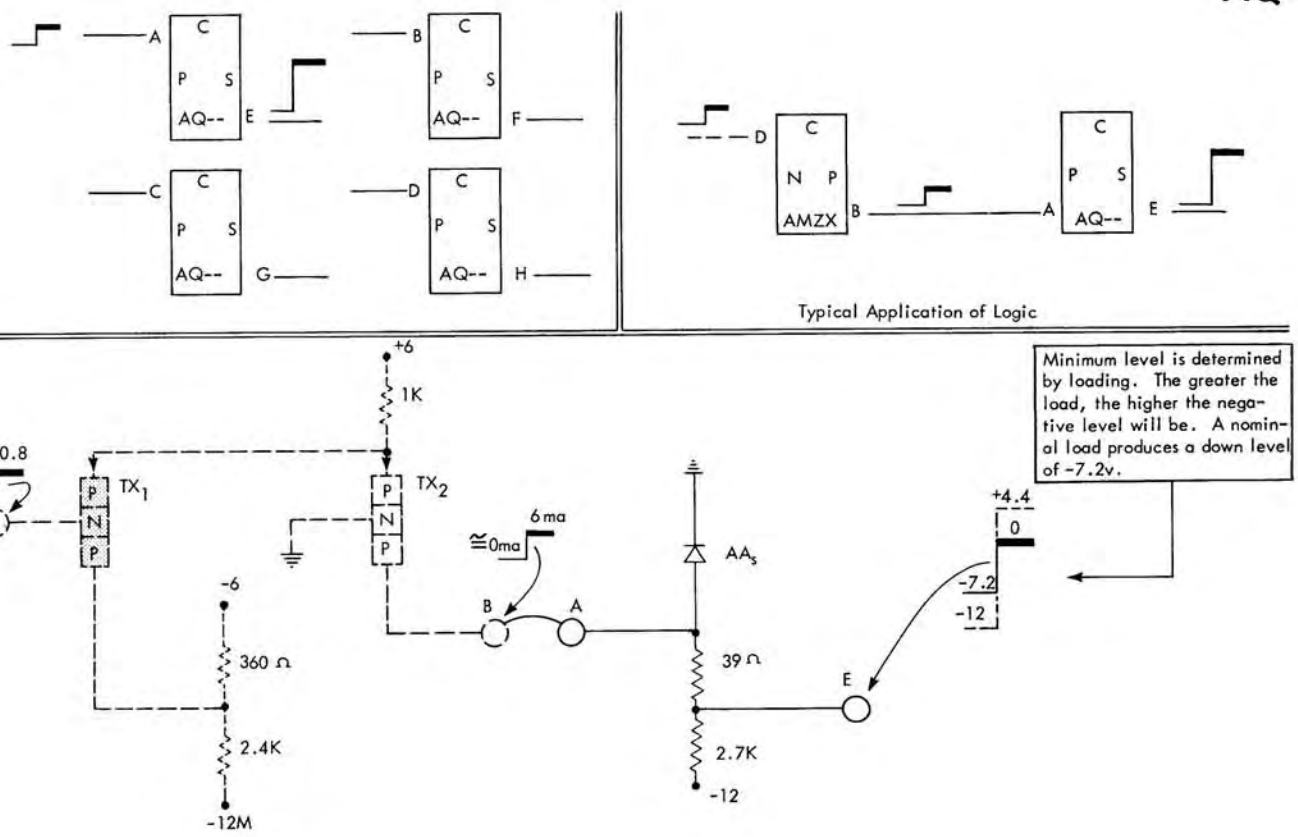
Circuit Description

This circuit configuration is that of a one-way OR circuit (the input transistor T5 has its base-to-emitter PN diode returned to a negative supply, −12v). Its emitter drives into a grounded base amplifier T4 referenced to −6v. With the input at the −P level shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −1.1v because of current flow (6ma) through T4 into its coupling network. Output A is at a +N level of 0.8v because of divider current through its coupling network.

When the input to T5 rises above −6v, the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output B rises to a +N level because of divider current through its coupling network and output A falls to a −N level of −1.6v because of current flow (7.6ma) through T5 into its coupling network.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases, cap codes ZX, ZY, and -- are used as required (see chart). This circuit is also used as a converter within a trigger (TC) and in DOT functions as a CA.



Card Code	Part No 37----	Circuit Use	Input Current		Output Levels Min.	Output Levels Max.	Max. Possible Loading (Pyramiding Factor)	
AQ--	1031	C			-0.2	+0.2	1	NPN Ctrl
			Min.	4.82			1	PNP Inverter
			Nom.	6.0	-6.6		2	PNP E.F.
			Max.	7.3		-12.5	3	Trigger Gates

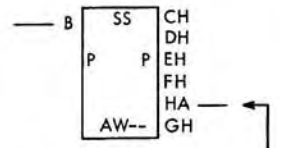
Current Mode to Voltage Mode Converter

This converter is used to translate from current-mode P levels to CTRL S levels. For a P line input it develops an in-phase S line output. It requires a current input and must be driven by the in-phase output of an N block and must be the only circuit connected to this output.

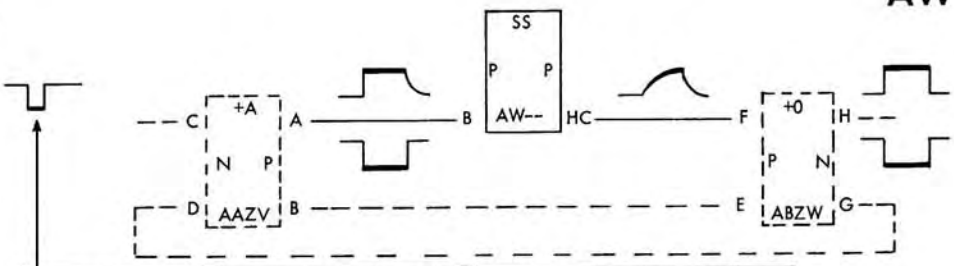
Circuit Description

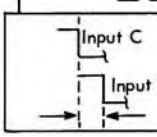
This circuit converts a 0 to 6ma input current to a −12v to 0v output signal. In the state shown, TX2 is reverse-biased and input current to the converter is close to zero. At this time the converter output will vary from −12v to −6.6v depending on the load tied to output E. This level would be −12v for an open circuit load and −6.6v for the maximum permissible.

When the input level to TX1 rises above ground, TX2 is forward-biased and, depending on its bias, will draw from 4.82ma to 7.3ma from the converter. A current drain of 4.82ma through the 2.7K resistor is large enough to raise output E above the 0v level. Output E does not rise above zero because the diode clamp becomes forward-biased and holds the output level at 0v. The 39 ohm resistor develops a −0.2v drop to compensate for the +0.2v diode drop. Such compensation places output E at zero volts instead of +0.2v. Once the diode is forward-biased it supplies any further increase in current demand to the transistor.

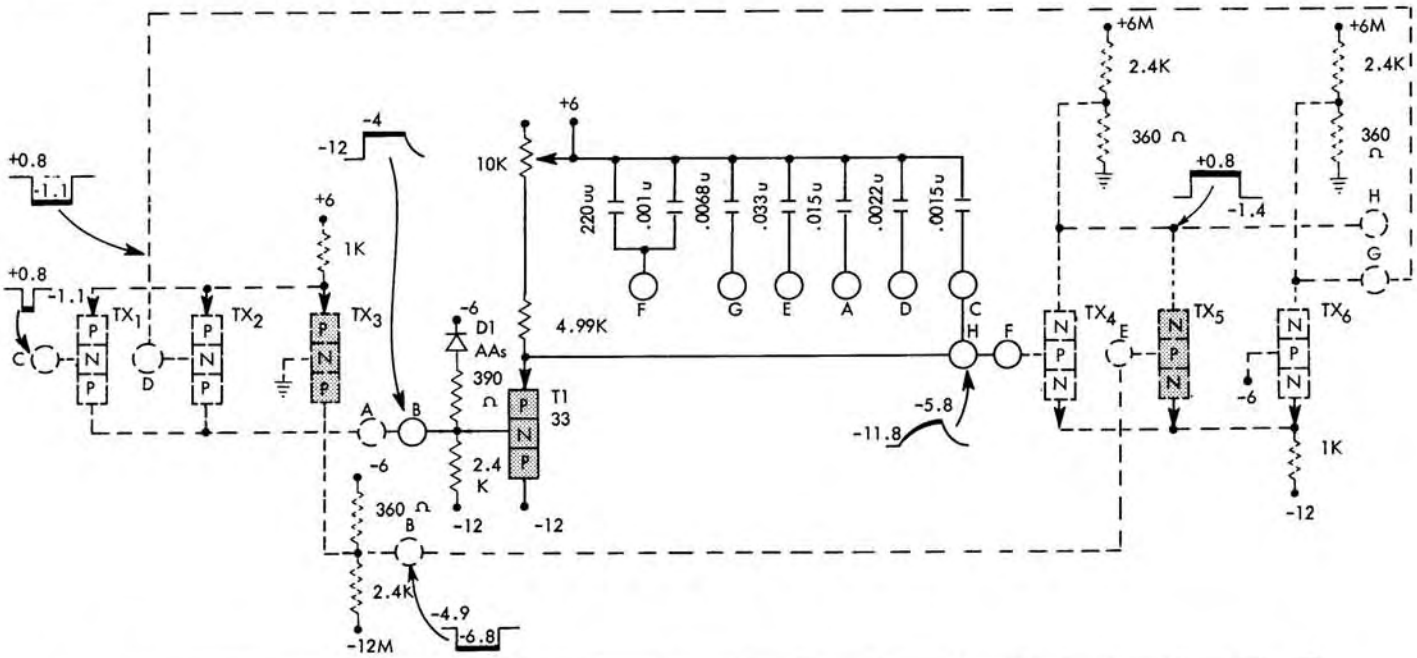


Many combinations of output pin use is possible. Specific jumpers connected to H alter the SS timing according to the chart below





The expanded time base illustrates that the fall at input C releases the AND circuit which starts the single shot timing. Input D is the OR circuit output coupled back to maintain the AND circuit off, until the single shot timing is complete



usec																
Timing	From	3.2	4.0	5.8	7.5	9.9	13	18	24	31	40	52	70	93	118	160
	To	4.2	5.4	7.8	9.8	13	17.5	24.5	32	42	53	69	94	118	160	215
Connect to Pin H		F	C	D	F,C	C,D	F,C D	G	G,D	C,D F,G	A	A,C D,F	A,C,D F,G	E	C,D,E F,G	A,C,D E,F,G

Card Code	Part No. 37----	Circuit Used as	Min Input Duration	Repetition Rate	Max Variation of Pulse Width
AW--	1039	SS	0.5 usec	A recovery time of 8% of T_* results in an output pulse of at least 95% of T_* T_* = Specific SS timing used	± 15%, six months after initial setting (assuming all worst case conditions of temperature, components, power supplies, etc.)

urrent Mode, 3.2 to 215 Microsecond Universal Single-Shot

he AW - - single shot (ss) card is an RC timing network. he required input for this network is supplied by a ansistor amplifier on the card. The circuit is triggered y a positive input signal. Once triggered, it develops an -phase exponential output waveform as shown. This ard is used with a standard AND and OR block to develop square wave output pulse (see logic application drawg). The width of the output square wave is determined y the AW - - card.

Signal information and flow of this multicard circuit as follows. In the inactive state, AND inputs C and D re up, the input and output of the ss are down, and OR put E is up.

To make the circuit active (start the single-shot) a egative signal to AND input C is required. This negative put drops out the AND circuit and its in-phase output alls. Both inputs to the OR circuit are now negative so t drops out; its in-phase output falls and its out-of-phase utput rises. The OR circuit is the output stage of this ulticard circuit, so at this time the leading edge of the quare wave signals desired are recognized at outputs G nd H. These signals are terminated (single-shot time is nded) when OR input F reaches a +P level. Input F tarted rising as shown when the AND circuit first dropped ut because AND output A developed a positive shift and icked the ss.

OR output G is coupled back to AND input D so the ND circuit is held off for at least the duration of the ingle-shot timing. This arrangement insures that the ingle-shot timing is not affected by input C if input C ises before the single-shot timing is completed. When the ingle-shot signal is ended and input C is again positive, he AND circuit is picked. AND output B holds the OR ircuit picked while AND output A drops out the ss. The ignal decay of AND output A is caused by the ss input ircuitry.

Because the AW - - card is a universal timing card (3.2 o 215 microseconds), it is necessary to do the following o obtain a specific timing:

1. Connect back panel wiring as shown in the chart to obtain a specific timing range.
2. Adjust the 10K potentiometer located on the card for the exact timing desired.

Circuit Description

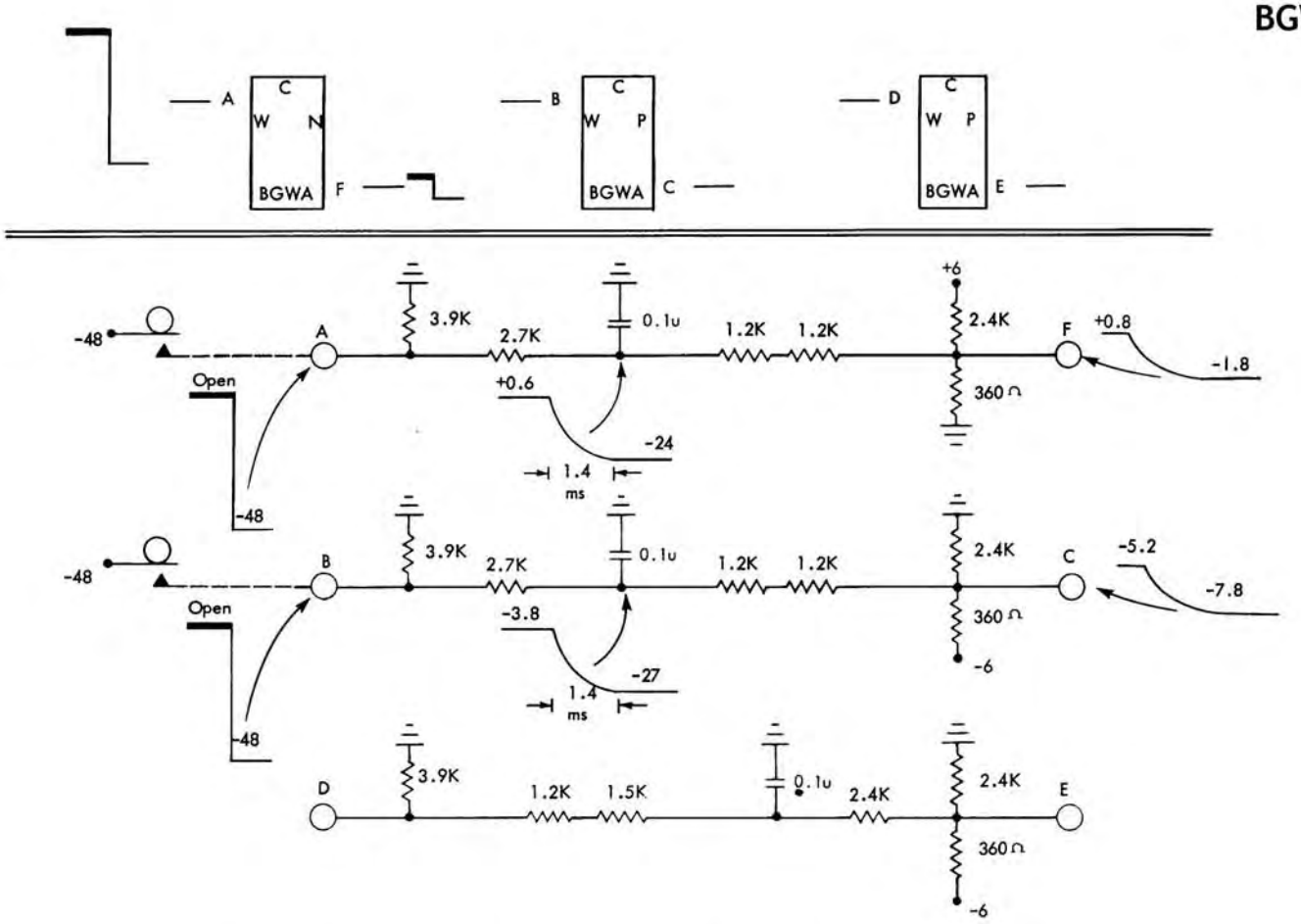
As shown, input C and D are +N and TX3 is forward-biased. Current flow out of the 360 ohm, 2.4K coupling network through TX3 to +6v establishes AND output B at a +P level of −4.9v which forward-biases TX5. Current flow from −12v through TX5 into its coupling network establishes OR output H at a −N level of −1.4v. OR output G is at a +N level of +0.8v because of divider current through its coupling network. Input current to ss input B is zero so the base of T1 is at −12v and T1 is forward-biased. Current flows from −12v through T1, the 4.99K resistor, and the 10K potentiometer to +6v. The emitter of T1 clamps to its base potential and the .0015μfd capacitor develops a 17.8v charge.

When input C falls, TX1 is forward biased and TX3 is cut off. AND output B falls to a −P level of −6.8v which forward biases TX6 and cuts off TX5. With TX5 cut off and TX6 conducting, output H rises to a +N level and output G falls to a −N level. Output G is coupled back to AND input D so TX2 is forward-biased with TX1. Current for TX1 and TX2 flows from −12v through the 2.4K resistor, TX1, and TX2 to +6v. When the voltage drop across the 2.4K resistor is greater than 6v, D1 is forward-biased, current flows from −6v through D1, TX1 and TX2 to +6v, and the base of T1 reaches a −4v level. T1 is reverse-biased and the .0015μfd capacitor starts to discharge through the 4.99K resistor and 10K potentiometer. If input C were of shorter duration than the single-shot timing, TX1 would cut off. Tx3 is held cut off at this time by TX2 so the rise of input C has no effect.

When the base of TX4 rises above −6v, TX4 is forward-biased and TX6 is cut off. Output G rises to a +N level and output H falls to a −N level. The rising signal to input D forward-biases TX3 and reverse-biases TX2. Current flow through TX3 causes output B to rise and forward bias TX5 and cut off TX6. With TX2 cut off, T1 is again forward-biased and T1 supplies input current to the .0015μfd. capacitor to again charge it to 17.8v.

Had input C been of greater duration than output G, TX2 would have cut off when output G rose, but TX3 would be held off by TX1.

The amount of capacitance wired to ss output H determines the timing range (from and to timing) of the ss. A specific time within the range is obtained by adjusting the 10K potentiometer located on card AW - -.



Card Code	Part No.
BGWA	371430

Note 1: Although the integrator is designed for a -48v input, other sources are also used. When sources other than -48v are used, the line notation W is not used.
2. The use of two series resistors, such as 1.2K and 1.2K, instead of 2.4K has no electrical significance. It is so used only to simplify packaging problems which result because of the land pattern layout on the card.

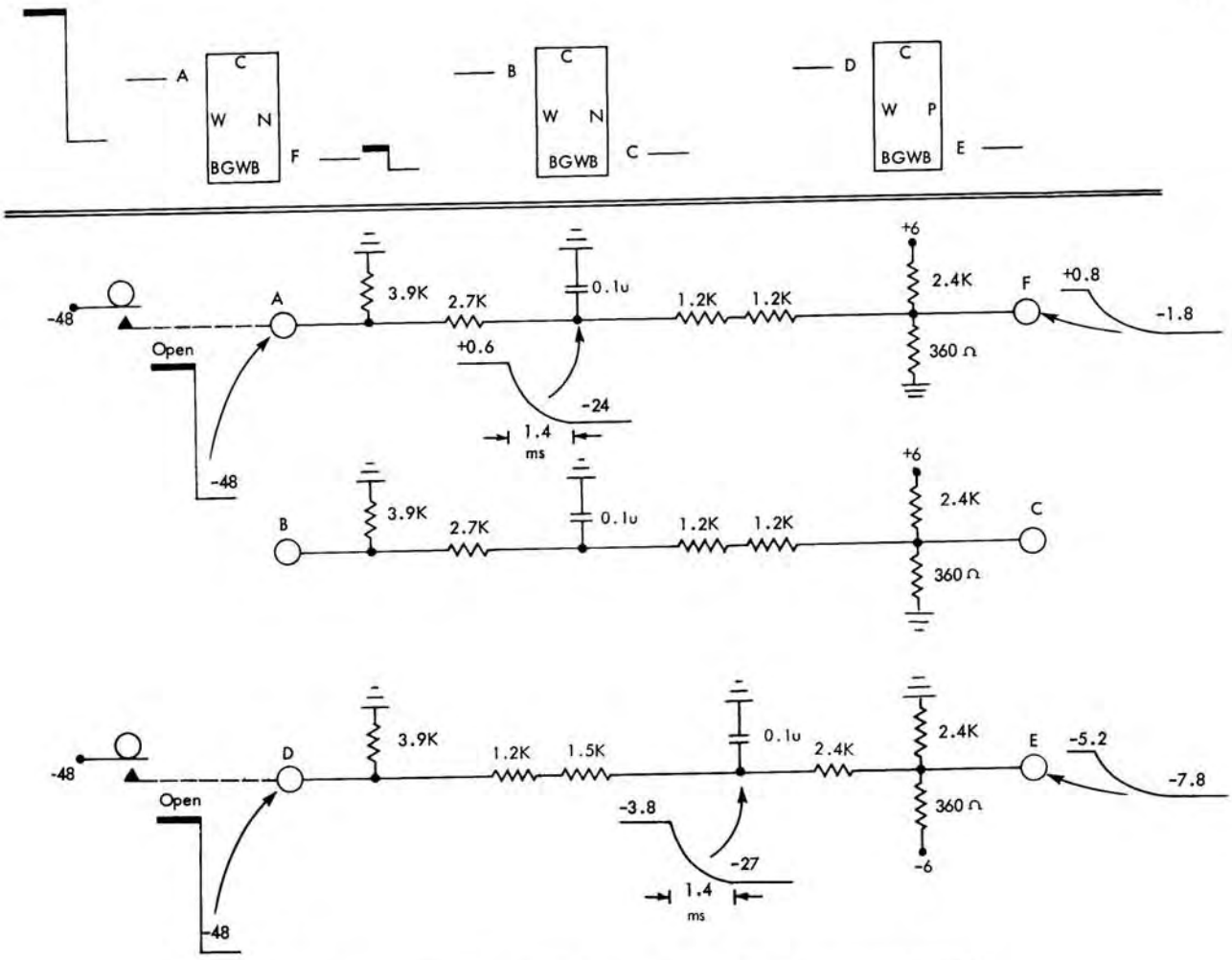
Current Mode W-to-N and W-to-P Integrators

The BGWA card has three integrators that accept a W line input. One of these circuits provides an in-phase N line output whereas the other two provide an in-phase P line output. The purpose of this circuit is to develop current-mode output levels that are free of the noise and bounce generally found on CB or relay lines.

Circuit Description

When the input to A is open, the N line output is at +0.8v because of divider current through the 360 ohm, 2.4K coupling network, and the .1μfd capacitor is charged to 0.6v. Closure of the CB puts input A at −48v, and the capacitor starts to charge to its −24v level as shown. Output F falls along with the capacitor charge until in the static state it reaches −1.8v because of approximately 8ma of current flow from −48v into the coupling network. The capacitor and the 2.7K resistor have a sufficiently long time constant so that relay bounce and line noise are filtered by the network and do not appear at output F. The 3.9K CB load resistor lowers the input impedance from approximately 5.4K to 2.3K. This low impedance draws 21ma of CB current, which is sufficient to break down an oxide film formation.

When the input to B is open, the P line output is at −5.2v because of divider current through the coupling network, and the capacitor is charged to −3.8v. Closure of the CB puts input B at −48v, and the capacitor starts to charge to its −27v level as shown. Output C falls along with the capacitor charge until in the static state it reaches −7.8v because of approximately 8ma of current flow from −48v into the coupling network.



Note 1. Although the integrator is designed for a -48v input, other sources are also used. When sources other than -48v are used, the line notation W is not used.

2. The use of two series resistors, such as 1.2K and 1.2 K, instead of 2.4K has no electrical significance. It is so used only to simplify packaging problems which result because of the land pattern layout on the card.

Card Code	Part No.
BGWB	371429

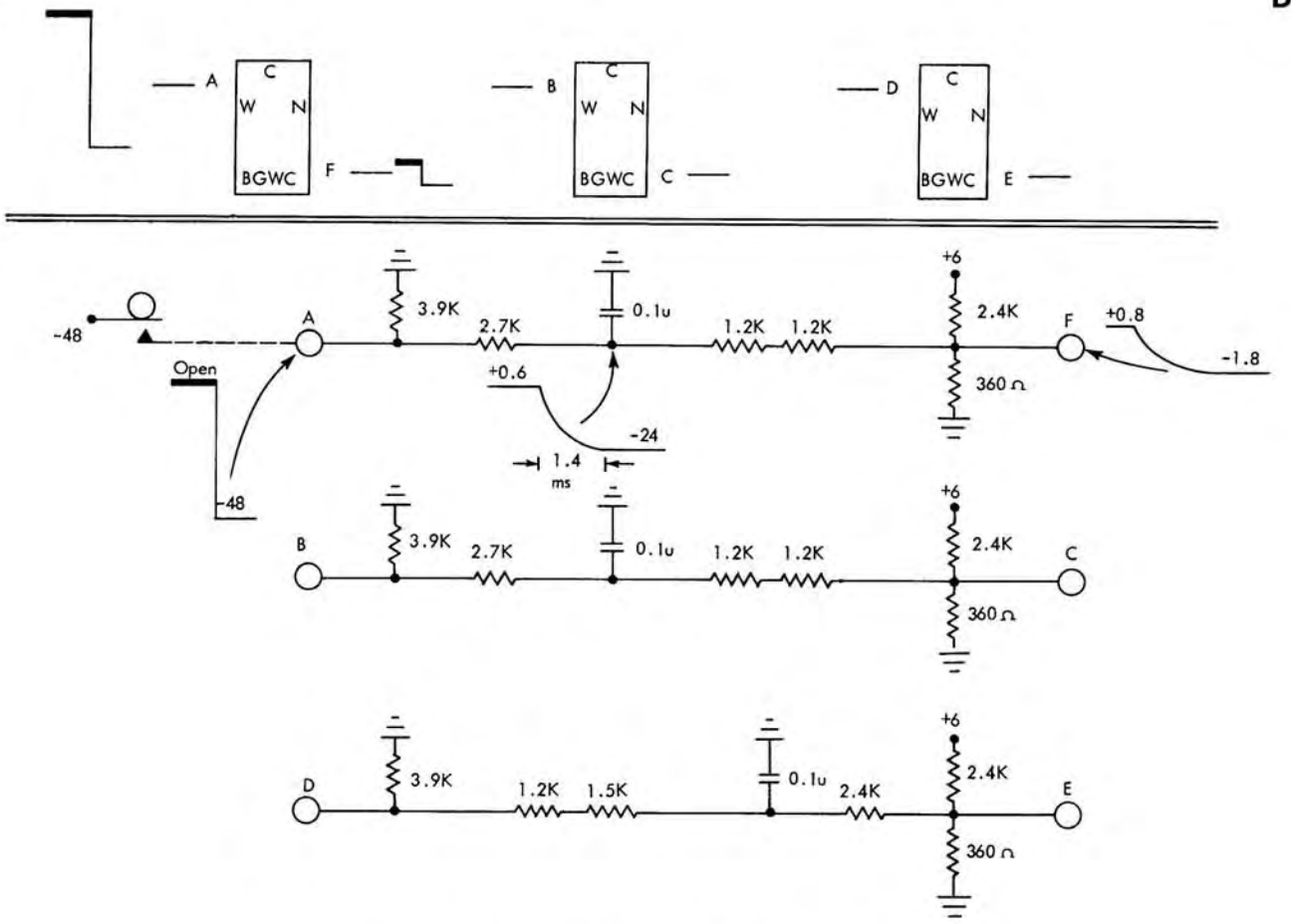
Current Mode W-to-N and W-to-P Integrators

The BGWB card has three integrators that accept a W line input. One of these circuits provides an in-phase P line output whereas the other two provide an in-phase N line output. The purpose of this circuit is to develop current-mode output levels that are free of the noise and bounce generally found on CB or relay lines.

Circuit Description

When the input to A is open, the N line output is at +0.8v because of divider current through the 360 ohm, 2.4K coupling network, and the .1μfd capacitor is charged to 0.6v. Closure of the CB puts input A at −48v, and the capacitor starts to charge to its −24v level as shown. Output F falls along with the capacitor charge until in the static state it reaches −1.8v because of approximately 8ma of current flow from −48v into the coupling network. The capacitor and the 2.7K resistor have a sufficiently long time constant so that relay bounce and line noise are filtered by the network and do not appear at output F. The 3.9K CB load resistor lowers the input impedance from approximately 5.4K to 2.3K. This low impedance draws 21ma of CB current, which is sufficient to break down an oxide film formation.

When the input to D is open, the P line output is at −5.2v because of divider current through the coupling network, and the capacitor is charged to 3.8v. Closure of the CB puts input B at −48v, and the capacitor starts to charge to its −27v level as shown. Output E falls along with the capacitor charge until in the static state it reaches −7.8v because of approximately 8ma of current flow from −48v into the coupling network.



Note 1. Although the integrator is designed for a -48v input, other sources are also used. When sources other than -48v are used, the line notation W is not used.

2. The use of two series resistors such as 1.2K and 1.2K instead of 2.4K has no electrical significance. It is so used only to simplify packaging problems which result because of the land pattern layout on the card.

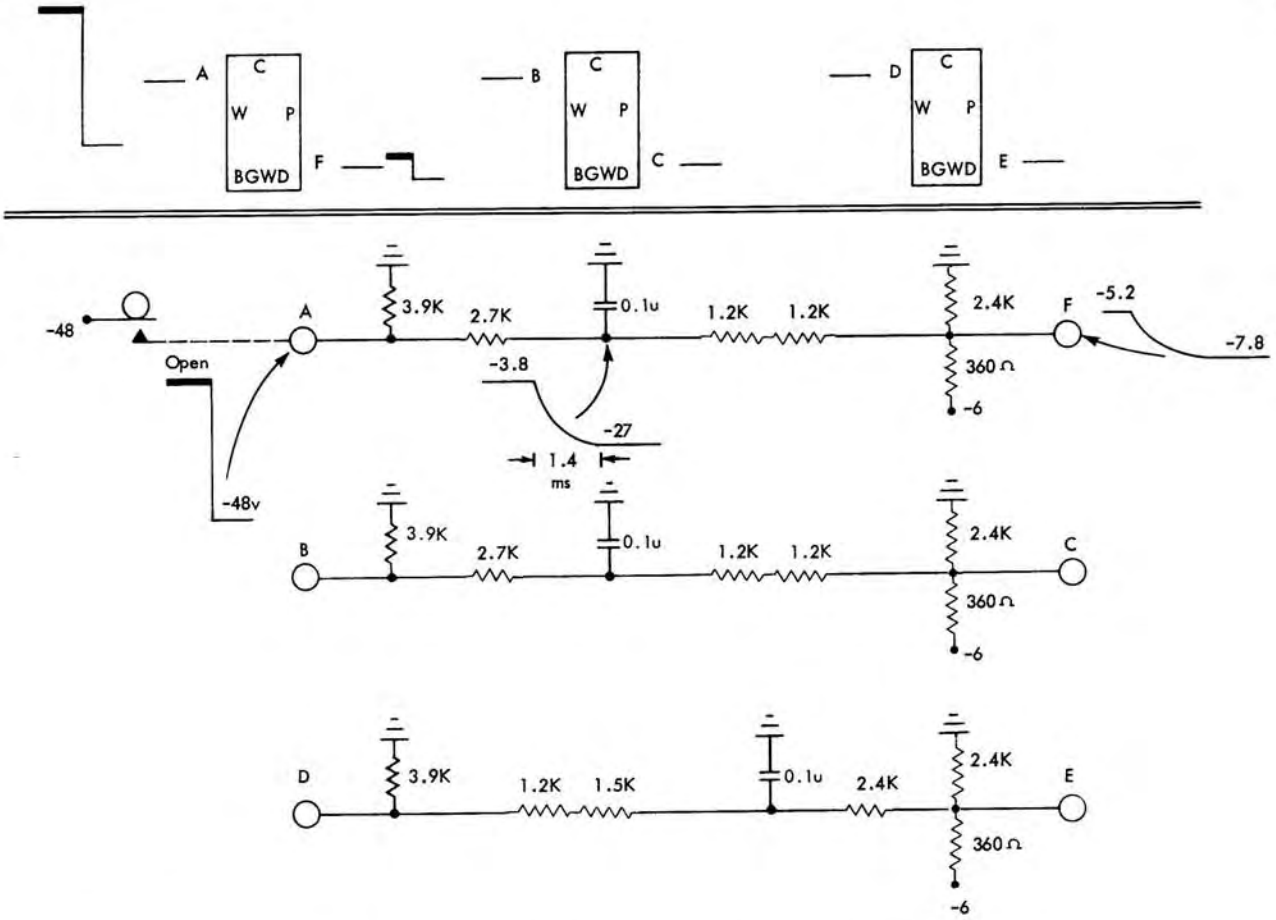
Card Code	Part No
BGWC	371428

Current Mode W-to-N Integrators

The BGWC card has three integrators that accept a W line input. Each circuit provides an in-phase N line output. The purpose of this circuit is to develop current-mode output levels that are free of the noise and bounce generally found on CB or relay lines.

Circuit Description

When the input to A is open, the N line output is at +0.8v because of divider current through the 360 ohm, 2.4K coupling network, and the .1μfd capacitor is charged to 0.6v. Closure of the CB puts input A at −48v, and the capacitor starts to charge to its −24v level as shown. Output F falls along with the capacitor charge until in the static state it reaches −1.8v because of approximately 8ma of current flow from −48v into the coupling network. The capacitor and the 2.7K resistor have a sufficiently long time constant so that relay bounce and line noise are filtered by the network and do not appear at output F. The 3.9K CB load resistor lowers the input impedance from approximately 5.4K to 2.3K. This low impedance draws 21ma of CB current, which is sufficient to break down an oxide film formation.



Card Code	Part No
BGWD	371427

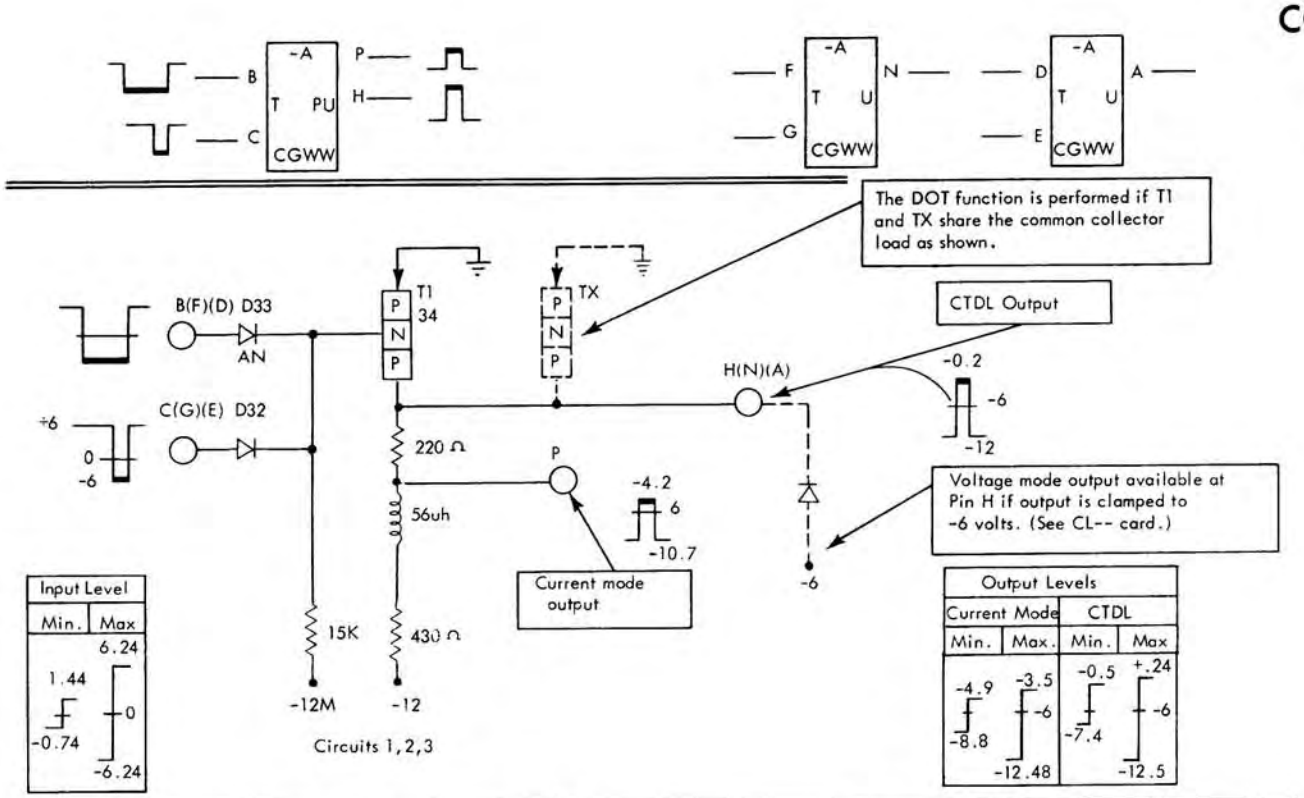
Note 1. Although the integrator is designed for a -48v input, other sources are also used. When sources other than -48v are used, the line notation W is not used.
2. The use of two series resistors, such as 1.2K and 1.2K, instead of 2.4K has no electrical significance. It is so used only to simplify packaging problems which result because of the land pattern layout on the card.

Current Mode W-to-P Integrators

The BGWD card has three integrators. Each accepts a W line input and develops an in-phase P line output. The purpose of this circuit is to develop current-mode output levels that are free of the noise and bounce generally found on CB or relay lines.

Circuit Description

When the input to A is open, the P line output is at −5.2v because of divider current through the 360 ohm, 2.4K coupling network, and the .1μfd capacitor is charged to −3.8v. Closure of the CB puts input A at −48v, and the capacitor starts to charge to its −27v level as shown. Output F falls along with the capacitor charge until in the static state it reaches −7.8v because of approximately 8ma of current flow from −48v into the coupling network. The capacitor and the 2.7K resistor have a sufficiently long time constant so that relay bounce and line noise are filtered by the network and do not appear at output F. The 3.9K CB load resistor lowers the input impedance from approximately 5.4K to 2.3K. This low impedance draws 21ma of CB current, which is sufficient to break-down an oxide film formation.



Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Circuit 1	2	3	Delays		Per	Basic Block	Par'lel C'lector	CM Base	Diode Input	100 uufd	Circuit Use	
CGWW	1251	No	1	Yes	Yes	Yes	Turn On		Min.	.20	.000	.000	.000	.02	+O	-A
CGVW	1261	No	1	Yes	Yes	No			Max.	.70	.007	.015	.020	.05	+OA	-AO
CGVV	1262	No	1	Yes	No	No	Turn Off		Min.	.06	.004	.005	.000	.03	+CA	-CO
CG--	1263	No	No	No	No	No			Max	.18	.010	.020	.005	.06	-TA	-TC
															-TAO	-TCO

CTDL Two-Way —AND

The CGWW card consists of three two-way PNP logic circuits. Each circuit on the card normally performs a —AND and INVERT logical function and translates a T input to an out-of-phase U output. All three circuits on the card have internal collector loads that provide CTDL outputs at pins H, N, and A and a suitable current-mode output at pin P.

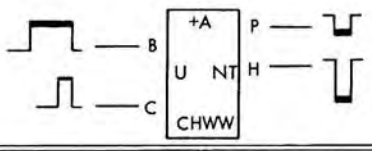
Circuit Description (Circuit 1)

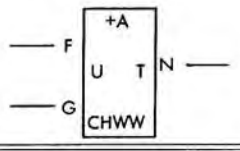
The —AND function is performed by the diode mix of D33 and D32 returned to —12 volts, and the INVERT function is accomplished by the transistor circuit. Coincidence of —T levels is required at input pins B and C to forward-bias T1 into saturation. With T1 on, the output at pin H approaches 0v (minus the small voltage drop across the transistor). When either of the input signals increases to +6v, T1 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance, and the output at pin H decreases to —12v (No Load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

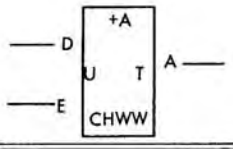
Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

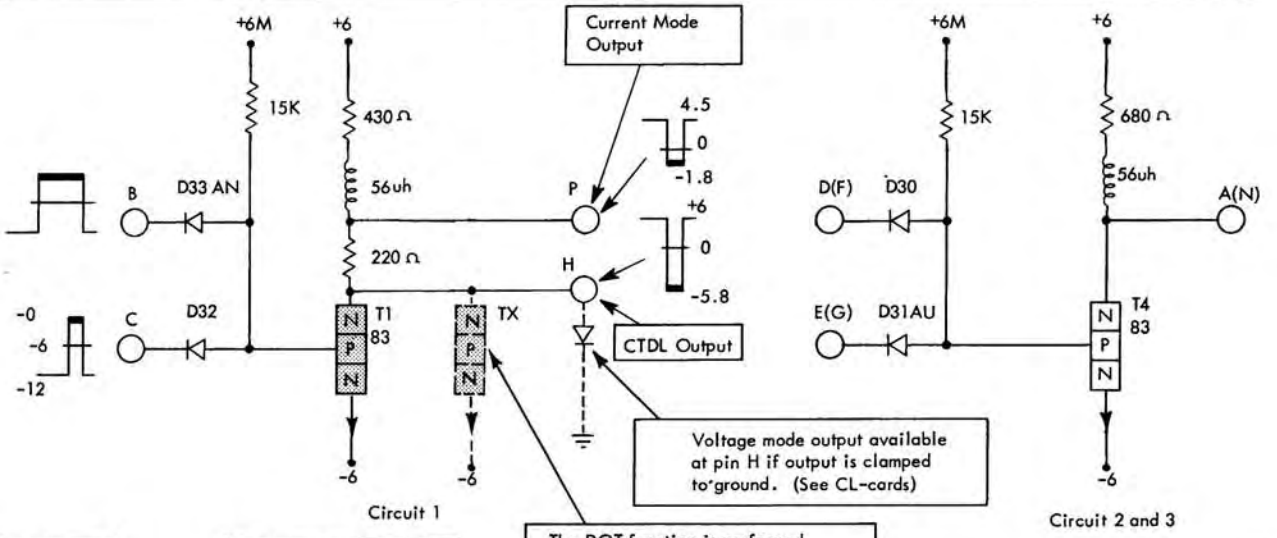
Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart, Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.









Input Levels	
Min.	Max.
-5.3 to -7.4	0.24 to -12.48

Output Levels			
Current Mode		CTDL	
Min.	Max.	Min.	Max.
+2.8 to -1.1	6.3 to -2.5	1.44 to -5.5	6.3 to -6.3

Card Code	Part No 37----	E'tender Input Circuit	CM Output Circuit	Collector Loading Ckt 1	Ckt 2	Ckt 3	Delays Per		Basic Block	Par'lel C'ltor	CM Base	Diode Input	100 uufd	Circuit Use	
CHWW	1252	No	1	Yes	Yes	Yes	Turn On	Min.	.18	.00	.00	.00	.02	+A	-O
CHVW	1264	No	1	Yes	Yes	No		Max.	.52	.007	.02	.02	.05	+AO	-AO
CHVV	1265	No	1	Yes	No	No	Turn Off	Min.	.05	.004	.005	.000	.03	+CO	-CA
CH--	1266	No	No	No	No	No		Max.	.12	.01	.02	.005	.06	+C	+TC
														+TCO	+TAO

CTDL Two-Way +AND

The CHWW card consists of three two-way NPN logic circuits. Each circuit on the card normally performs a +AND and INVERT logical function that translates a U input to an out-of-phase T output. All three circuits on the card have internal collector loads that provide CTDL outputs at pins H, A, and N and a suitable current-mode output at pin P.

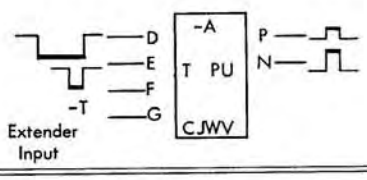
Circuit Description (Circuit 1)

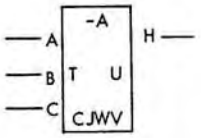
The +AND function is performed by the diode switch of D33 and D32 returned to +6v, and the INVERT function is accomplished by the transistor circuit. Coincidence of +U levels is required at input pins B and C to forward-bias T1 into saturation. With T1 on, the output at pin H nears −6v (minus the small voltage drop across the transistor). When either of the input signals drops to −12v, T1 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance, and the output at pin H increases toward +6v (No Load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current mode output.

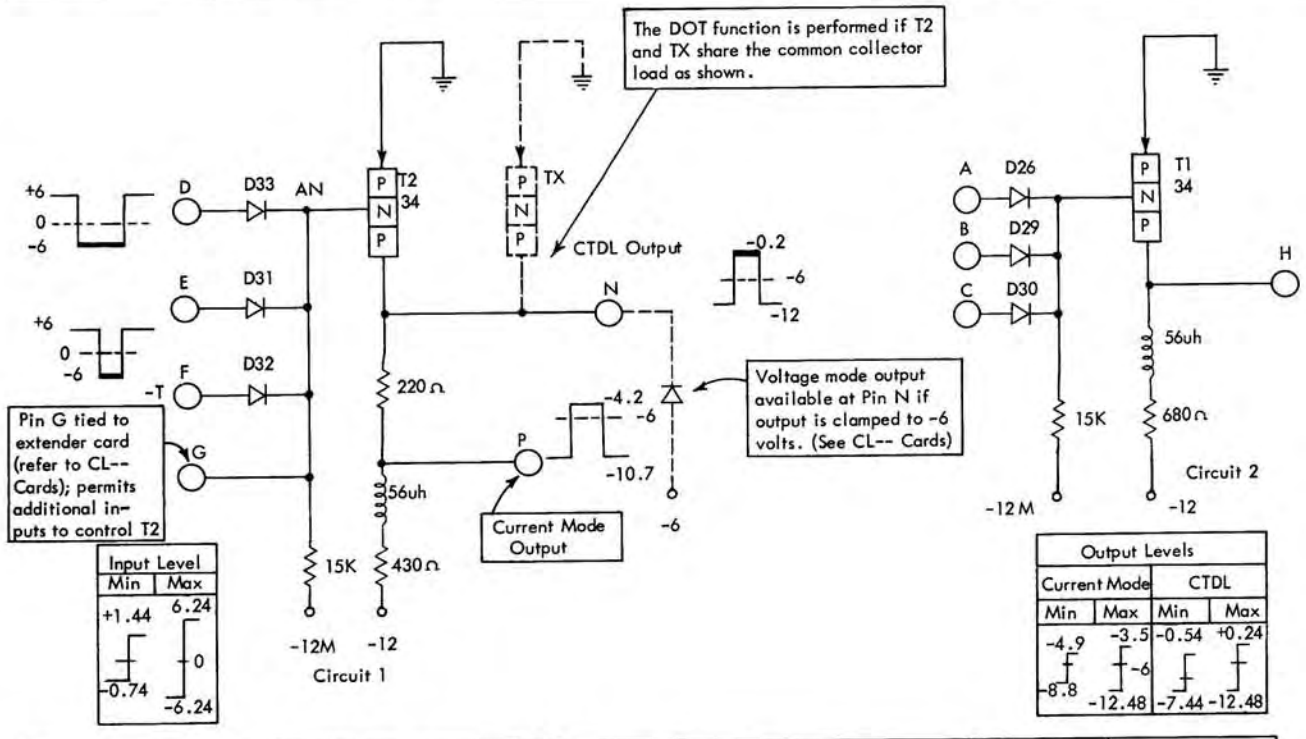
Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.







Card Code	Part No 37----	Extender Inputs	CM Output	Collector Loading		Delays		Basic Block (usec)	Parallel Collector (usec)	CM Base (usec)	Diode Input (usec)	100 uufd (usec)	Circuit Use	
		Circuit	Circuit	Ckt 1	Ckt 2									
CJWV	1253	1	1	Yes	Yes	Turn On	Min.	0.20	0.00	0.00	0.00	0.02	+O	-A
							Max.	0.70	0.007	0.015	0.02	0.05	+OA	-AO
CJVU	1267	1	1	Yes	No	Turn Off	Min.	0.06	0.004	0.005	0.00	0.03	+CA	-CO
CJ--	1268	1	No	No	No		Max.	0.18	0.01	0.02	0.005	0.06	-TA	-TC
													-TCO	+C

CTDL Three-Way —AND

The CJWV card consists of two three-way PNP logic circuits. Each circuit on the card normally performs a —AND and INVERT logical function and translates a T input to an out-of-phase U output. Both circuits on the card have internal collector loads that provide CTDL outputs at pins N and H and a suitable current-mode output at pin P. Extender pin G permits additional inputs to control circuit 1.

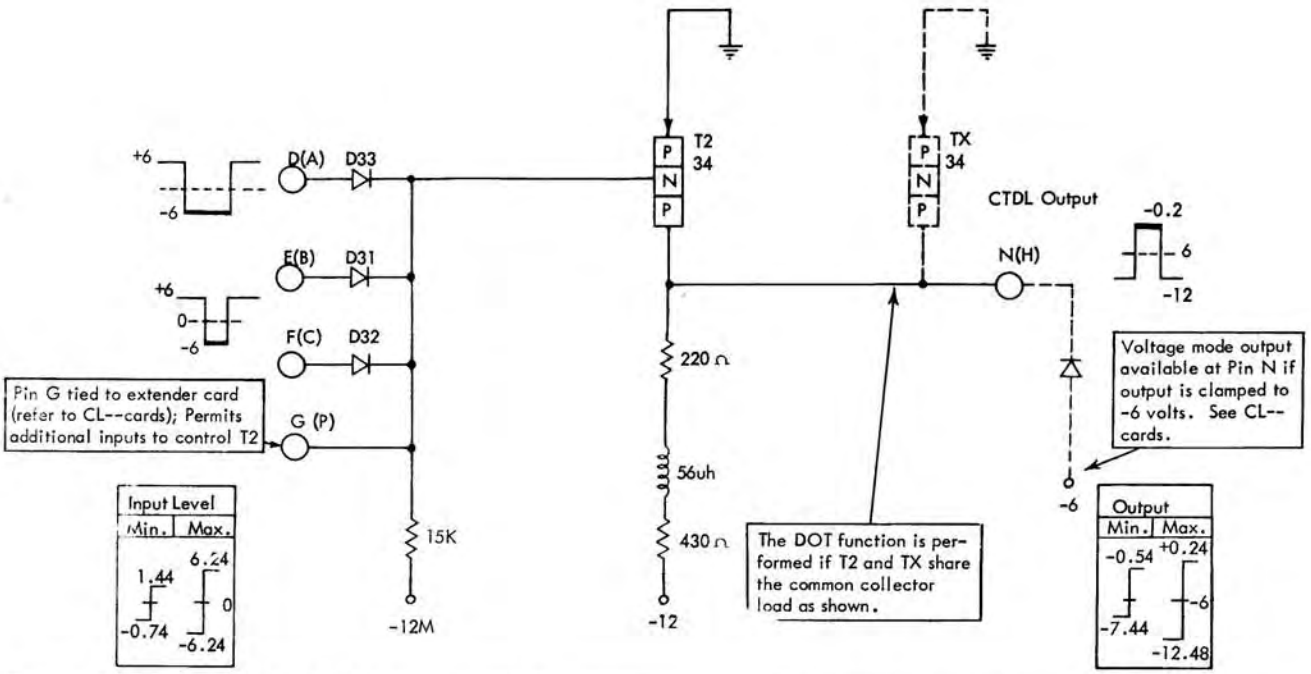
Circuit Description (Circuit 1)

The —AND function is performed by the diode mix of D33, D31 and D32 returned to —12v, and the INVERT function is accomplished by the transistor circuit. Coincidence of —T levels is required at input pins D, E, and F to forward-bias T2 into saturation. With T2 on, the output at pin N nears 0v (minus the small voltage drop across the transistor). When either of the input signals increases to +6v, T2 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin N decreases to —12v (No Load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.



Card Code	Part No. 37----	Extender Inputs Circuit	CM Output Circuit	Collector Loading Ckt1	Collector Loading Ckt 2	Delay (usec) Per		Basic Block	Parallel Collector	CM Base	Diode	100 uufd	Circuit Use
CJYC	1071	1,2	No	Yes	Yes	Turn On	Min.	.20	.00	.00	.00	.02	+O +OA -A -AO -TA
							Max.	.70	.007	.02	.0?	.05	
						Turn Off	Min.	.06	.004	.005	.00	.03	
							Max.	.18	.01	.02	.005	.06	

CTDL Three-Way —AND Extendible Inputs

The CJYC card consists of two three-way PNP logic circuits. Each circuit on the card normally performs a —AND and INVERT logical function and translates a T input to an out-of-phase U output. Both circuits on the card have internal collector loads that provide CTDL outputs at pins N and H. Extender pins G and P permit additional inputs to control circuits 1 and 2.

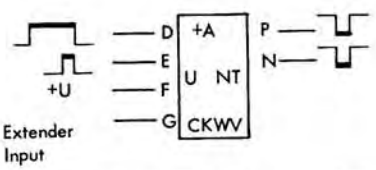
Circuit Description

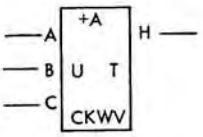
The —AND function is performed by the diode mix of D33, D31, and D32 returned to —12v, and the INVERT function is accomplished by the transistor circuit. Coincidence of —T levels is required at input pins D, E, and F to forward-bias T2 into saturation. With T2 on, the output at pin N nears 0v (minus the small voltage drop across the transistor). When any of the input signals increases to +6v, T2 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin H decreases to —12v (No Load).

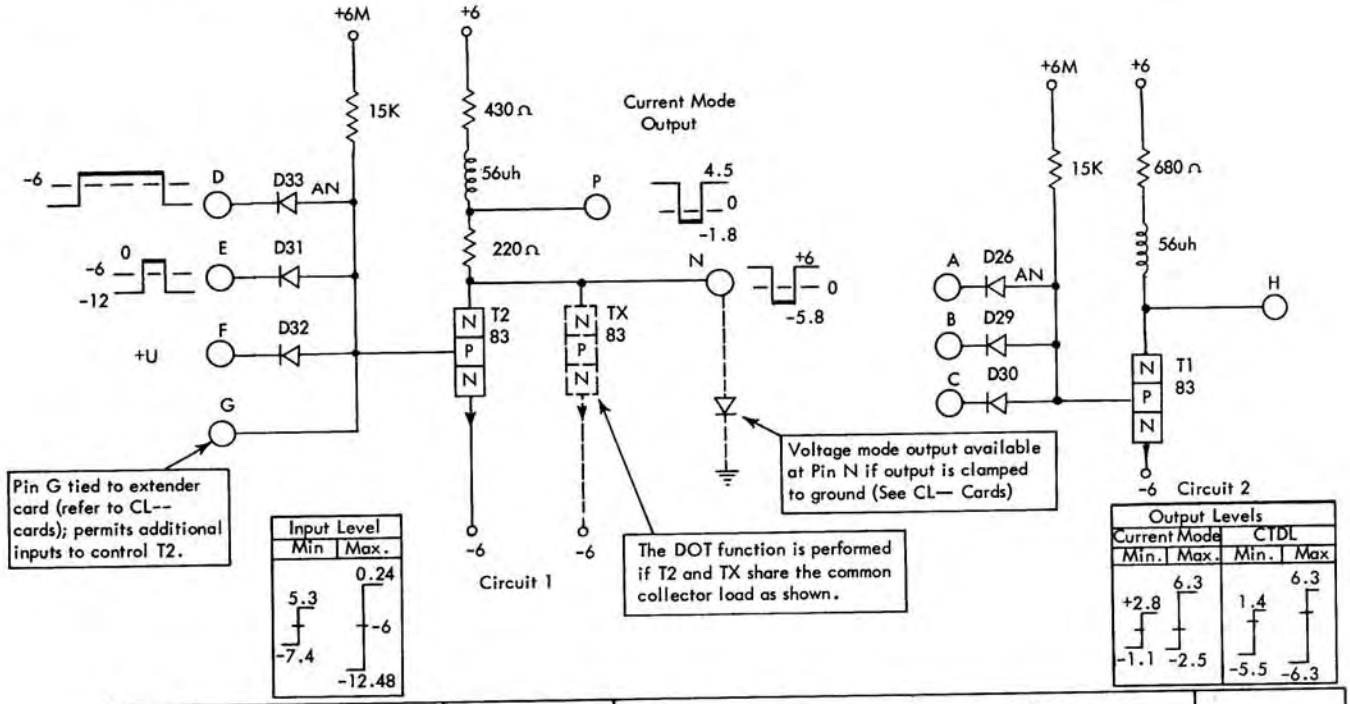
Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.







Card Code	Part No 37----	Extender Input	CM Output	Collector Loading Circuit		Delays	Per	Basic Block	Par'lel Collector	CM Base	Diode Input	100 uufd	Circuit Use	
		Circuit	Circuit	1	2									
CKWV	1254	1	1	Yes	Yes	Turn On	Min.	.18	.00	.00	.00	.02	+A	-O
							Max.	.52	.007	.02	.02	.05	+AO	-OA
CKVU	1269	1	1	Yes	No	Turn Off	Min.	.05	.004	.005	.000	.03	+CA	+C
CK--	1270	1	No	No	No		Max.	.12	.01	.02	.005	.06	+TAO	-TCO
													+TA	+TC

(usec)

CTDL Three-Way +AND

The CKWV card consists of two three-way NPN logic circuits. Each circuit on the card normally performs a +AND and INVERT logical function and translates a U input to an out-of-phase T output. Both circuits on the card have internal collector loads that provide CTDL outputs at pins N and H and a suitable current-mode output at pin P. Extender pin G permits additional inputs to control circuit 1.

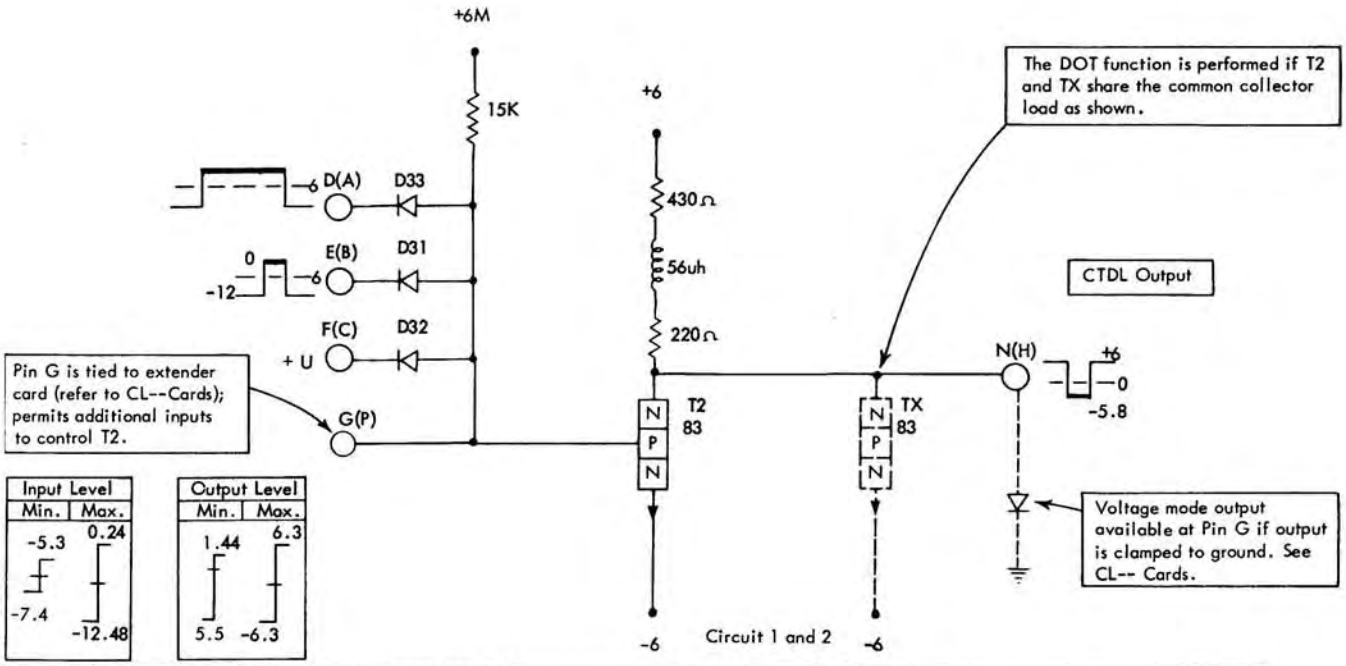
Circuit Description (Circuit 1)

The +AND function is performed by the diode switch of D33, D31, and D32 returned to +6v, and the INVERT function is accomplished by the transistor circuit. Coincidence of +U levels is required at input pins D, E, and F to forward-bias T2 into saturation. With T2 on, the output at pin N nears −6v (minus the small voltage drop across the transistor). When either of the input signals drops to −12v, T2 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a faster response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin N increases to +6v (No Load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading conditions for the different cap connections in this group of cards are noted above. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.



Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Circuit 1	Collector Loading Circuit 2	Delays	Per	Basic Block (usec)	Par'lel C'lector (usec)	CM Base (usec)	Diode Input (usec)	100 uufd (usec)	Circuit Use
CKYC	1071	1,2	No	Yes	Yes	Turn On	Min.	.18	.0000	.00	.00	.02	+A
							Max.	.52	.007	.02	.02	.05	+AO
						Turn Off	Min.	.05	.001	.005	.000	.03	+TA
							Max.	.12	.010	.02	.005	.06	-O -OA

CTDL Three-way +AND Extendible Inputs

The CKYC card consists of two three-way NPN logic circuits. Each circuit on the card performs a +AND and INVERT logical function that translates a U input to an out-of-phase T output. Internal collector loading to each circuit provides CTDL outputs at pins N and H. Extender pins G and P permit additional inputs to control circuits 1 and 2.

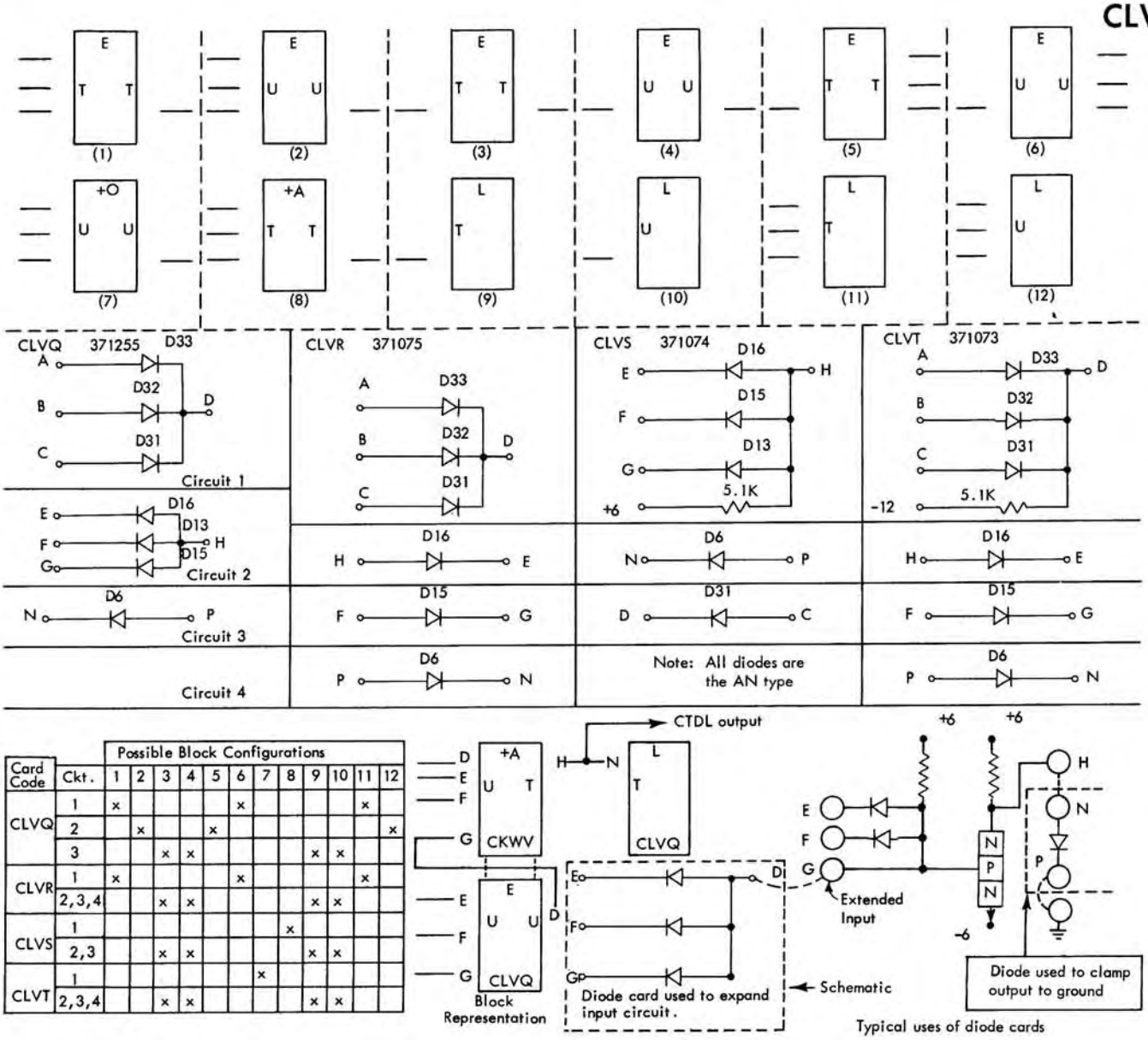
Circuit Description

The +AND function is performed by the diode switch of D33, D31, and D32 returned to +6v, and the INVERT function is accomplished by the transistor circuit. Coincidence of +U levels is required at input pins D, E, and F to forward-bias T2 into saturation. With T2 on, the output at pin N nears −6v (minus the small voltage drop across the transistor). When any of the input signals drops to −12v, T2 is turned off. The low forward impedance of the conducting logic diode rapidly removes the excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a faster response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin N increases to +6v. (No Load).

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Logical functions performed by this circuit are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from this circuit as noted on the schematic.



CTDL Extender and Limiter Diode Cards

This group of SMS cards contains various diode configurations used to expand the number of inputs to CTDL logic blocks, perform diode logic (AND-OR functions), or to limit voltage levels.

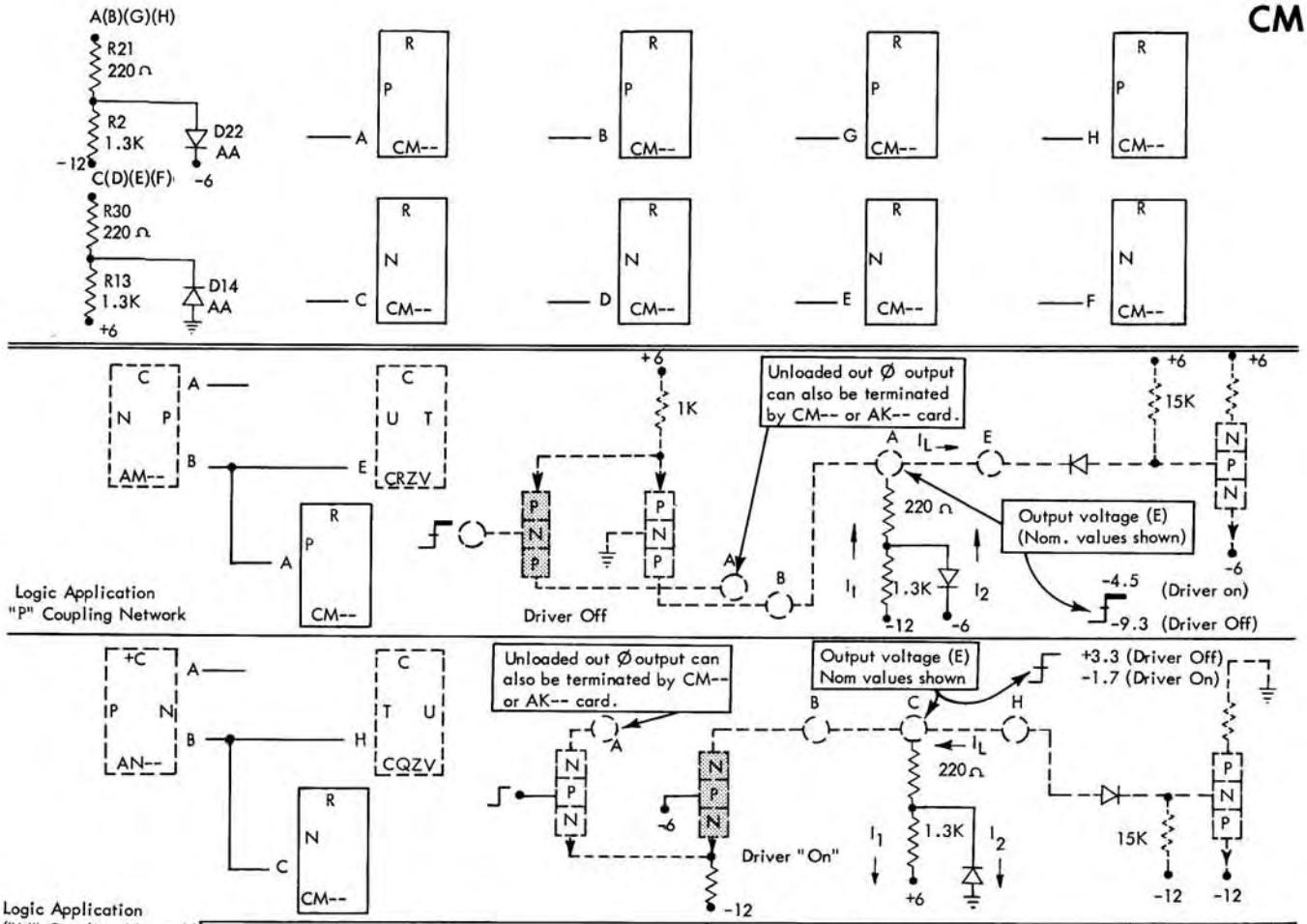
The various diode configurations are used to expand the inputs to both P and N type blocks by reversing the connections to the terminal pins.

Possible logic block representations for these diode cards are shown at the top of the page. The blocks denote the logical function performed and the associated line types. The chart at the bottom of the schematic shows the possible logic block configurations for each circuit on a particular card. For example, circuit 1 of the CLVQ card could be represented by logic blocks 1, 6, or 11.

Typical applications of the diode cards are noted above. A three-legged diode network is shown expanding the +AND input circuit to a P type logic block. Coincidence of plus levels must occur at all inputs to the +AND and the extender card for the transistor to turn on. A single diode is also shown limiting the off output of the CTDL transistor to ground which permits direct drive into voltage mode circuitry.

Application

These diode cards are normally tied to extender inputs of CTDL logic blocks and allow additional inputs to control the logic transistor. The logical functions performed by the various configurations are dependent on their circuit use.



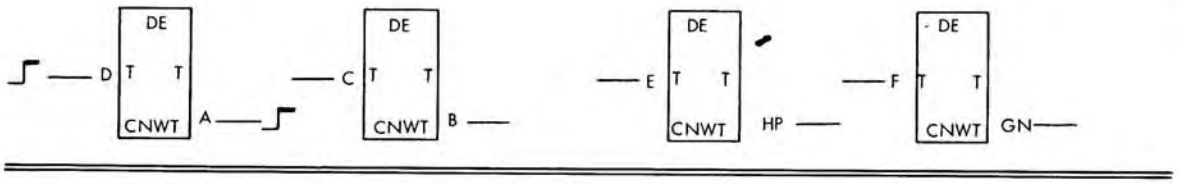
CM-- 371256		"P" Coupling Network						"N" Coupling Network						Nom. Load I_L (ma)
		In Ø			Out Ø			In Ø			Out Ø			
		E	I_1	I_2	E	I_1	I_2	E	I_1	I_2	E	I_1	I_2	
		Volts	ma	ma	Volts	ma	ma	Volts	ma	ma	Volts	ma	ma	
Driver On	Min.	-5.4	4.8	0.0	-5.2	5.0	0.0	-0.6	4.8	0	-0.8	5.0	0	0.2 (Min)
	Max.	-3.7	4.9	2.5	-3.0	5.3	5.3	-2.3	4.9	2.5	-3.0	5.3	5.3	
Driver Off	Min.	-7.6	0.7	-0.1	-7.4	0.7	-0.1	1.6	0.7	-0.1	1.4	0.7	-0.1	2.3 (Max)
	Max.	-11.0	2.4	0.0	-11.0	2.5	0.0	+5.0	2.4	0	5.0	2.5	0	

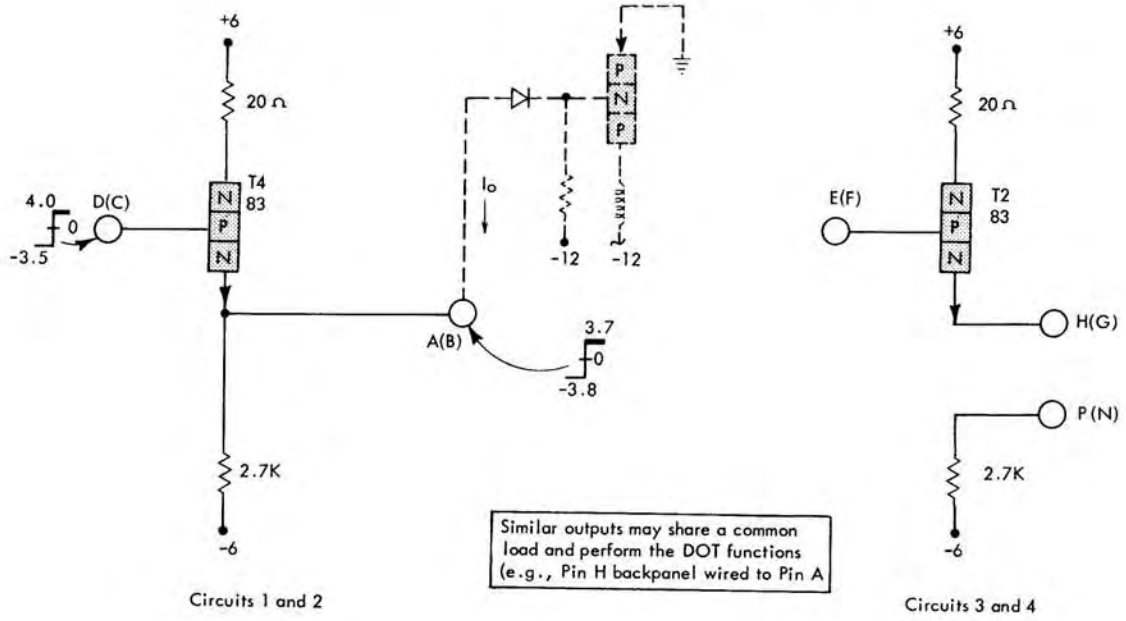
Current Mode to CTDL Coupling Network

Eight coupling networks are located on the CM - - card and are used to properly terminate unloaded current-mode blocks for direct drive into CTDL logic blocks. Four of the coupling networks permit the outputs of N type current-mode blocks to drive directly into P type CTDL blocks. The remaining four coupling networks permit the output of P type current-mode blocks to drive directly into N type CTDL blocks.

The chart above shows the current required from the load supply voltages to the CTDL output voltage available from the coupling network. Values are shown for the (1) driver on-off status (2) current-mode output used (in-phase or out-of-phase) and (3) type of coupling network used.

Consider the P type coupling network illustrated above. An in-phase current-mode output is properly terminated by the coupling network and drives a P type CTDL block. With the driver off, to have an output of −7.6 to −11.0v from the coupling network, 0.7 to 2.4ma flows from the −12v. supply. When the driver is on, to obtain an output of −5.4 to 3.7v, 4.8 to 4.9ma flows from the −12v supply and 0 to 2.5ma flows from the −6v supply. Output loading conditions determine the actual voltage values obtained.





Circuits 1 and 2

Circuits 3 and 4

CNWT 371260

Input Level		Output Level		Delays * (usec)				Circuit Use
Min.	Max.	Min.	Max.		Load	3 CTDL Blocks	15 CTDL Blocks	
1.8 / -0.7	6.24 / 0 / -6.24	1.44 / -0.7	6.24 / 0 / -6.24	Turn On	Min.	.23	.32	DE -DEA +DEO
					Max.	.68	.68	
				Turn Off	Min.	.05	.09	
					Max.	.13	.25	

* Function of capacitive loading and number of CTDL blocks driven

CTDL Emitter Follower NPN

The CNWT card consists of four one-way NPN emitter follower circuits that provide sufficient current to drive into branching circuits. Each circuit serves as a non-translating current amplifier that accepts a T input from a CTDL logic block and provides an in-phase T output. There is a slight DC shift between the input and output voltage levels.

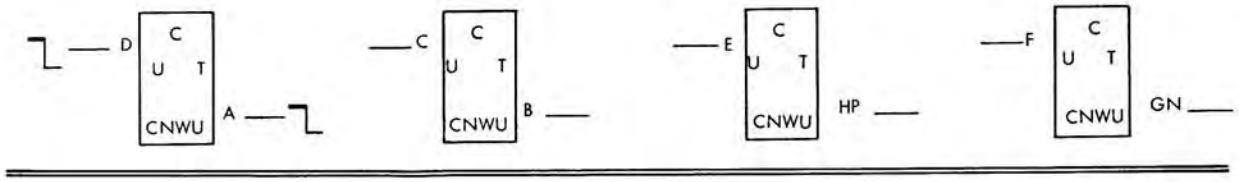
Circuit Description

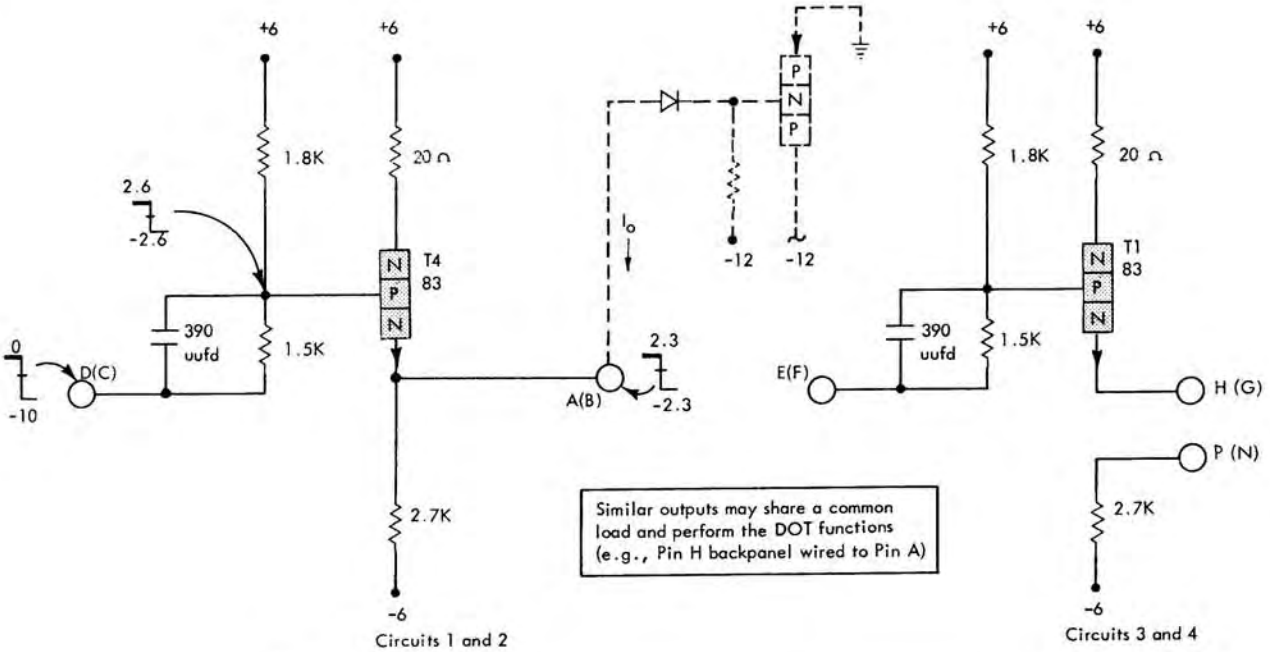
A −T level input allows a minimum of current to flow through the emitter follower T4. The output at pin A clamps to this input value minus the base-emitter voltage drop of approximately 0.3v. When the input increases to +4v, conduction through T4 increases and the output at pin A clamps to the input voltage. Capacitive loading and the number of blocks driven affect the circuit delays.

Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. These circuits are normally used for power amplification of positive-going T lines, for impedance matching, or for isolation without inversion of a signal.

Additional flexibility is provided by this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. In the circuits illustrated above, the DEO function is performed if pin H is wired to pin A. Considering positive logic, a +T input at either pin D or pin E will give a +T output at pin A and satisfy the DEO function. Circuits 3 and 4 also function as standard emitter followers by back-panel wiring to their respective emitter resistors.





CNWU 371258

Input Level		Output Level		Delays* (usec)				Circuit Use
Min.	Max.	Min.	Max.		Load	1 CTDL Block	10 CTDL Block	
-0.5 / -6 / -7.4	+0.2 / -6 / -12.48	1.44 / 0 / -0.74	3.1 / 0 / -5.2	Turn On	Min.	.21	.25	C +CO -CA +TC +TCO
					Max.	.70	.70	
				Turn Off	Min.	.19	.28	
					Max.	.34	.60	

*Function of capacitive loading and the number of CTDL blocks driven

CTDL U to T Converter

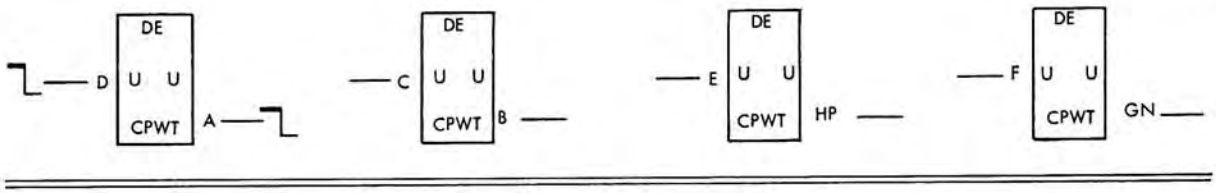
The CNWU card consists of four one-way NPN emitter follower circuits. Each circuit converts a U line input to an in-phase T line and provides the current amplification required to drive branching circuits.

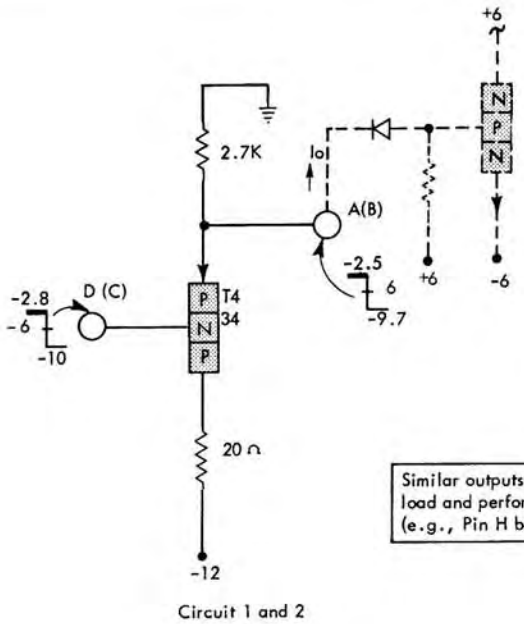
Circuit Description

Operation is similar to that of the basic emitter follower. The input voltage divider network sets the base level so that T4 is always in conduction. When the input is up, the base voltage of T4 is near +2.6v and sets the output at pin A to approximately this voltage minus the base-emitter drop. Decreasing the input of pin D to −10v causes the base voltage to drop to −2.6v. The conduction through T4 decreases and the output at pin A follows the input swing (minus the base-emitter voltage drop). Capacitive loading and the number of blocks driven effect the circuit delays noted in the chart above.

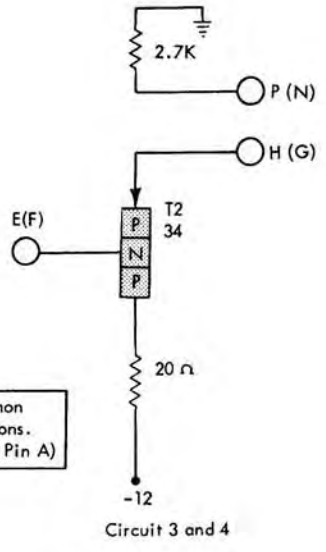
Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. These circuits provide current amplification of positive-going signals, serve as buffer devices to match impedances, or provide isolation without inversion. Additional flexibility is provided on this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back panel wiring. In the circuits illustrated above, the CO function is performed if pin H is wired to pin A. Considering positive logic, a +U level at either pin D or pin E will provide a +T output level. Circuits 3 and 4 also function as standard convert circuits by pack-panel wiring to their respective emitter resistors.





Circuit 1 and 2



Circuit 3 and 4

Similar outputs may share a common load and perform the DOT functions. (e.g., Pin H backpanel wired to Pin A)

CPWT 371259

Input Level		Output Level		Delay* (usec)				Circuit Use
Min.	Max.	Min.	Max.		Load	3 CTDL Blocks	15 CTDL Blocks	
-5.46 / -7.6	+.24 / -6 / -12.48	-5.26 / -7.4	0.2 / -6 / -12.48	Turn On	Min.	.18	.27	DE
					Max.	.48	.62	-DEO
				Turn Off	Min.	.08	.12	+DEA
					Max.	.17	.33	

*Function of capacitive loading and number of CTDL blocks driven

CTDL Emitter Follower PNP

The CPWT card consists of four one-way PNP emitter follower circuits that provide sufficient current to drive into branching circuits. Each circuit serves as a non-translating current amplifier, accepting a U input from CTDL logic blocks and providing an in-phase U output. There is a slight DC shift between the input and output voltage levels.

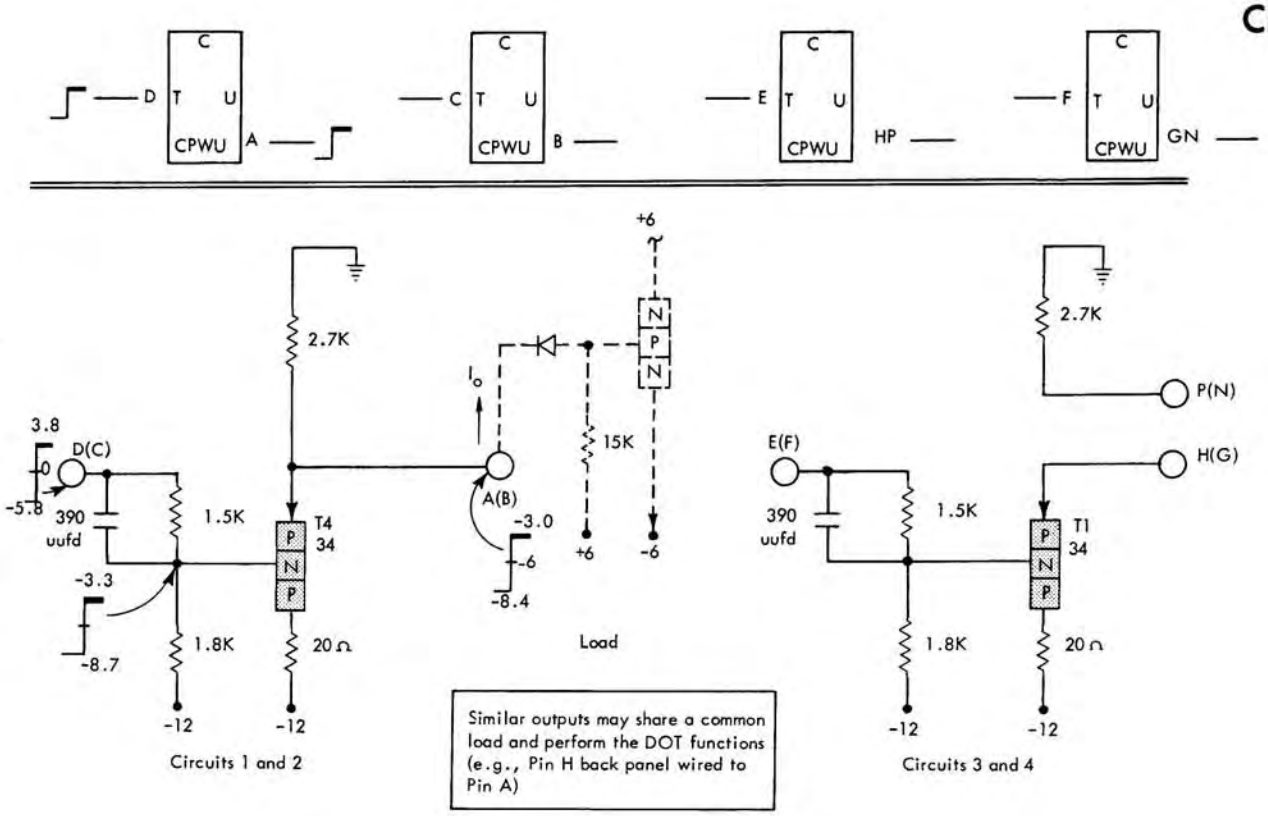
Circuit Description

A +U input allows a minimum of current to flow through the emitter follower T4. The output at pin A clamps to this input value minus the base-emitter drop of 0.3v. When the input drops to −10v, T4 is forward-biased more and conduction through T4 increases. The voltage at pin A follows the voltage swing at the base of T4 (minus the base-emitter drop). Capacitive loading and the number of blocks driven affect the circuit delays noted above.

Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The PNP emitter follower circuit is normally used for current amplification of negative-going U lines and to furnish additional drive to P type branching circuits. These circuits are also used for impedance matching or for isolation without inversion.

Additional flexibility is provided on this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. In the circuit illustrated above the DEA function is performed if pin H is wired to Pin A. Considering positive logic, a +U input is required at both pins D and E to obtain a +U output at pin A and satisfy the DEA function. Circuits 3 and 4 also function as standard emitter followers by back-panel wiring to their respective emitter resistors.



*Function of capacitive loading and number of CTDL blocks driven.

CPWU 371257

Input Level		Output Level		Delays* (usec)				Circuit Use
Min.	Max.	Min.	Max.		Load	1 CTDL Block	10 CTDL Blocks	
+1.44	+6.24	-5.2	-0.8	Turn Off	Min.	.17	.20	C
-5.46	-6.24	-7.4	-9.2		Max.	.52	.53	CA
				Turn On	Min.	.14	.25	-TC
					Max.	.26	.56	-TCO

CTDL T to U Converter

The CPWU card consists of four one-way PNP emitter follower circuits designed for current amplification. Each circuit translates a T input to a U in-phase output and provides the current amplification required to drive branching circuits.

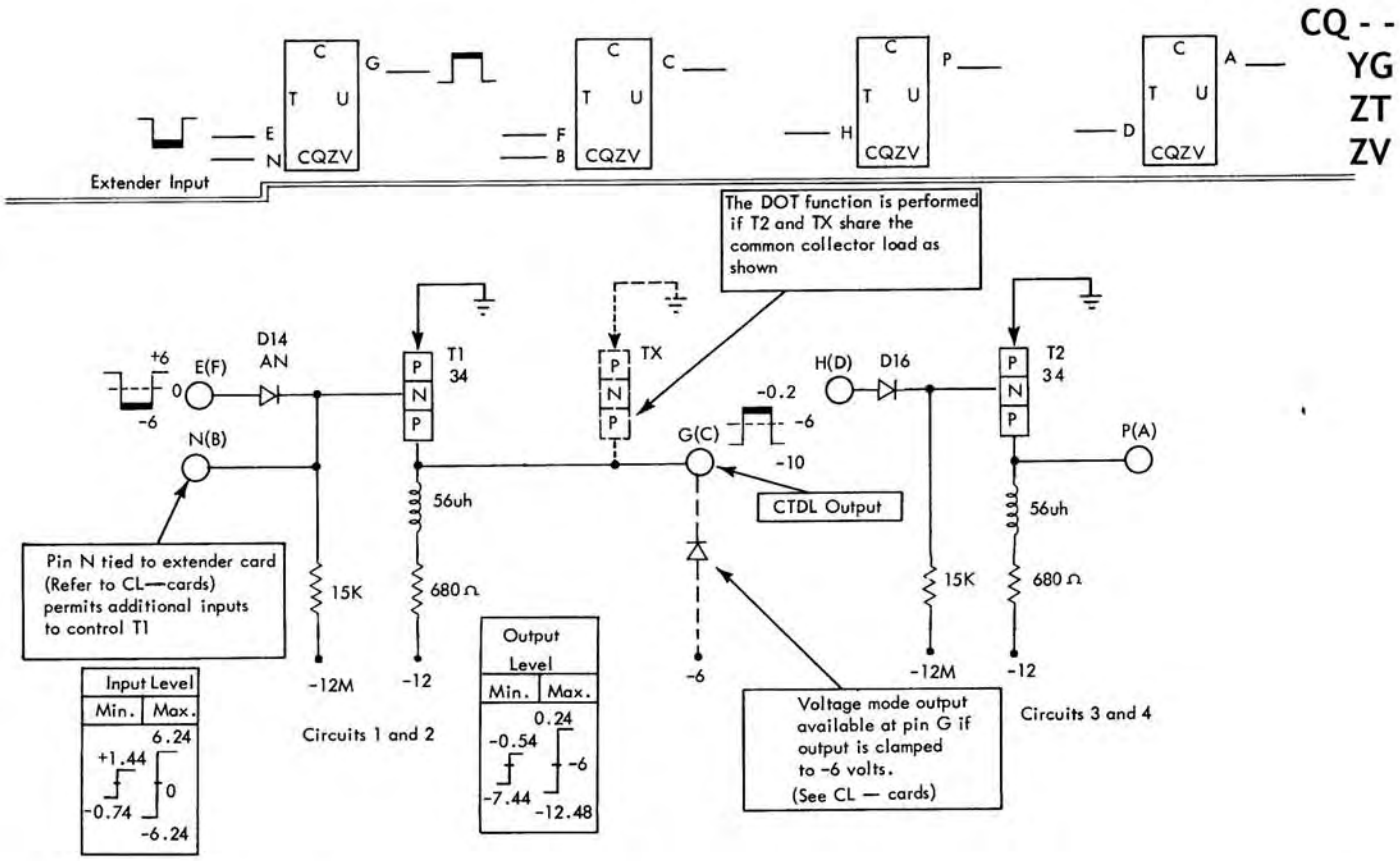
Circuit Description

The input voltage divider network sets the base voltage of T4 so that it is always in conduction. When the input is up, the base level of T4 is near −3.3v. T4 is forward-biased on and clamps the output at pin A to −3.0v. The small drop (0.3v) exists between the base and the emitter of the conducting transistor. Decreasing the input to −5.8v causes the base voltage to drop to −8.7v. Conduction through T4 increases and the output at pin A becomes −8.4v. Capacitive loading and the number of blocks driven affect the circuit delays given in the chart.

Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. These circuits normally provide current amplification to negative-going signals. They are also used as buffer devices, to match impedances, or to provide isolation without inversion.

Additional flexibility is provided on the card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. In the circuit illustrated above the CA function is performed if pin H is wired to pin A. Considering positive logic, a +T level is required at both pins D and E to obtain a +U output level, and to perform the CA function. Circuits 3 and 4 also function as standard convert circuits by back-panel wiring to their respective emitter resistors.



Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Ckt 1	Ckt 2	Ckt 3	Ckt 4	Delays Per (usec)		Basic Block	Par'lel C'lector	CM Base	Diode Input	100 uufd	Circuit Use
CQZV	1271	1-2	No	Yes	Yes	Yes	Yes	Turn On	Min.	.20	.00	.00	.00	.02	+C
CQZT	1272	1-2	No	Yes	Yes	No	No		Max.	.70	.007	.015	.02	.05	-CO +CA
CQYG	1278	1-2	No	Yes	No	No	No	Turn Off	Min.	.06	.004	.005	.00	.03	-TC
CQ--	1273	1-2	No	No	No	No	No		Max.	.18	.01	.02	.005	.06	-TCO

CTDL T to U Converter

The CQZV card consists of four one-way NPN logic circuits.Each circuit on the card translates a T input to an out-of-phase U output. Internal collector loading for each circuit gives CTDL outputs at pins G, C, P and A. Extender pins N and B permit additional inputs to control circuits 1 and 2.

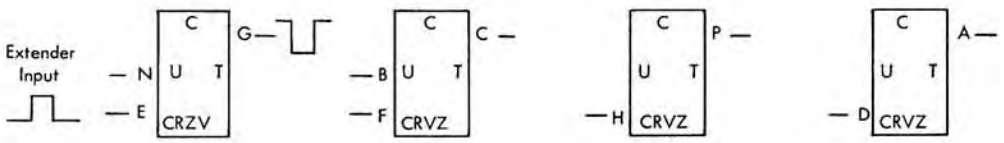
Circuit Description (Circuit 1)

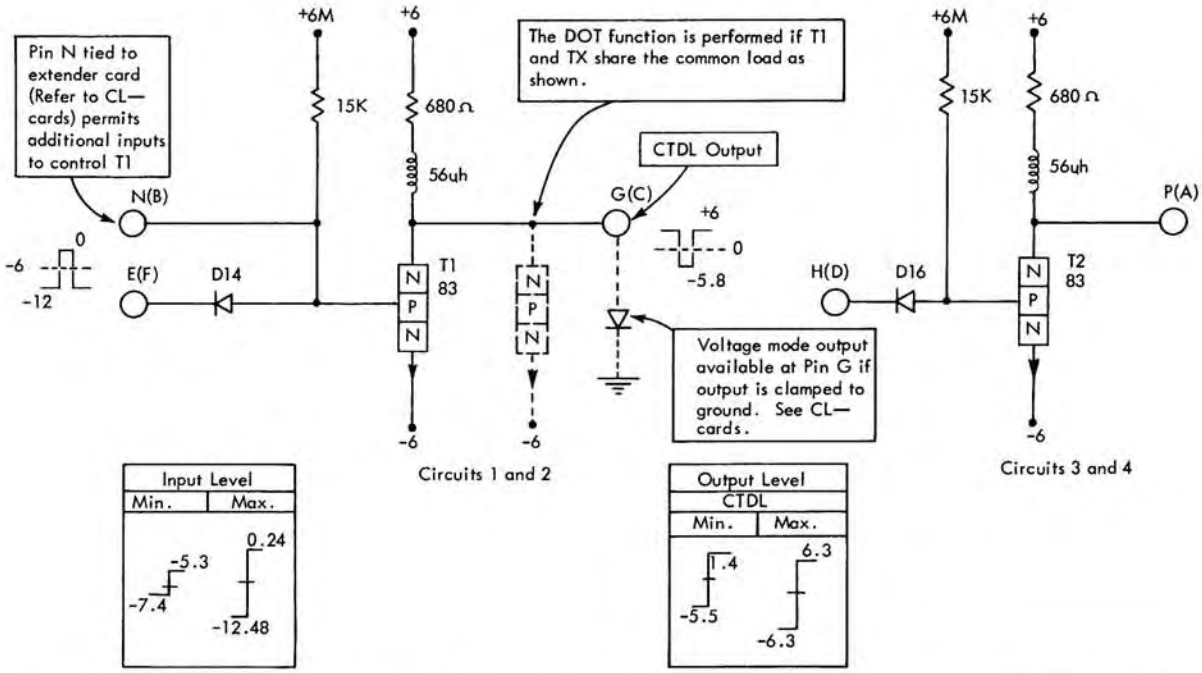
A −T level is required at pin E to forward-bias T1 on. With T1 on, the output at pin G is near 0v (minus the slight drop across the forward-biased transistor). When the input signal increases to +6v, T1 is turned off. The low forward impedance of the conducting diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin H decreases to −12v.

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

The circuit loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT function is accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.





Card Code	Part No 37---	Extender Input Circuit	CM Output Circuit	Collector Loading Circuit 1	2	3	4	Delays	Per	Basic Block	Par'lel C'lector	CM Base	Diode Input	100 uufd (usec)	Circuit Use
CRVZ	1274	1,2	No	Yes	Yes	Yes	Yes	Turn On	Min.	0.18	.00	.00	.00	.02	+C CO +TC +TCO -CA
CRZT	1275	1,2	No	Yes	Yes	No	No		Max.	0.52	.007	.02	.02	.05	
CRYG	1277	1,2	No	Yes	No	No	No	Turn Off	Min.	0.05	.004	.005	.000	.03	
CR--	1276	1,2	No	No	No	No	No		Max.	0.12	.01	.02	.005	.06	

CTDL U to T Converter

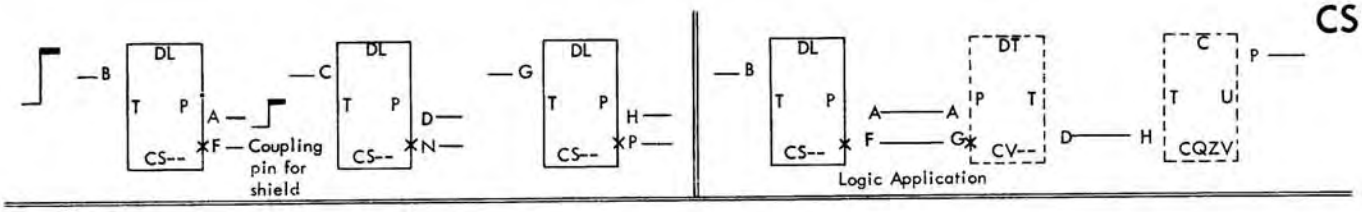
The CRZV card consists of four one-way NPN logic circuits. Each circuit on the card translates a U input to an out-of-phase T output. Internal collector loading for each circuit gives CTDL outputs at pins G, C, P and A. Extender pins N and B permit additional inputs to control circuits 1 and 2.

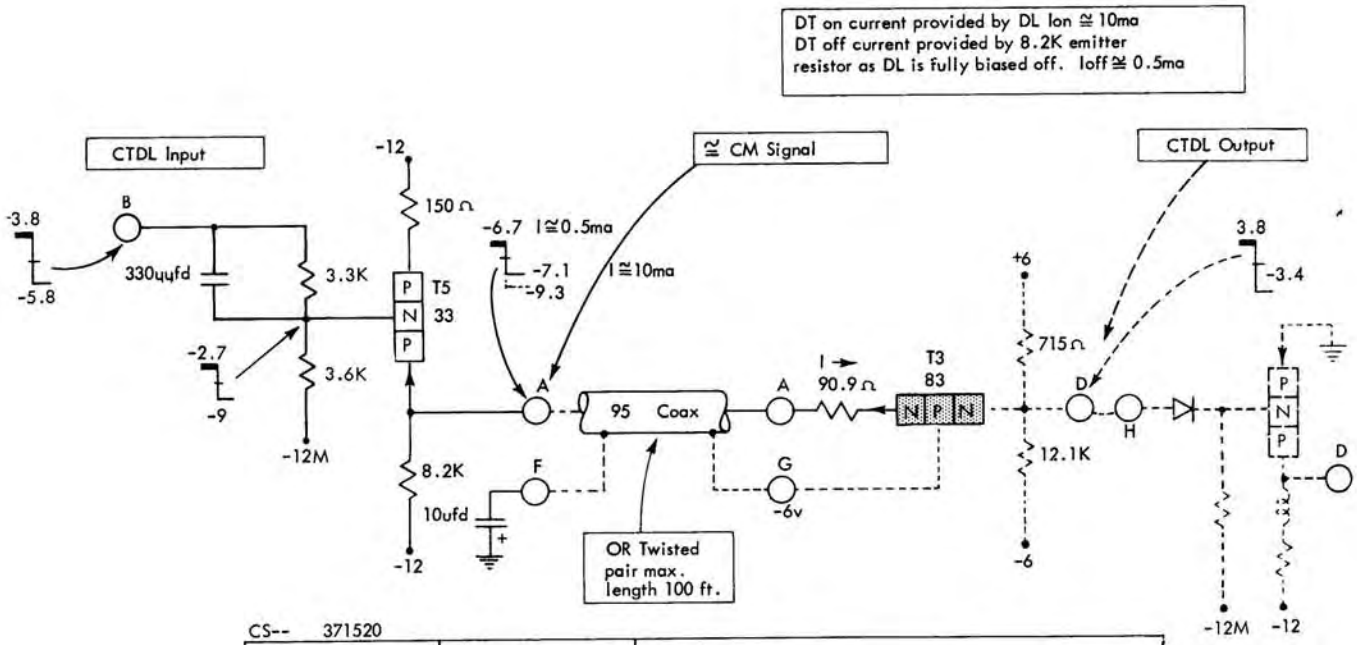
A +U level is required at pin E to forward-bias T1 on. With T1 on, the output at pin G is near −6v minus the slight voltage drop across the forward-biased transistor. When the input signal drops to −12v, T1 is turned off. The low forward impedance of the conducting diode rapidly removes the excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin G increases to +6v (No Load).

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

The circuit loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT function is accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.





CS-- 371520

CTDL Input		CTDL Output		Delays		usec		
Pin B	(DL)	Pin D	(DT)		Per	Driver-Cable-Termin'r	100 uufd	Cable
Min	Max	Min	Max	Turn On	Min	0.03	0.01	.003/ft
1.4 / -5.5	6.2 / -6.2	1.4 / -0.7	5.9 / 0 / -6.2		Max	0.15		
				Turn Off	Min	0.03	0.02	.003/ft
					Max	0.15		

CTDL N-Type Line Driver

The CS - - card consists of three PNP line driver circuits that translate a T input to a suitable P output for efficient transmission between two widely separated points. Each circuit provides the necessary drive to a coaxial or twisted pair cable that is properly terminated by a NPN line terminator. For proper decoupling action, the neutral wire of the twisted pair or the shield of the coaxial cable is AC coupled to ground at the line driver and returned to the base reference voltage at the line terminator. The decoupling capacitor is physically located on the line driver card. There is no phase inversion between the T input to the line driver and the T output from the line terminator.

Circuit Description

The line driver and the line terminator are discussed at this time to fully illustrate the operation of this circuit.

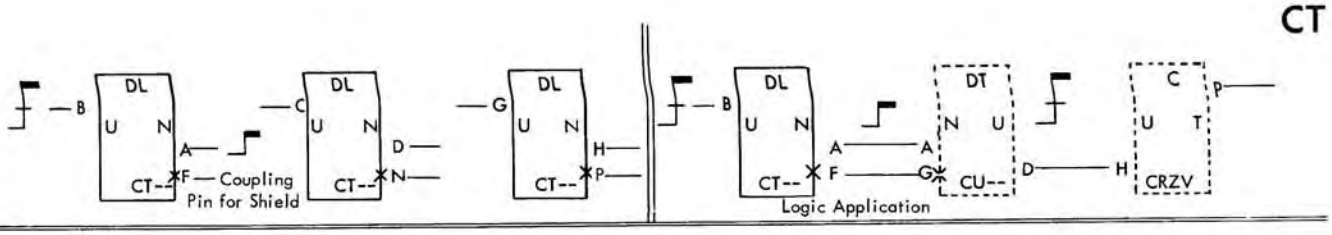
Assume a starting condition of T5 off and T3 on, with the emitter of T5 at −6.7v. When a +T line is applied to pin B of the line driver, the input divider network sets the base of T5 to −2.7v. T5 is reverse-biased off and approximately 0.5ma of current is supplied the emitter of T3. Current flow through the common-base amplifier and coupling network causes the voltage at pin D of the line terminator to approach +3.8v.

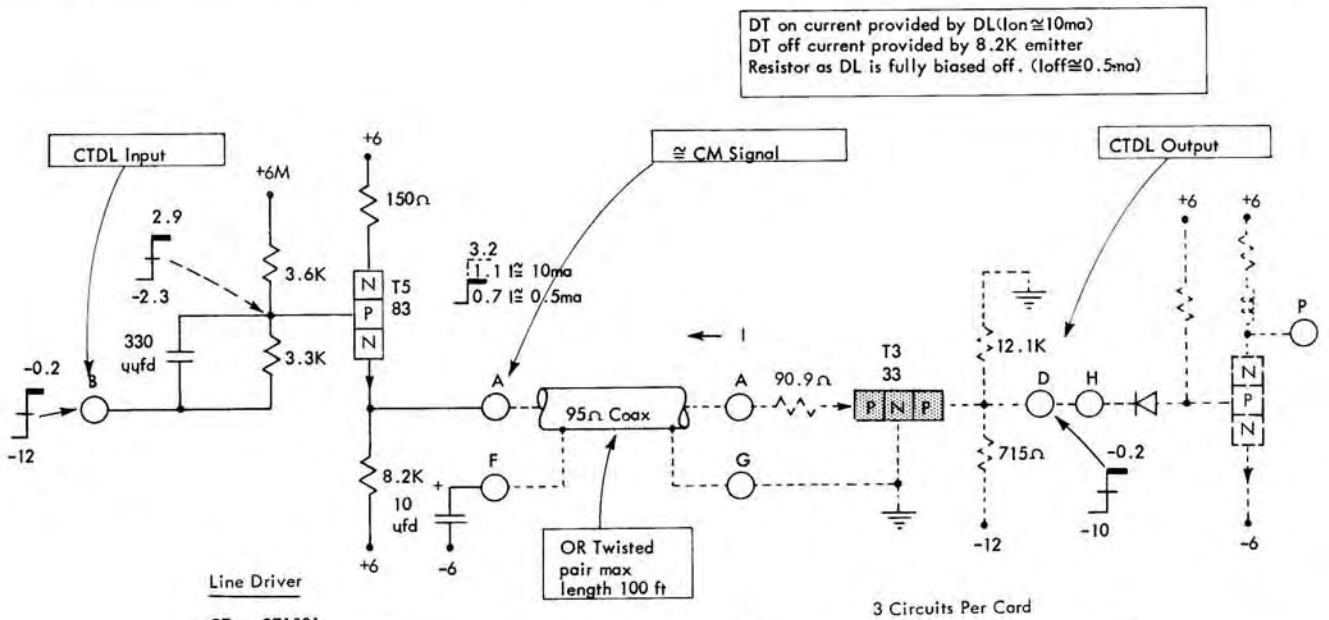
A −T input at pin B of the line driver causes the base level of T5 to decrease to −9v. T5 is forward-biased on and supplies up to 10ma to the line terminator. The output at pin A of the line driver decreases to −7.1v. The additional current through T3 and the coupling network causes the line terminator output at pin D to drop to −3.4v.

The delays given above are for the complete driver, cable, and terminator configuration. Capacity loading and cable length increase the delay values. Typical loading on the line terminator is shown above.

Application

This configuration (transmission line driver and line terminator) is used whenever a CTDL T line is to be driven between two widely separated points. By limiting the voltage swings driving into the cable, the effects of cable delays and DC crosstalk between cables are minimized. A NPN line terminator (CV - - card) is used with the line driver.





CT-- 371521

CTDL Input		CTDL Output		Delays: usec				
Pin B (DL)		Pin D (DT)					100 uufd	Cable
Min.	Max.	Min.	Max.	Turn On	Per	Driver-Cable-Termin'r		
-0.5	0.24	-5.3	0.24		Min.	0.03	0.01	.003/ft
-7.4	-6 -12.48	-7.4	+6 -12		Max.	0.15		
				Turn Off	Min.	0.03	0.02	.003/ft
					Max.	0.15		

CTDL P-Type Line Driver

The CT - - card consists of three NPN transmission line driver circuits that translate a CTDL U line to a current-mode N line for efficient transmission between two widely separated points. Each circuit provides the necessary drive to a coaxial or twisted pair cable that is properly terminated by a PNP line terminator.

For proper decoupling action, the neutral wire of the twisted pair or the shield of the coaxial cable is AC coupled to −6v at the line driver and returned to the base reference voltage at the line terminator. The decoupling capacitor is physically located on the line driver card. No phase inversion occurs between the U input at the line driver and the U output from the line terminator.

Circuit Description

To aid in understanding the operation of this line driver, both the transmission line driver and terminator circuits are discussed at this time.

Assume a starting condition of T5 off and the grounded base terminator conducting at least 0.5ma. The emitter voltage of T5 is near +0.7v. When a −U line is applied to pin B of the line driver, the base level of T5 is set at −2.3v by the input divider. T5 is reverse-biased off and the output at pin A stays at +0.7v. Minimum current flow through T3 and the coupling network to the 8.2K resistor and +6v results in an output at pin D near −10.0v.

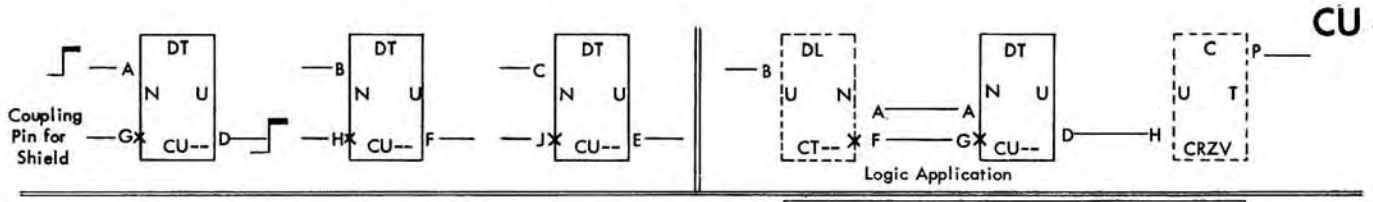
A +U input at pin B of the line driver causes the base level of T5 to increase to +2.9v. T5 is forward-biased on, and increased current flow (10ma) from the coupling network through T3, the cable, and T5 to +6v causes the output of the line terminator to increase to −0.2v.

The delays given are for the complete driver, cable, and terminator configuration. Capacity loading and cable length increase these delay values. Typical loading is shown for the line terminator.

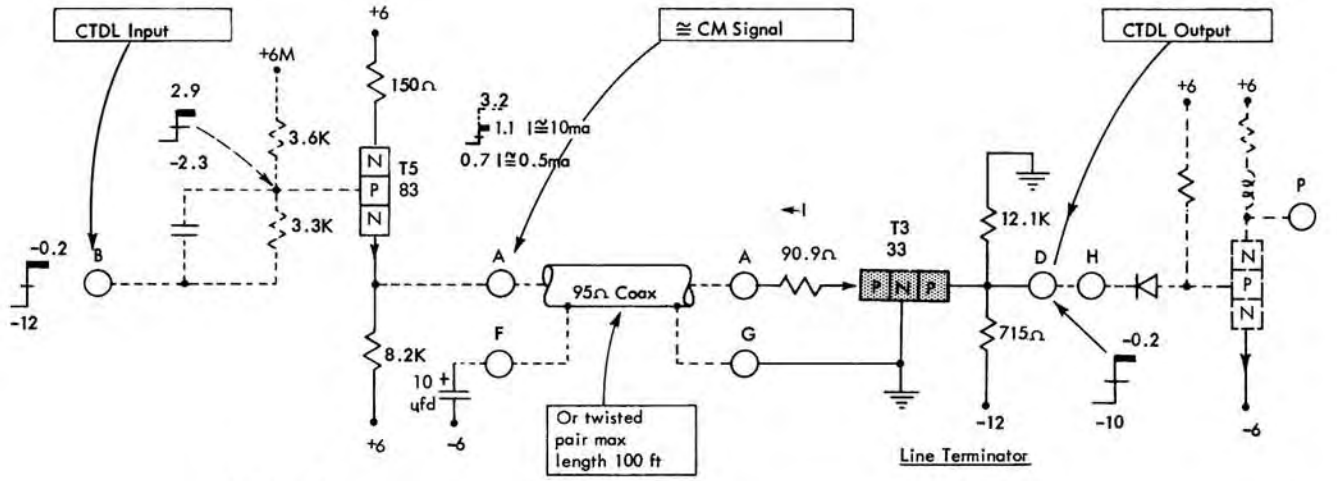
Application

This configuration (transmission line driver and line terminator) is used whenever a CTDL U line is to be driven between two widely separated points. By limiting the voltage swings driving into the cable, the effects of the cable delays and the DC crosstalk between cables are minimized.

A PNP line terminator circuit (CU - - card) is used with this line driver.



DT on current provided by DL (Ion ≅ 10 ma.)
DT off current provided by 8.2K emitter
Resistor as DL is fully biased off (Ioff ≅ 0.5 ma.)



CU-- 371518

3 Circuits Per Card

CTDL Input		CTDL Output		Delays:	usec			
Pin B (DL)		Pin D (DT)		Turn On	Per	Driver-Cable-Termin'r	100 uufd	Cable
Min.	Max.	Min.	Max.		Min.	0.03	0.01	.003/ft
-0.5 to -7.4	0.24 to -6 to -12.48	-5.3 to -7.4	0.24 to -6 to -12		Max.	0.15		
				Turn Off	Min.	0.03	0.02	.003/ft
					Max.	0.15		

CTDL N-Type Line Terminator

The CU - - card consists of three PNP transmission line terminator circuits that translate a current mode N input to a CTDL U in-phase output. Each circuit terminates coaxial or twisted pair cables in their characteristic impedance and provides minimum loading on the NPN driving circuit. The 90.9 ohm resistor in series with the emitter to base impedance of the grounded base stage is selected for optimum match to the twisted pair and coaxial cables.

For proper decoupling action, the neutral wire of the twisted pair or the shield of the coaxial cable is AC coupled to −6v at the line driver and returned to the base reference voltage at the line terminator. The decoupling capacitor is physically located on the line driver card. No phase inversion occurs between the U input at the line driver and the U output from the line terminator.

Circuit Description

To aid in understanding the operation of the PNP line terminator, both the transmission line driver and terminator circuits are discussed at this time.

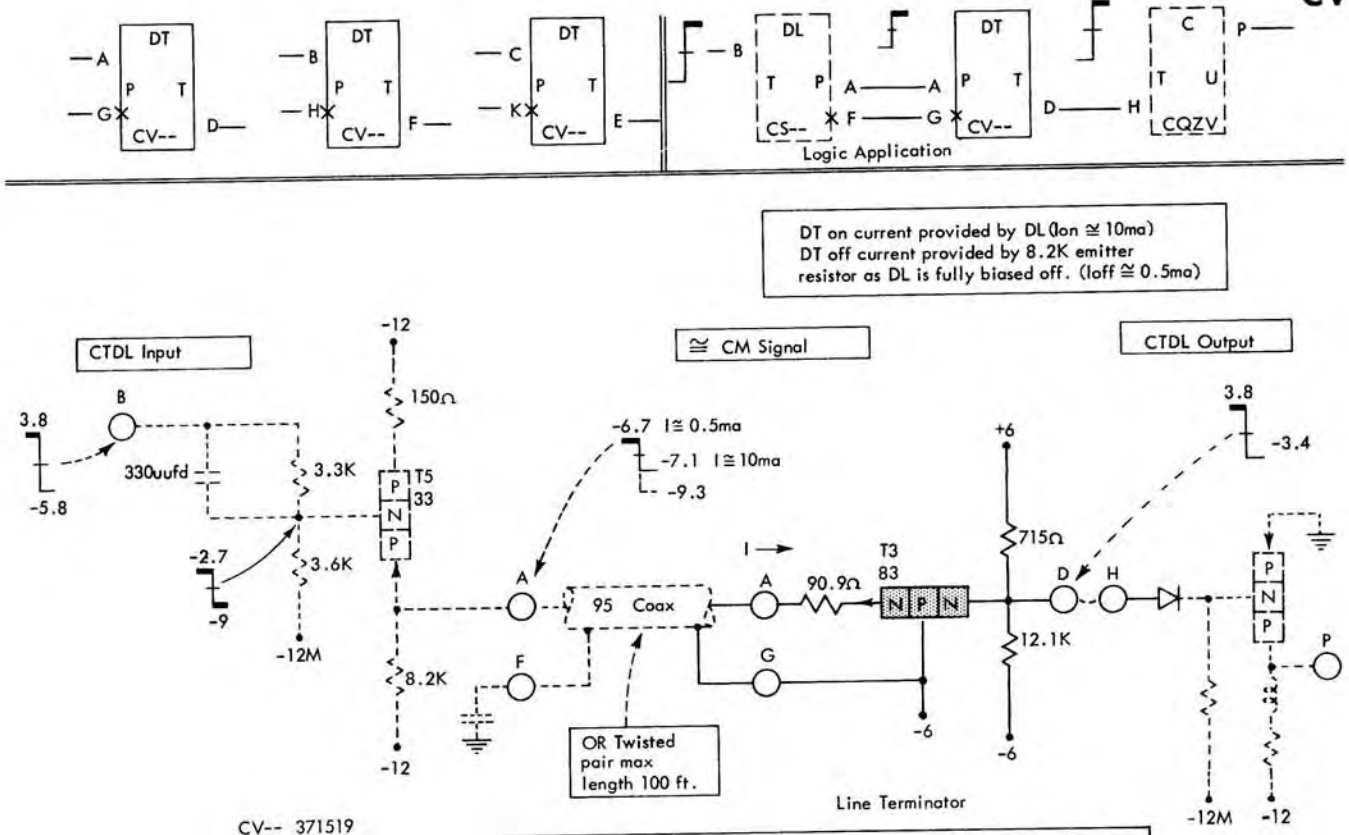
Assume a starting condition of T5 off and the grounded base terminator conducting at least 0.5ma. The emitter voltage of T5 is +0.7v. When a −U line is applied to pin B of the line driver, the base level of T5 is set to −2.3v by the input divider. T5 is reverse-biased off and the output at pin A stays at +0.7v. Minimum current flowing in T3 and the coupling network results in an output at pin D near −10.0v.

A +U input at pin B of the line driver causes the base level of T5 to increase to +2.9v. T5 is forward-biased on and increases the current flow through the grounded base terminator circuit to 10ma. The line driver output at pin A is clamped at 1.1v by the line terminator. Increased current flow from the coupling network through T3, the cable, and T5 causes the output of the line terminator to increase to −0.2v.

The delays given are for the complete driver, cable and terminator configuration. Capacity loading and cable length increase the delay values. Typical loading is illustrated for the line terminator.

Application

This configuration (transmission line driver and line terminator) is used whenever a CTDL U line is to be driven between two widely separated points. By limiting the voltage swings driving into the cable, the effects of the cable delays and the DC crosstalk between cables are minimized. A NPN line driver circuit (CT - - card) is used to drive this line terminator.



CV-- 371519

CTDL Input		CTDL Output		Delays		(usec)		
Pin B (DL)		Pin D (DT)			Per	Driver-Cable-Termin'r	100uufd	Cable
Min.	Max.	Min.	Max.	Turn On	Min.	0.03	0.01	0.003/ft
1.4 / -5.5	6.2 / -6.2	1.4 / -0.7	5.9 / -6.2		Max.	0.15		
				Turn Off	Min.	0.03	0.02	0.003/ft
					Max.	0.15		

CTDL P-Line Terminator

The CV-- card consists of three NPN transmission line terminator circuits that translate a current-mode P input to a CTDL T in-phase output. Each circuit terminates coaxial or twisted pair cables in their characteristic impedance and provides minimum loading on the PNP driving circuit. The 90.9 ohm resistor in series with the emitter to base impedance of the grounded base stage is selected for optimum match of the twisted pair or coaxial cable used.

For proper decoupling action, the neutral wire of the twisted pair or the shield of the coaxial cable is AC coupled to ground at the line driver and returned to the base reference voltage at the line terminator. The decoupling capacitor is physically located on the line driver card. No phase inversion occurs between the T input at the line driver and the T output from the line terminator.

Circuit Description

Both the line driver and the line terminator are discussed at this time to fully illustrate the operation of the line terminator.

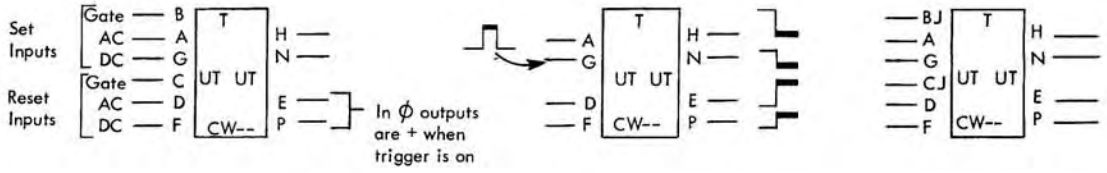
Assume a starting condition of T5 off and T3 on, with the emitter of T5 at −6.7v. When a +T line is applied to pin B of the line driver, the input divider network sets the base of T5 to −2.7v. T5 is reverse-biased off and approximately 0.5ma of current is supplied to the emitter of T3. Current flow into the common-base amplifier and coupling network causes the voltage at pin D of the line terminator to approach 3.8v.

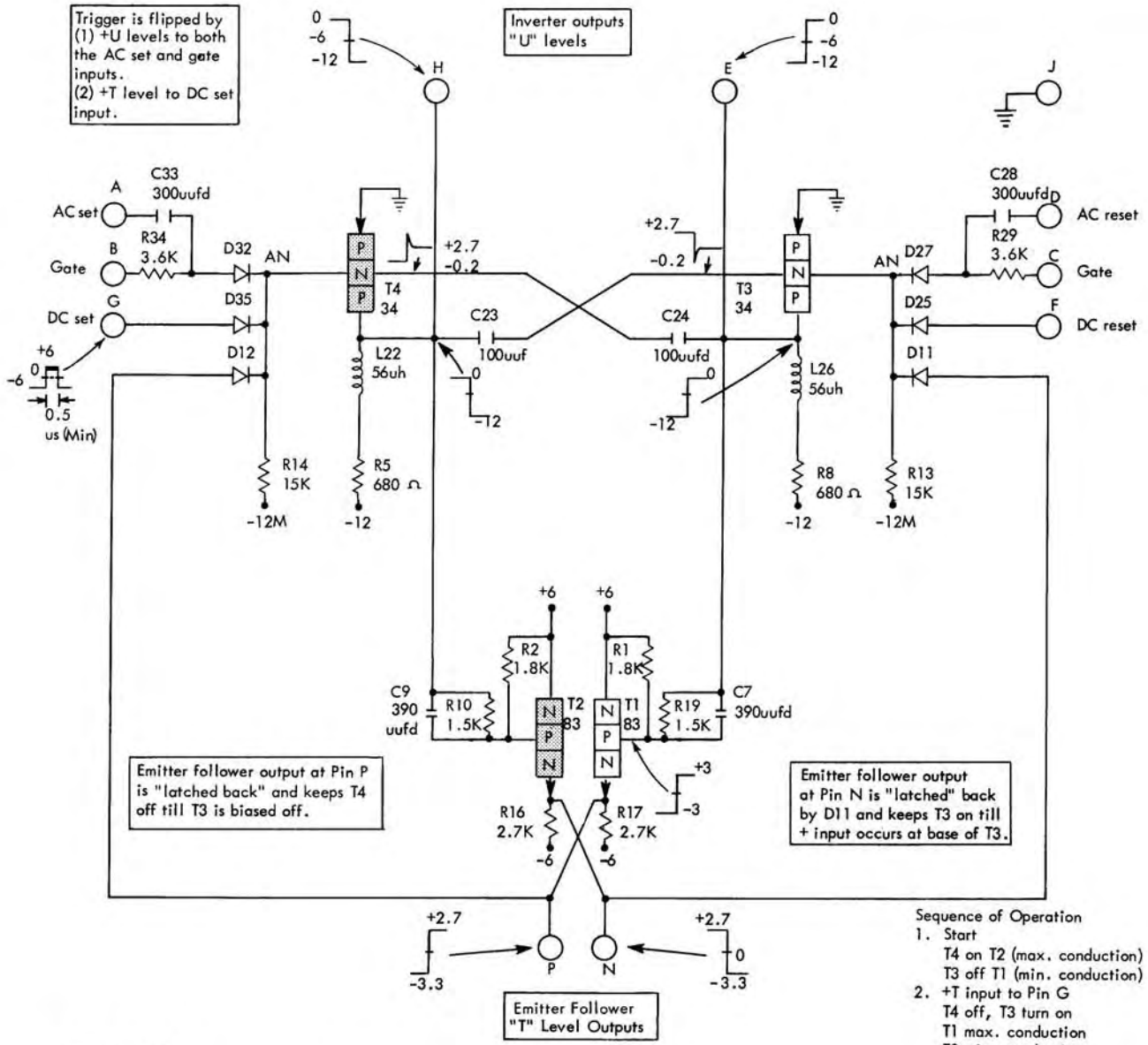
A −T input at pin B of the line driver causes the base level of T5 to decrease to −9v. T5 is now forward-biased on and supplies up to 10ma to the line terminator. The output at pin A of the line driver decreases to −7.1v. Additional current through T3 and the coupling network causes the line terminator output at pin D to drop to −3.4v.

The delays given above are for the complete driver, cable, and terminator configuration. Capacity loading and cable length increase the delay values. Typical loading for the line terminator is shown.

Application

This configuration (transmission line driver and line terminator) is used whenever a CTDL T line is to be driven between two widely separated points. By limiting the voltage swings driving into the cable, the effects of cable delays and DC crosstalk between cables are minimized. A PNP line driver circuit (CS-- card) is used with this line terminator circuit.





Sequence of Operation

1. Start
   T4 on T2 (max. conduction)
   T3 off T1 (min. conduction)
2. +T input to Pin G
   T4 off, T3 turn on
   T1 max. conduction
   T2 min. conduction
   Emitter follower outputs latch trigger in this state till positive signal appears at base of T3 and returns trigger to its original state.

CW-- 371534

Input Levels				Output Levels				Delays * (usec)				
AC Set & Gate "U"		Dc Set "T"		Emitter Follower		Inverter			Inverter		Emitter Follower	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
-0.5 / -7.4	+0.2 / -6 / -12.4	+1.4 / 0 / -0.7	6.2 / 0 / -6.2	1.4 / 0 / -0.7	3.1 / -5.2	-5.2 / -7.4	-0.8 / -9.2	Turn On	1	.3	.08	0.4
								Turn Off	.15	.8	.055	0.1

*Measured from 10% to 90% Values

CTDL Trigger 1

The CW - - card consists of a CTDL trigger circuit designed for use in clock and ring circuits and as a single bit memory device. The bistable circuit, consisting of two inverters and two emitter followers, operates at a frequency near 250kc. A positive CTDL signal applied to the AC set and gate inputs or to the DC set inputs controls the triggering action. Both in-phase and out-of-phase outputs are available from this card.

DC Set Input: A positive T line applied to the DC set input causes the circuit to be triggered. Because of the circuit delays, the input pulse duration must be long enough to insure the latch back condition of the trigger (minimum 0.5 microseconds).

AC Set Input: When using the trigger as a single bit memory device, both the signal input and the gate input are driven by CTDL U lines. The gate sets the reference threshold for the AC set input and must be conditioned 3.75 microseconds before the set signal is applied. If the gate is up, a positive U line shift having a minimum pulse duration of 0.5 microseconds is required to flip the trigger.

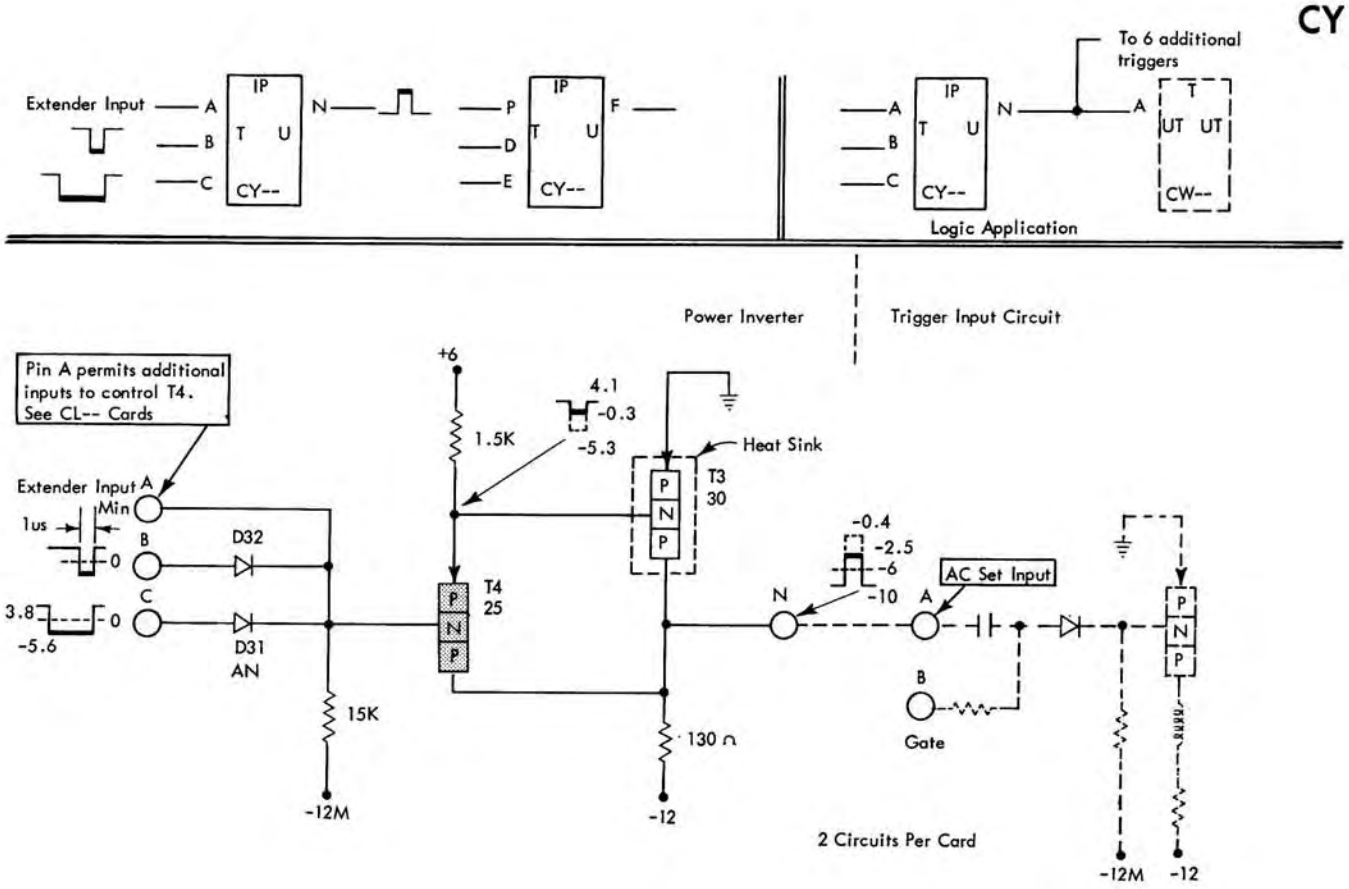
Circuit Description

Assume a starting condition of T4 and T2 conducting, and T3 and T1 off. When a +T level is applied to the DC set input (pin G), the base of T4 becomes more positive than the emitter (ground potential). T4 becomes reverse-biased off and causes its collector voltage to drop to −12v. This negative swing is coupled through C23 to forward-bias T3 on, and to T2 to decrease the conduction through the emitter follower (T2). Conduction through T3 causes its collector voltage to rise to 0v. This positive swing is coupled to T4 by C24 (keeping it cut off) and also to the base of T1. T1 becomes more forward-biased and conducts harder, causing the emitter follower output (pin P) to increase to +2.7v. This up-level is latched back through D12 to keep T4 cut off. If a +T level is now applied to pin F (DC reset), the trigger is flipped to its original state. The positive level at pin F cuts off T3, causing its collector to drop to −12v. This negative shift is coupled through C24 to forward-bias T4 and drive it into conduction. The collector voltage of T4 goes to 0v and allows the emitter follower T2 to conduct more. The positive shift at the collector of T4 is also coupled through C23 to the base of T3 and holds it cut off. The emitter follower output at pin N (2.7v) is latched back through D11 to keep T3 cut off.

The turn-on and turn-off delays are a function of circuit loading and are noted above for nominal conditions. Over-all trigger delays in flipping from state to state average from 0.12 microsecond to 0.45 microsecond.

Application

This circuit is used mainly in ring applications (such as digit and word rings) to provide output pulses of a specific duration. It is also used as a storage device in a binary operation. Various logic block configurations for the trigger circuit are possible and are illustrated above.



CY--371542

Input Level		Output Levels		Delay		usec
Min.	Max.	Min.	Max.		Per	Circuit
1.44 / -1.14	+6.2 / -6.2	-0.4 / -9.	+0.2 / -12.48	Turn On	Min.	0.21
					Max.	0.60
				Turn Off	Min.	0.24
					Max.	0.37

CTDL Power Inverter

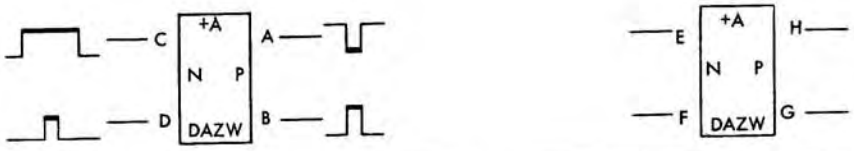
The CY - - card consists of two power inverter circuits used to drive the AC set inputs of the CTDL triggers or equivalent loading. Each circuit is basically a modified emitter follower driving an inverter. Relatively small input signals develop a large power output capable of driving seven CTDL triggers or a maximum capacitive load of 1650$\mu\mu$fd. The input arrangement is similar to the CTDL logic block, and has two diode inputs and an extender input. A −T line of at least one microsecond duration at all inputs is required to drive T4 into maximum conduction.

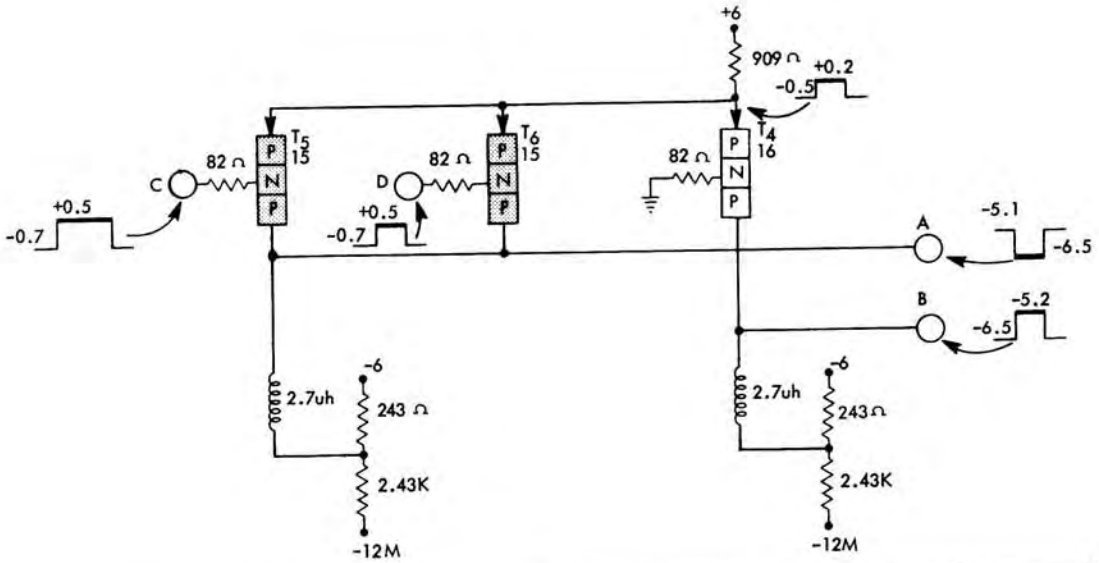
Circuit Description

If any of the inputs at pins A, B, or C are up (3.8v), minimum current flows in the emitter follower T4 and the 1.5K resistor. The emitter follower output (4.1v) reverse-biases T3 off. Minimum current flow from the −12v supply, 130 ohm resistor to the emitter follower circuit sets the output at pin N to near −10v.

When all inputs at pins C, B, and the extended input are down (−5.6v), maximum current flows through T4. The emitter follower output decreases toward −5.3v, but is clamped at −0.3v when T3 becomes forward-biased and conducts. When T3 turns on, increased current through the 130 ohm resistor quickly raises the output at pin N to −2.5v, and up to 30ma is supplied to the AC set inputs of the CTDL triggers or to equivalent loading.

The 130 ohm resistor relates the two collectors so that if T3 becomes saturated, the current through T4 is decreased, which in turn reduces the base current to T3. This degenerative action prevents T3 from operating in saturation and provides medium current outputs with minimum turn-on and turn-off delays.





Card Code	Part No 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
DAZW	1280	Yes	Yes	+A	-O	+0.4	See driver for max. Output Levels	-5.6	-4.9	-5.6	-4.6
DAZU	1281	No	Yes	+AO	-OA	-0.4		-6.4	-6.6	-6.4	-6.6
				+TA	-TO						

Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	Turn Off
Min.	5.62	5.98	4	3
Nom.	6.25	7.22	14	11
Max.	6.87	8.46	23	21

Diffused Junction Two-Way AND, Type A

The two-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of two +N inputs produces a +P in-phase output and a −P out-of-phase output.

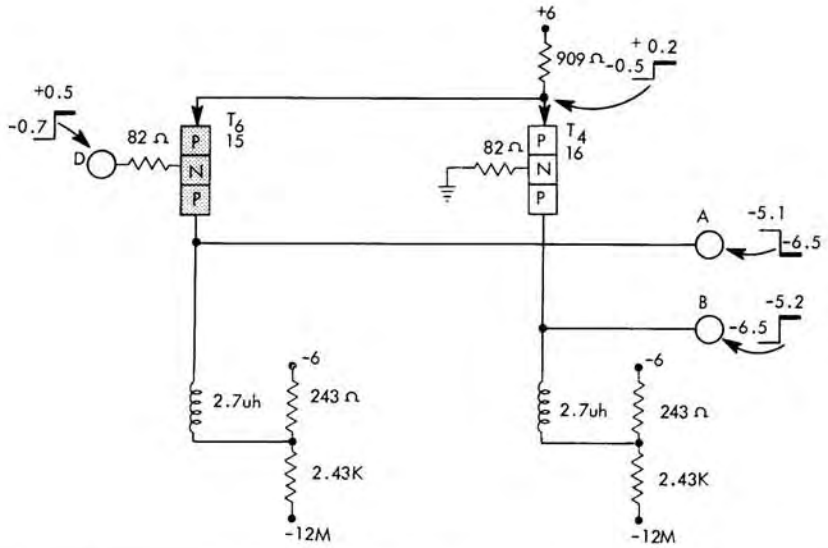
Circuit Description

This circuit utilizes two transistors (T5 and T6) in an AND configuration similar to diode circuitry (the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive, 6v, supply). The emitter output of this AND circuit drives into a ground-base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4, as shown. In this state, output B is at a −P level of −6.5v because of divider current through its coupling network, and output A is at a +P level of −5.1v because of current flow (7.2ma) out of its coupling network through T5 and T6 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output A falls to a −P level and output B rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v).

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 243 ohm and 2.43K resistors shown. In such cases cap code ZU is used (see chart). This circuit is also combined with an OR circuit to make up a trigger, and with other AND circuit blocks to obtain DOT functions.



Card Code	Part No 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
DAZZ	1282	Yes	Yes	C	CO	+0.4	See driver for max. Output Levels	-5.6	-4.9	-5.6	-4.6
DAZX	1283	No	Yes			-0.4		-6.4	-6.6	-6.4	-6.6

	Ma. Output In Ø	Ma. Output Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
Min.	5.62	5.98	3	4
Nom.	6.25	7.22	14	12
Max.	6.87	8.46	23	24

Diffused Junction N-to-P Converter, Type A

The N-to-P converter is a single input logic block. It is fed by an N line and produces both an in-phase and out-of-phase output. Thus, for a −N line input, a −P in-phase output and a +P out-of-phase output result. It is used as follows:

1. To translate from an N to a P line.
2. To obtain a P line inversion of the input sign, i.e., a +N to −P or a −N to a +P.
3. As a current amplifier to drive other logic blocks.

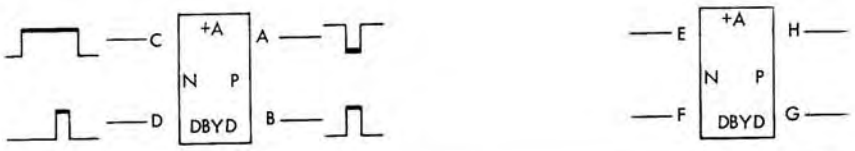
Circuit Description

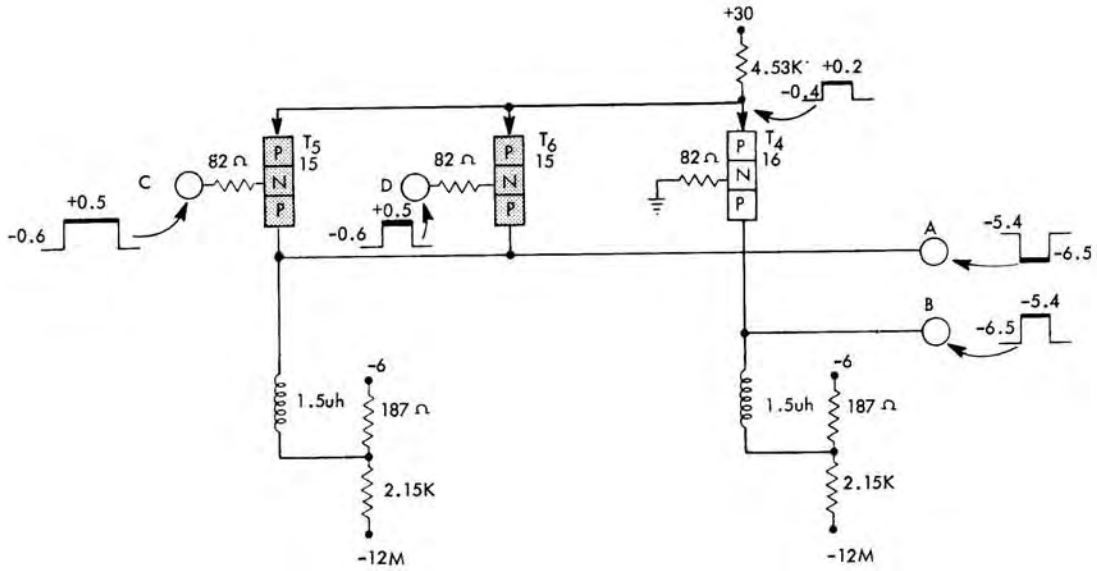
This circuit configuration is that of a one-way AND circuit, i.e., the input transistor T6 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a formed emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse bias T4, as shown. In this state, output B is at a −P level of −6.5v because of divider current through its coupling network, and output A is at a +P level of −5.1v owing to current flow (7.2ma) out of its coupling network through T6 to +6v.

When the input to T6 rises to a +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state, output B rises to a +P level because of current flow (6.3ma) out of its coupling network through T4 to +6v, and output A falls to a −P level because of divider current through its coupling network. The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v).

Application

For some applications, the circuit driven by this logic block requires a coupling network other than 243 ohm and 2.43K resistors shown. In such cases cap code ZX is used (see chart). This circuit is also used in DOT functions as a CO.





Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DBYD	1359	Yes	Note	+A	-O	+0.4 -0.4	See driver for max Output Levels	-5.6 -6.4	-5.2 -6.5	-5.6 -6.4	-5.1 -6.5	Min.	5.97	6.04	4	3
				+TA	-TO							Nom.	6.56	6.69	14	11
												Max.	7.14	7.34	23	21

Note: Output "A" has a network. Output "H" has no network

Diffused Junction Two-Way AND, Type B

The two-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of 2 +N inputs produces a +P in-phase output and a −P out-of-phase output.

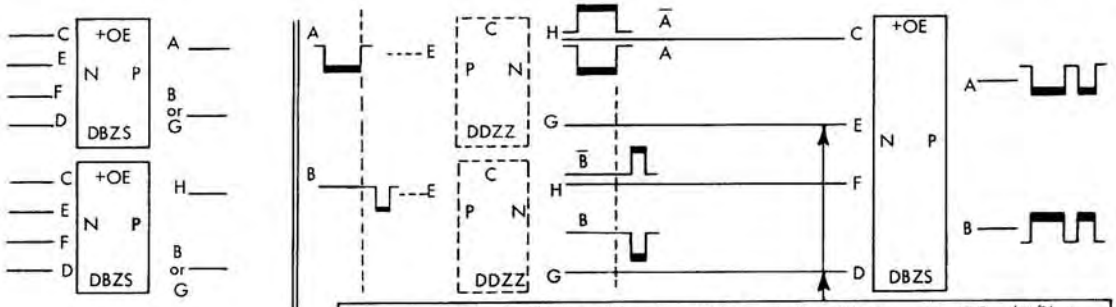
Circuit Description

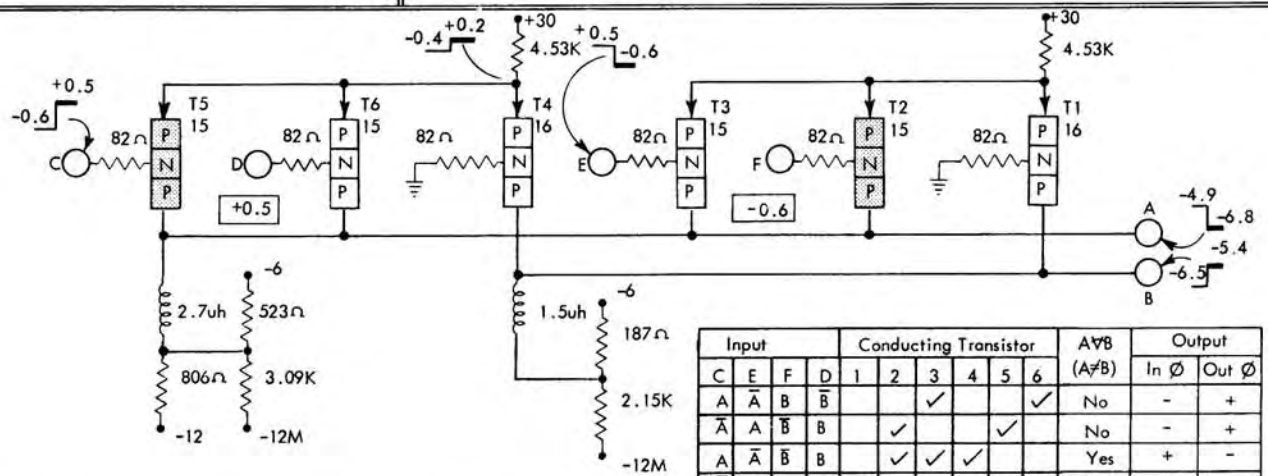
This circuit utilizes two transistors (T5 and T6) in an AND configuation similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (30v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output B is at a −P level of −6.5v because of divider current through its coupling network, and output A is at a +P level of −5.4v because of current flow (6.7ma) out of its coupling network through T5 and T6 to +30v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward biased and clamps to its base potential. In this state all input transistors are cut off so that output A falls to a −P level and output B rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohm to +6v) so that transistor parameters are less critical than in type A.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases output H (which has no coupling network) is used (see chart). This circuit is also combined with an OR circuit to make up a trigger.





Input				Conducting Transistor						A∀B	Output	
C	E	F	D	1	2	3	4	5	6	(A≠B)	In Ø	Out Ø
A	$\bar{A}$	B	$\bar{B}$			✓			✓	No	-	+
$\bar{A}$	A	$\bar{B}$	B		✓			✓		No	-	+
A	$\bar{A}$	$\bar{B}$	B		✓	✓	✓			Yes	+	-
$\bar{A}$	A	B	$\bar{B}$	✓				✓	✓	Yes	+	-

Card Code	Part No 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit used as		Input Levels Min.	Input Levels Max.	In-phase Output Min.	In-phase Output Max.	Out-phase Output Min.	Out-phase Output Max.	Ma. Output	In Ø	Out Ø (On)	Out Ø (Off)	musec block delay Turn On	musec block delay Turn Off
DBZS	1288	Yes	Yes	+OE		+0.4 -0.4	See driver for max. output levels	-5.6 -6.4	-5.2 -6.5	-5.6 -6.4	-4.2 -7.1	Min.	5.97	12.07	6.04	8	4
DBZR	1289	Yes	No									Nom.	6.59	13.40	6.75	15	9
DBZQ	1290	No	Yes									Max.	7.20	14.72	7.45	24	15
DBZP	1291	No	No														

Diffused Junction, Plus Exclusive OR

The +OE circuit is a special type of OR circuit. It develops a +P in-phase output and a −P out-of-phase output when an A∀B (read A exclusive OR B) statement is recognized at the input. This statement simply means A ≠B. In order to clarify what this means, the signal information-flow in the logic application above is described. First, two pieces of information, signals A and B, are passed through converters. These signals and their complements are mixed at the input of the +OE. Of these four inputs, the signals of two (either E and D or C and F) must be compared to establish if A≠B (See the note associated with inputs E and D).

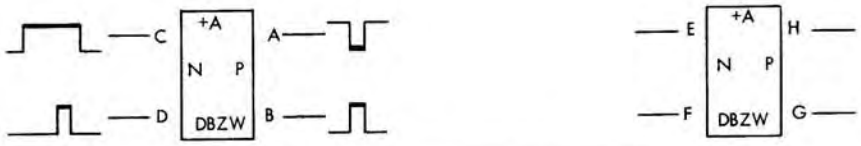
A check of the A and B signals shows that first A = B (the A∀B is not established) and output B is −P. Next A falls and B is still up so that A∀B exists and output B is +P. When A again rises, both A and B are up and output B is again −P. Finally B falls with A up and again A∀B is realized; output B is +P. Simply stated, the in-phase output follows the sign of the function for an A∀B input.

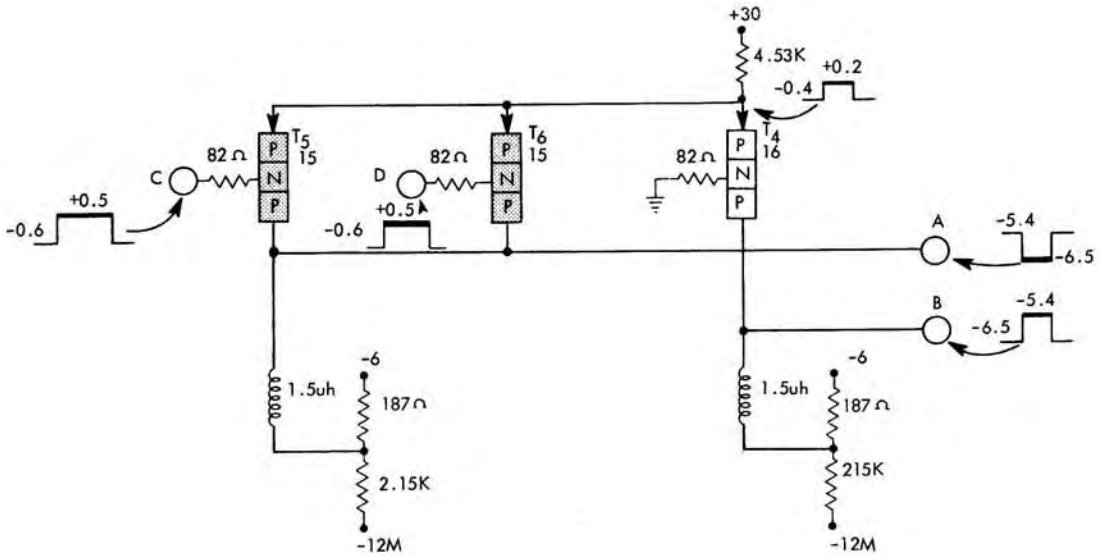
Circuit Description

In the state shown T5 and T2 are forward-biased and 13.4ma flows out of the 523 ohm, 806 ohm, 3.09K coupling network; 6.7ma flows through T5 to +30v, and 6.7ma flows through T2 to +30v. This current flow out of the network sets output A at a +P level of −4.9v. Divider current through the 187 ohm, 2.15K network establishes output B at a −P level of −6.5v.

Because a signal and its complement appear at two of the inputs, two signals switch simultaneously. Thus, input C rises, which forward-biases T4 and cuts off T5, while input E falls to forward-bias T3. In this state, 6.7ma flows out of the out-of-phase network through T3 and T2 to +30v. Thus, the current flow out of this network falls from 13.4ma to 6.7ma and output A falls to a −P level of −6.8v. Current out of the 187 ohm, 2.15K network flows through T4 to +30v and output B rises to a +P level of −5.4v.

If the signals to inputs D and F had been switched instead of the signal to C and F, the output levels would have switched as described above, only in this case T1 would conduct instead of T4.





Card Code	Part No. 37----	Clpg Network In Ø	Clpg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DBZW	1284	Yes	Yes	+A	-O	+0.4	See driver for max. Output Levels	-5.6	-5.2	-5.6	-5.1					
DBZV	1285	Yes	No	+AO	-OA	-0.4		-6.4	-6.5	-6.4	-6.5	Min.	5.97	6.04	4	3
DBZU	1286	No	Yes	+TA	-TO							Nom.	6.56	6.69	14	11
DBZT	1287	No	No									Max.	7.14	7.34	23	21

Diffused Junction Two-Way AND, Type B

The two-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of two +N inputs produces a +P in-phase output and a −P out-of-phase output.

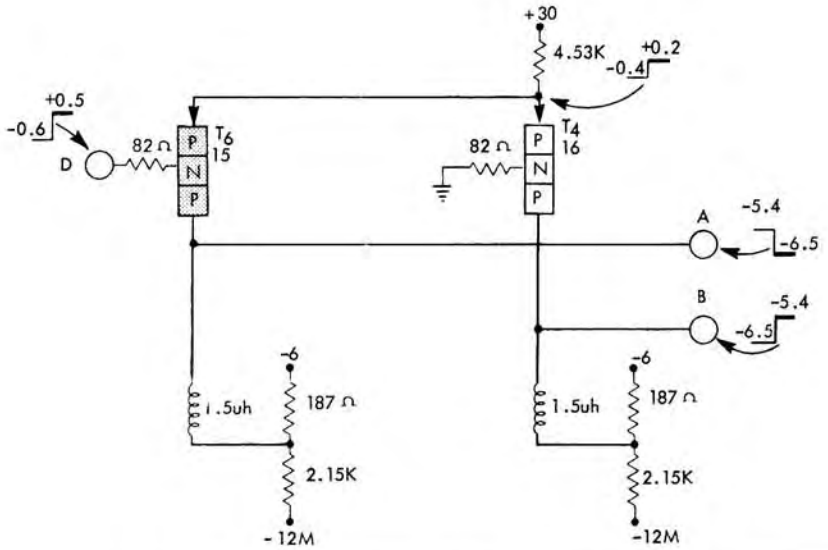
Circuit Description

This circuit uses two transistors (T5 and T6) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (30v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output B is at a −P level of −6.5v because of divider current through its coupling network, and output A is at a +P level of −5.4v because of current flow (6.7ma) out of its coupling network through T5 and T6 to +30v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output A falls to a −P level and output B rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical then in type A.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap codes ZT, ZU and ZV are used as required (see chart). This circuit is also combined with an OR circuit to make up a trigger, and with other AND circuit blocks to obtain DOT functions.



Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DBZZ	1292	Yes	Yes	C	CO	+0.4 / -0.4	See driver for max. Output Levels	-5.6 / -6.4	-5.2 / -6.5	-5.6 / -6.4	-5.1 / -6.5	Min.	5.97	6.04	3	4
DBZY	1293	Yes	No									Nom.	6.56	6.69	14	12
DBZX	1294	No	Yes									Max.	7.14	7.34	23	24
DB--	1295	No	No													

Diffused Junction N-to-P Converter, Type B

The N-to-P converter is a single input logic block. It is fed by an N line and produces both an in-phase and out-of-phase output. Thus, for a −N line input, a −P in-phase output and a +P out-of-phase output result. It is used as follows:

1. To translate from an N to a P line.
2. To obtain a P line inversion of the input sign, i.e., a +N to a −P or a −N to a +P.
3. As a current amplifier to drive other logic blocks.

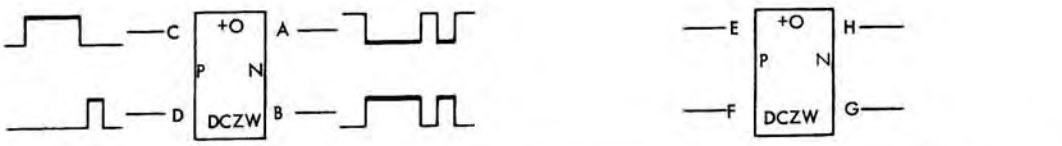
Circuit Description

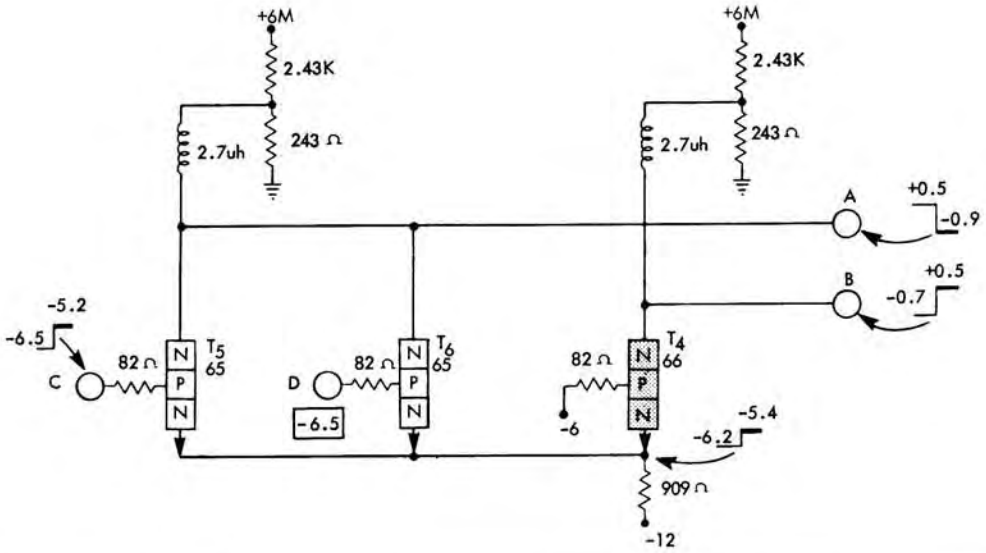
This circuit configuration is that of a one-way AND circuit; i.e., the input transistor T6 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output B is at a −P level of −6.5v because of divider current through its coupling network, and output A is at a +P level of −5.4v because of current flow (6.7ma) out of its coupling network through T6 to +30v.

When the input to T6 rises to a +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state, output B rises to a +P level because of current flow (6.6ma) out of its coupling network through T4 to +30v, and output A falls to a −P level because of divider current through its coupling network. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap codes ZX, ZY and - - are used as required (see chart). This circuit is also used in DOT functions as a CO.





Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuits Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DCZW	1296	Yes	Yes	+O	-A	-5.6	See driver for max. Output Levels	+0.4	+0.6	+0.4	+0.6	Min.	5.62	5.98	5	4
DCZU	1297	No	Yes	+OA	-AO	-6.4		-0.4	-1.1	-0.4	-1.4	Nom.	6.25	7.22	15	11
				+TO	-TA							Max.	6.87	8.46	25	19

Diffused Junction Two-Way OR, Type A

The two-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output.

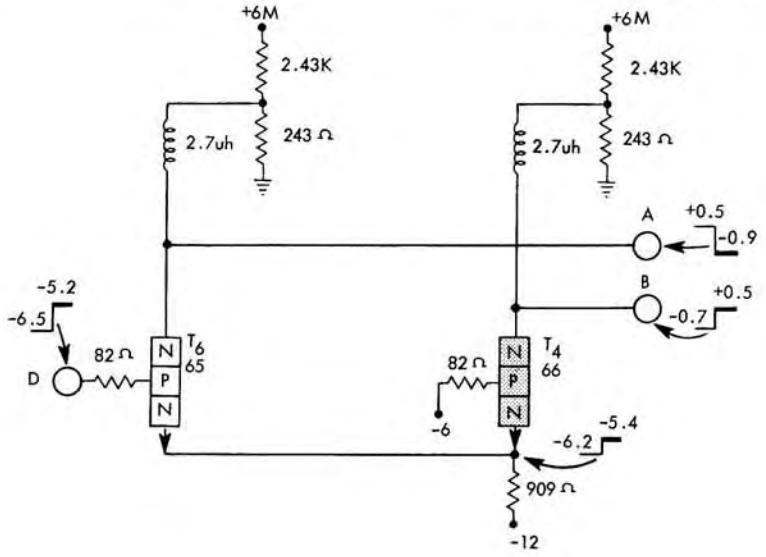
Circuit Description

This circuit uses two transistors (T5 and T6) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. In this state, all inputs are −P as shown, and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −0.7v because of current flow (6.3ma) through T4 into its coupling network. Output A is at a +N level of 0.5v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. Output B rises to a +N level because of divider current through its coupling network and output A falls to a −N level of −0.9v because of current flow (7.2ma) through the input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v).

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 243 ohm and 2.43K resistors shown. In such cases cap code ZU is used (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions.



Card Code	Part No 37----	Cplg Network		Circuit Used as		Input Levels		In Ø Output		Out Ø Output		Ma. Output			musec Block Delay	
		In Ø	Out Ø			Min.	Max.	Min.	Max.	Min.	Max.		In Ø	Out Ø	Turn On	Turn Off
DCZZ	1298	Yes	Yes	C	-CO	-5.6 / -6.4	See driver for max. Output Levels	+0.4 / -0.4	+0.6 / -1.1	+0.4 / -0.4	+0.6 / -1.4	Min.	5.62	5.98	4	4
DCZX	1299	No	Yes	CA								Nom.	6.25	7.22	14	12
												Max.	6.87	8.46	24	20

Diffused Junction P-to-N Converter, Type A

The P-to-N converter is a single input logic block. It is fed by a P line and produces both an in-phase and out-of-phase output. Thus, for a −P line input, a −N in-phase output and a +N out-of-phase output result. It is used as follows:

1. To translate from a P to an N line.
2. To obtain an N line inversion of the input sign, i.e., a +P to a −N or a −P to a +N.
3. As a current amplifier to drive other logic blocks.

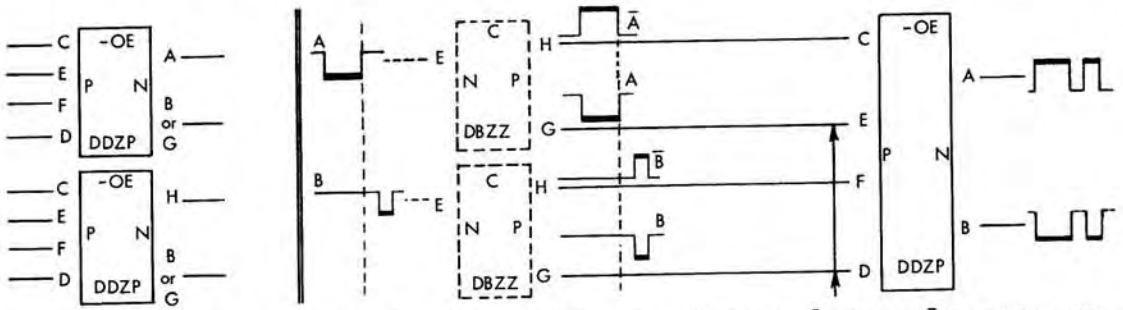
Circuit Description

This circuit configuration is that of a one-way OR circuit; i.e., the input transistor T6 has its base-to-emitter PN diode returned to a negative supply (−12v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −P level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −0.7v because of current flow (6.3ma) through T4 into its coupling network. Output A is at a +N level of 0.5v because of divider current through its coupling network.

When the input to T6 rises above −6v, the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output B rises to a +N level because of divider current through its coupling network and output A falls to a −N level of −0.9v because of current flow (7.2ma) through T6 into its coupling network. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v).

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 243 ohm and 2.43K resistors shown. In such cases, cap code ZX is used (see chart). This circuit is also used in DOT functions as a CA and a− CO.



Comparison of the in Ø inputs determines if the exclusive OR statement $[A \forall B = (A \neq B)]$ is established. When established, the in Ø output follows the sign of the function; i.e., the in Ø output is negative for a -OE when $A \neq B$

Input				Conducting Transistor						A∀B	Output	
C	E	F	D	1	2	3	4	5	6	(A≠B)	In Ø	Out Ø
A	Ā	B	B̄		✓			✓		No	+	-
Ā	A	B̄	B			✓			✓	No	+	-
A	Ā	B̄	B	✓				✓	✓	Yes	-	+
Ā	A	B	B̄		✓	✓	✓			Yes	-	+

Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used As		Input Levels Min.	Input Levels Max.	In-phase Output Min.	In-phase Output Max.	Out-phase Output Min.	Out-phase Output Max.
DDZS	1304	Yes	Yes	-OE		-5.6 to -6.4	See driver for max output levels	+0.4 to -0.4	+0.5 to -0.8	+0.4 to -0.4	+1.1 to -1.8
DDZR	1305	Yes	No								
DDZQ	1306	No	Yes								
DDZP	1307	No	No								

Ma Output	In Ø	Out Ø (on)	Out Ø (off)	musec Block Delay Turn On	Turn Off
Min.	5.97	12.07	6.04	7	5
Nom.	6.59	13.40	6.75	15	10
Max.	7.20	14.72	7.45	26	16

Diffused Junction, Minus Exclusive OR

The -OE circuit is a special type of OR circuit. It develops a -N in-phase output and a +N out-of-phase output when an A∀B (read A exclusive OR B) statement is recognized at the input. This statement simply means $A \neq B$. To clarify what this means, the signal information flow in the logic application above is described. First, two pieces of information, signals A and B, are passed through converters. These signals and their complements are mixed at the input of the -OE. Of these four inputs, the signals of two (either E and D or C and F) must be compared to establish if $A \neq B$. (See note, inputs E and D).

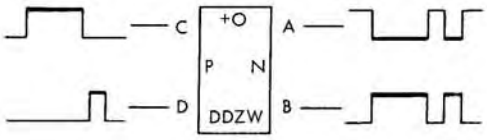
A check of the A and B signals shows that first A=B (A∀B is not established) and output B is +N. Next A falls and B is still up, so A∀B exists and output B is -N. When A again rises, both A and B are up and output B is again +N. Finally, B falls with A up and again A∀B is realized; output B is -N. Simply stated, the in-phase output follows the sign of the function for an A∀B input.

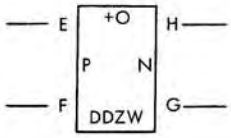
Circuit Description

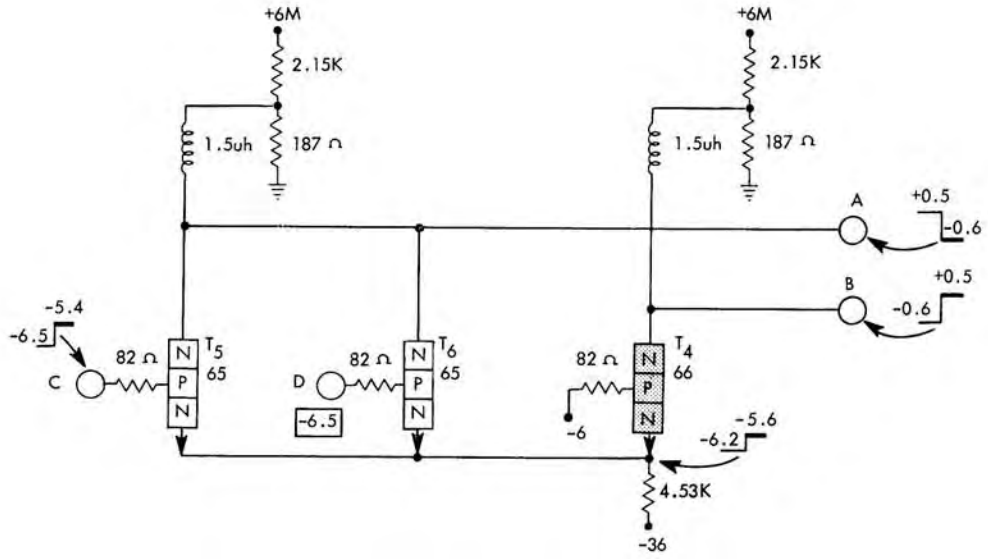
In the state shown, T6 and T3 are forward-biased. A current of 6.7ma flows from -36v through T6 into the 523 ohm, 806 ohm, 3.09K coupling network, and a similar current flows through T3. Thus, a combined current of 13.4ma flows into the coupling network, which establishes output A at a -N level of -1.1v. Divider current through the 187 ohm, 2.15K network establishes output B at a +N level of +0.5v.

Because a signal and its complement appear at two of the inputs, two signals switch simultaneously. Thus, input C rises and forward-biases T5 while E falls and forward-biases T1 and cuts off T3. In this state, 6.7ma flows from -36v through T5 and T6 into the coupling network. Thus, the current flow into the out-of-phase network falls from 13.4ma to 6.7ma and output A rises to a +N level of +0.8v. Current flow from -36v through T1 into the 187 ohm, 2.15K network causes output B to fall to a -N level.

If the signal to inputs D and F had been switched instead of the signal to C and F, the output levels would have switched as described above, only in this case, T4 would conduct instead of T1.







Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DDZW	1300	Yes	Yes	+O	-A	-5.6	See driver for max. Output Levels	+0.4	+0.5	+0.4	+0.5					
DDZV	1301	Yes	No	+OA	-AO	-6.4		-0.4	-0.8	-0.4	-0.9	Min.	5.97	6.04	5	4
DDZU	1302	No	Yes	+TO	-TA							Nom.	6.56	6.69	15	11
DDZT	1303	No	No									Max.	7.14	7.34	25	19

Diffused Junction Two-Way OR, Type B

The two-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output.

Circuit Description

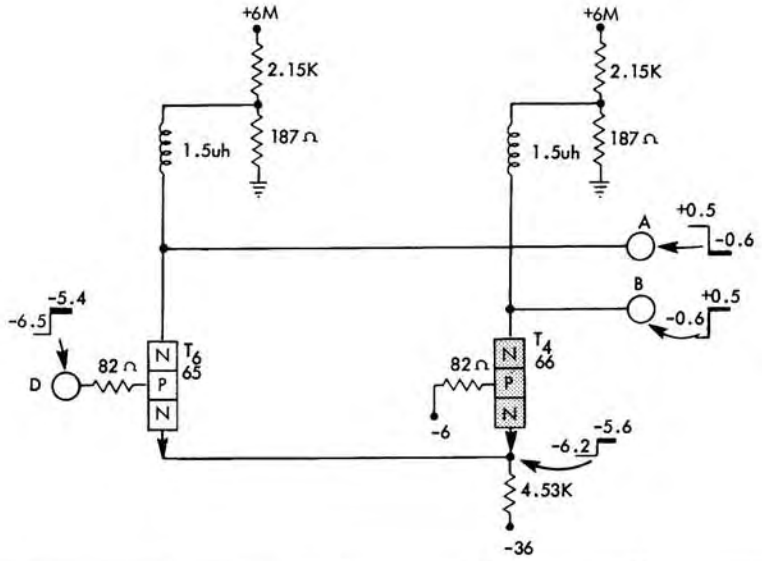
This circuit uses two transistors (T5 and T6) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−36v). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. All inputs are −P as shown and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward biased and clamps to the base potential of −6v.

Output B is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network. Output A is at a +N level of +0.5v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output B rises to a +N level because of divider current through its coupling network, and output A falls to a −N level because of current flow (6.7ma) through an input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-ware response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v) so that transistor parameters are less critical than in type A.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap codes ZT, ZU and ZV are used as required (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions.



Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DDZZ	1308	Yes	Yes	C	-CO	-5.6	See driver for max. Output Levels	+0.4	+0.5	+0.4	+0.5					
DDZY	1309	Yes	No	CA								Min.	5.97	6.04	4	4
DDZX	1310	No	Yes			-6.4		-0.4	-0.8	-0.4	-0.9	Nom.	6.56	6.09	14	12
DD--	1311	No	No									Max	7.14	7.34	24	20

Diffused Junction P-to-N Converter, Type B

The P-to-N converter is a single input logic block. It is fed by a P line and produces both an in-phase and out-of-phase output. Thus, for a −P line input, a −N in-phase output and a +N out-of-phase output result. It is used as follows:

1. To translate from a P to an N line.
2. To obtain an N line inversion of the input sign; i.e., a +P to a −N or a −P to a +N.
3. As a current amplifier to drive other logic blocks.

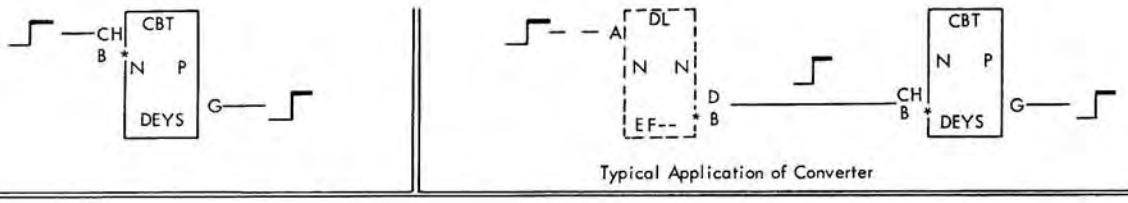
Circuit Description

This circuit configuration is that of a one-way OR circuit; i.e., the input transistor T6 has its base-to-emitter PN diode returned to a negative supply (−36v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −P level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network. Output A is at a +N level of 0.5v because of divider current through its coupling network.

When the input to T6 rises above −6v, the emitter line follows it and T4 is reverse biased and cuts off. In this state, output B rises to a +N level because of divider current through its coupling network and output A falls to a −N level of −0.6v because of current flow (6.7ma) through T6 into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v) so that transistor parameters are less critical than for type A.

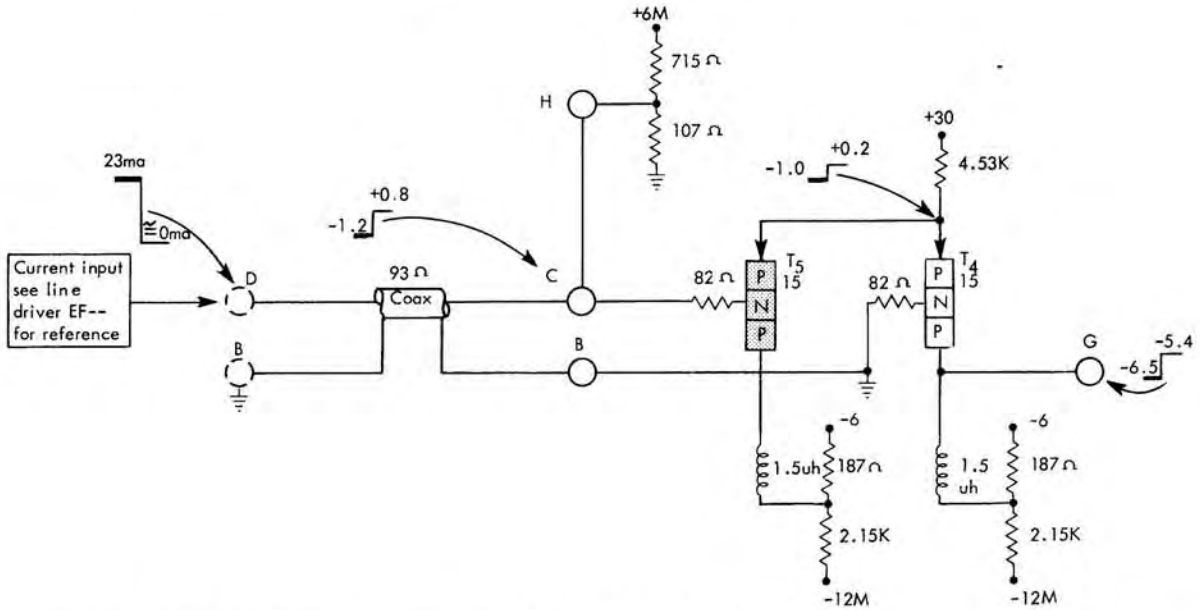
Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases, cap codes ZX, ZY and - - are used as required (see chart). This basic circuit is also used in DOT functions as a CA and a −CO.



Typical Application of Converter

DEYR YS



Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	T5 Collector Min.	T5 Collector Max.	Ma. Output	In Ø	T5	musec Block Delay Turn On	musec Block Delay Turn Off
DEYS	1328	Yes	Yes	CBT		+0.4	See driver for max. Output Levels	-5.2	-6	-5.1	-5.6	Min.	5.97	6.04	3	4
DEYR	1329	No	Yes			-0.4		-6.4	-6.5	-6.4	-6.5	Nom.	6.56	6.69	14	12
												Max.	7.14	7.34	23	24

Diffused Junction N-to-P Terminator-Buffer-Converter

This circuit is designed to terminate a coaxial line and to provide an in-phase P-line output for an N-line input. The input circut has a coupling network whose equivalent resistance is 93 ohms. This network terminates the coaxial line in its characteristic impedance and converts input current to N line signal levels.

Circuit Description

This circuit configuration is that of a one-way AND circuit; i.e., the input transistor T5 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network.

When the input to T5 rises to +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward biased and clamps to its base potential. In this state, output G rises to a +P level of −5.4v because of current flow (6.6ma) out of its coupling network through T4 to +30v.

The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, the line driver is supplying 23ma of current into the network to develop a −N level of −1.2v. When the input current is reduced to zero, divider current through the network establishes the +N level.

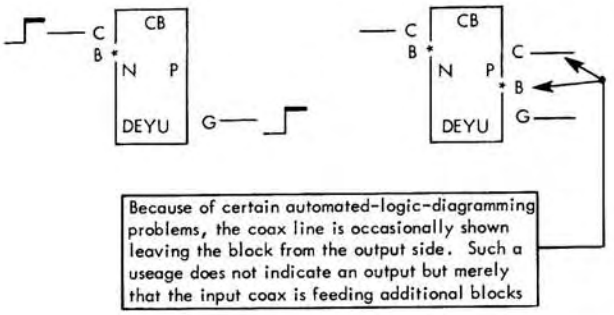
The peaking coil compensates for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor that is necessary because of the inductive coupling networks used.

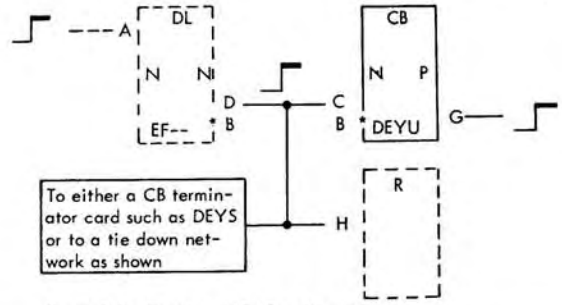
This circuit is essentially a differential amplifier so that if unwanted power line signals are induced in the coaxial line these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals appear at input B and C in-phase and cancellation results.

Application

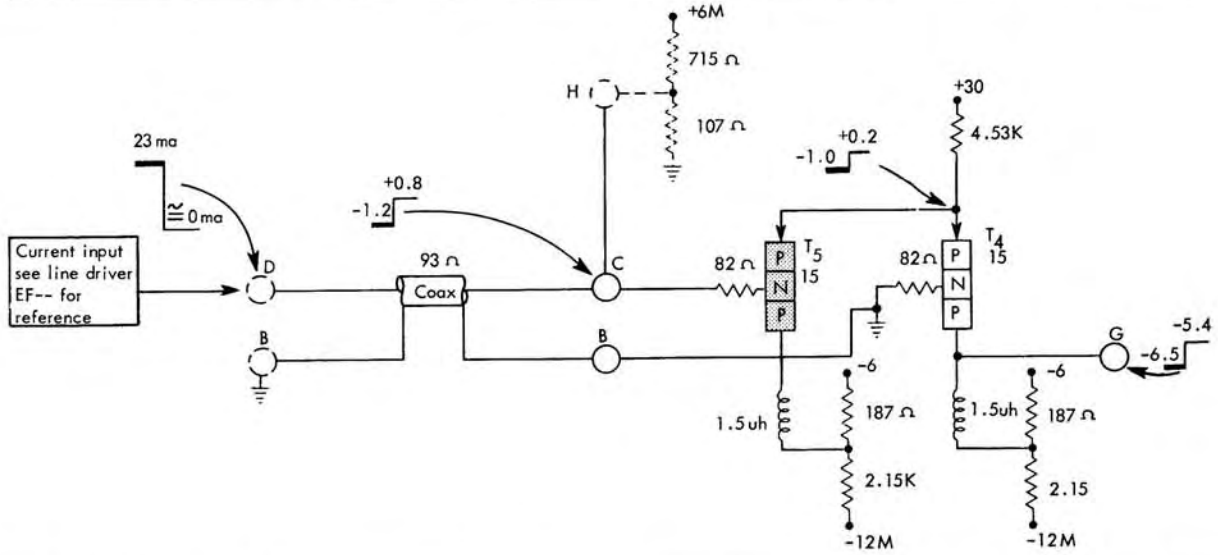
For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap code YR is used (see chart).

DEYT
YU





Typical Application of Buffer Converter



Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	T_5 Collector Min.	T_5 Collector Max.
DEYU	1326	Yes	Yes	CB		+0.4 / -0.4	See driver for max. Output Levels	-5.6 / -6.4	-5.2 / -6.5	-5.6 / -6.4	-5.1 / -6.5
DEYT	1327	No	Yes								

Ma. Output	In Ø	T_5	musec Block Delay Turn On	Turn Off
Min.	5.97	6.04	3	4
Nom.	6.56	6.69	14	12
Max.	7.14	7.34	23	24

Diffused Junction N-to-P Buffer Converter

This circuit is designed to act as a buffer stage between a line driver and local logic blocks. It accepts an N line input and provides an in-phase P line output. A CB circuit does not provide a termination for the line driver because several of these circuits are usually driven by the same driver. Therefore, a CBT block or an R block must be tied to the output of the line driver to terminate it and to develop N line signal levels.

Circuit Description

This circuit configuration is that of a one-way AND circuit; i.e., the input transistor T5 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network.

When the input to T5 rises to a +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state, output G rises to a +P level of −5.4v because of current flow (6.6ma) out of its coupling network through T4 to +30v.

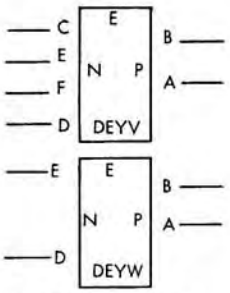
The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, the line driver is supplying 23ma of current into the network to develop a −N level of −1.2v. When the input current is reduced to zero, divider current through the network establishes the +N level.

The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used.

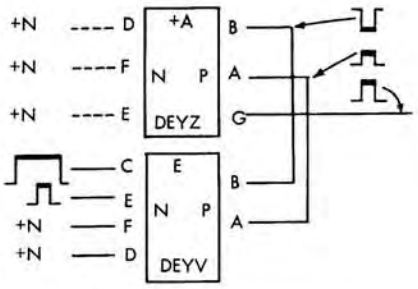
This circuit is essentially a differential amplifier so that, if unwanted power line signals are induced in the coaxial line these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals appear at input B and C in-phase and cancellation results.

Application

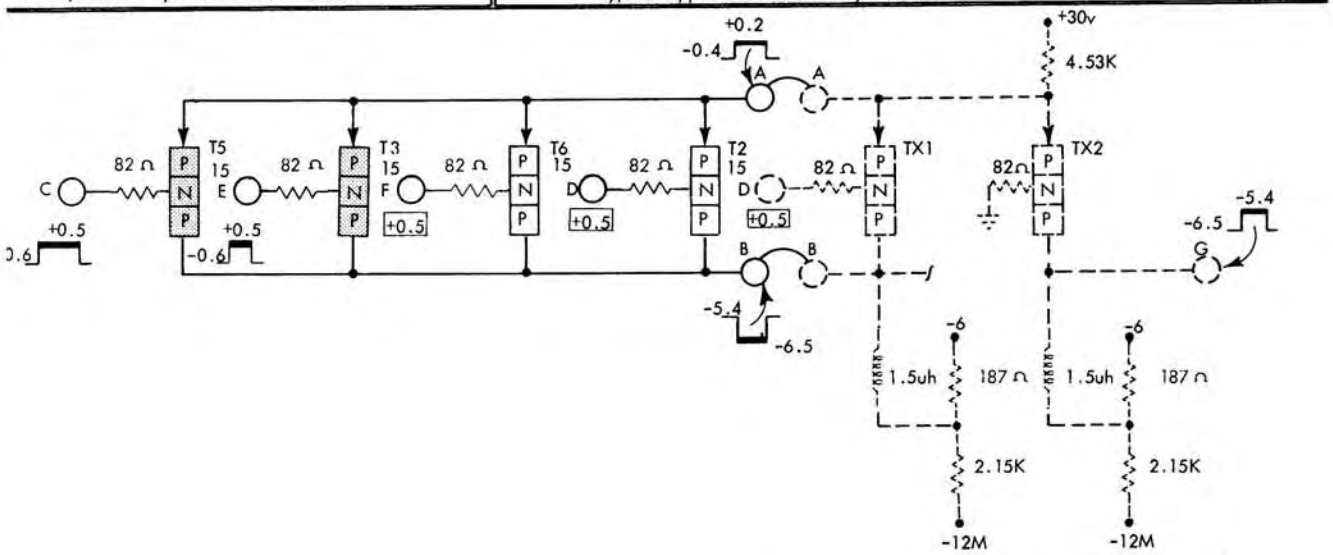
For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm, 2.15K resistors shown. In such cases cap code YT is used (see chart).



2-Way and 4-Way AND-Block Extenders



Typical Application of a 4-Way Extender



Card Code	Part No 37----	No of Inputs	Circuit Used as	Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
DEYV	1318	4	AND-Block Extender	+0.4 -0.4	See driver for max output Levels	-5.6 -6.4	-5.2 -6.5	-5.6 -6.4	-5.1 -6.5
DEYW	1325	2							

ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
Min.	5.97	6.04	8	4
Nom.	6.56	6.69	15	9
Max.	7.14	7.34	24	15

iffused Junction Two-Way and Four-Way AND Block Extenders

his type of extender card is used in combination with an ND circuit to increase the number of input legs to the AND. s shown above, a 3-way AND is increased to a 7-way AND / using the four-way extender DEYV. Had the two-way :tender DEYW been used, the three-way AND would be creased to a five-way AND. In logic, the circuit above orks as a seven-way AND, which means that the +AND inction is satisfied only when all seven inputs are positive. s in any +AND circuit, the in-phase output (G) follows ıe sign of the function and is positive when all inputs are ɔsitive. If the —OR function is desired, the in-phase out-ıt is negative for any negative input.

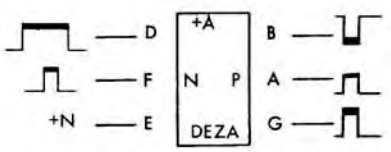
ircuit Description

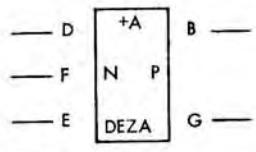
The extender increases the number of inputs by con-ɛcting, in parallel with the input transistors of the AND rcuit, additional input transistors. For example, in the rcuit above, back panel wiring A-A and B-B connects T5, 3, T6 and T2 in parallel with TX1 of the AND circuit card DEYZ. Any —N input (see input C and E) forward-biases an input transistor and the emitter line clamps within 0.2v to the input potential. With the emitter at 0.4v as shown, TX2 is reverse-biased and output G is at a —P level of —6.5v because of divider current through its coupling network; output B is at a +P level of —5.4v because of current flow (6.7ma.) out of its coupling network through T5 and T3 to +30v.

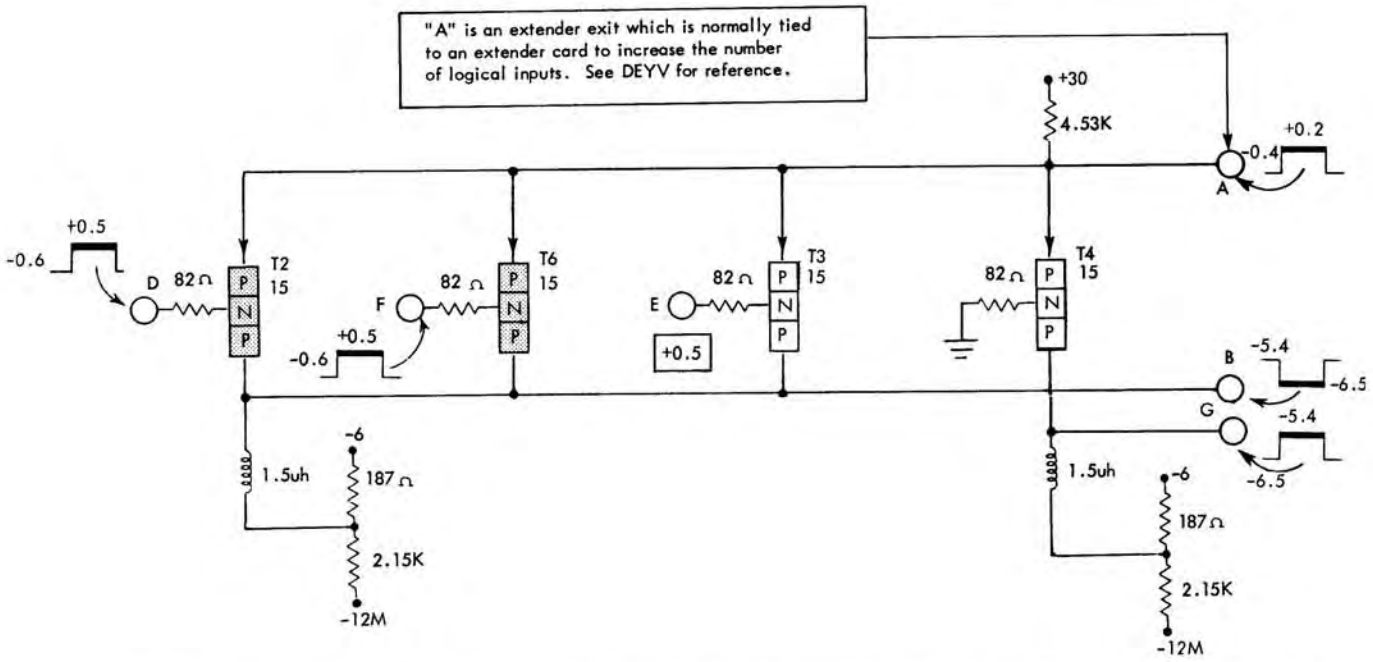
When all inputs are positive, the emitter of TX2 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off, so that output B falls to a —P level and output G rises to a +P level because TX2 is conducting.

Application

Extenders are used as +A block extenders or —OR block extenders.







Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DEZA	1321	Yes	Yes	+A	-O	+0.4	See driver for max. Output Levels	-5.6	-5.2	-5.6	-5.1					
DEYZ	1322	Yes	No	+AO	-OA							Min.	5.97	6.04	6	3
DEYY	1323	No	Yes	+TA	-TO	-0.4		-6.4	-6.5	-6.4	-6.5	Nom.	6.56	6.69	14	10
DEYX	1324	No	No									Max.	7.14	7.34	24	18

Diffused Junction Three-Way AND, Type B

The three-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of three +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit.

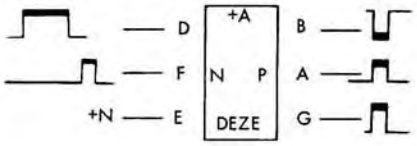
Circuit Description

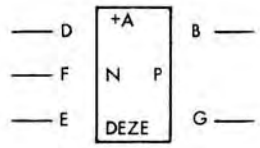
This circuit uses three transistors (T2, T6 and T3) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (30v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network, and output B is at a +P level of −5.4v because of current flow (6.7ma) out of its coupling network through T2 and T6 to +30v.

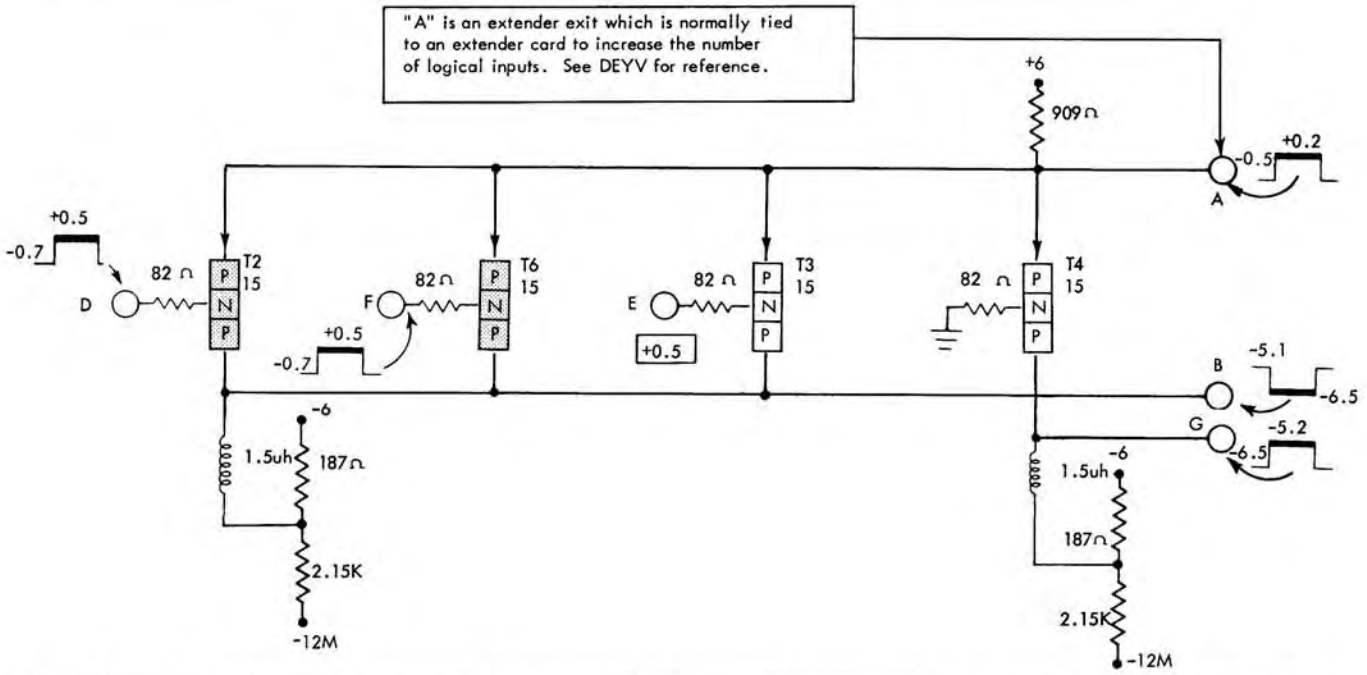
When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a −P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap codes YX, YY and YZ are used as required (see chart). This circuit is also combined with an OR circuit to make up a trigger, and with other AND circuit blocks to obtain DOT functions.







Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DEZE	1319	Yes	Yes	+A	-O	+0.4 -0.4	See driver for max. Output Levels	-5.6 -6.4	-4.9 -6.6	-5.6 -6.4	-4.6 -6.6	Min.	5.62	5.98	6	3
DEZC	1320	No	Yes	+AO	-OA							Nom.	6.25	7.22	14	10
				+TA	-TO							Max.	6.87	8.46	24	18

Diffused Junction Three-Way AND, Type A

The three-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of three + inputs produces a +P in-phase and a −P out-of-phase output. Output A is an extender exit.

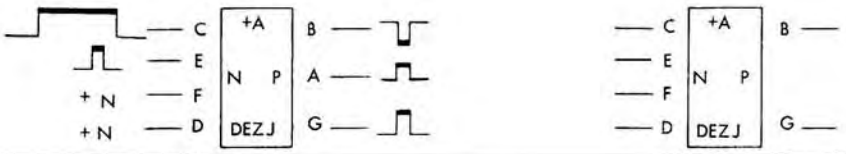
Circuit Description

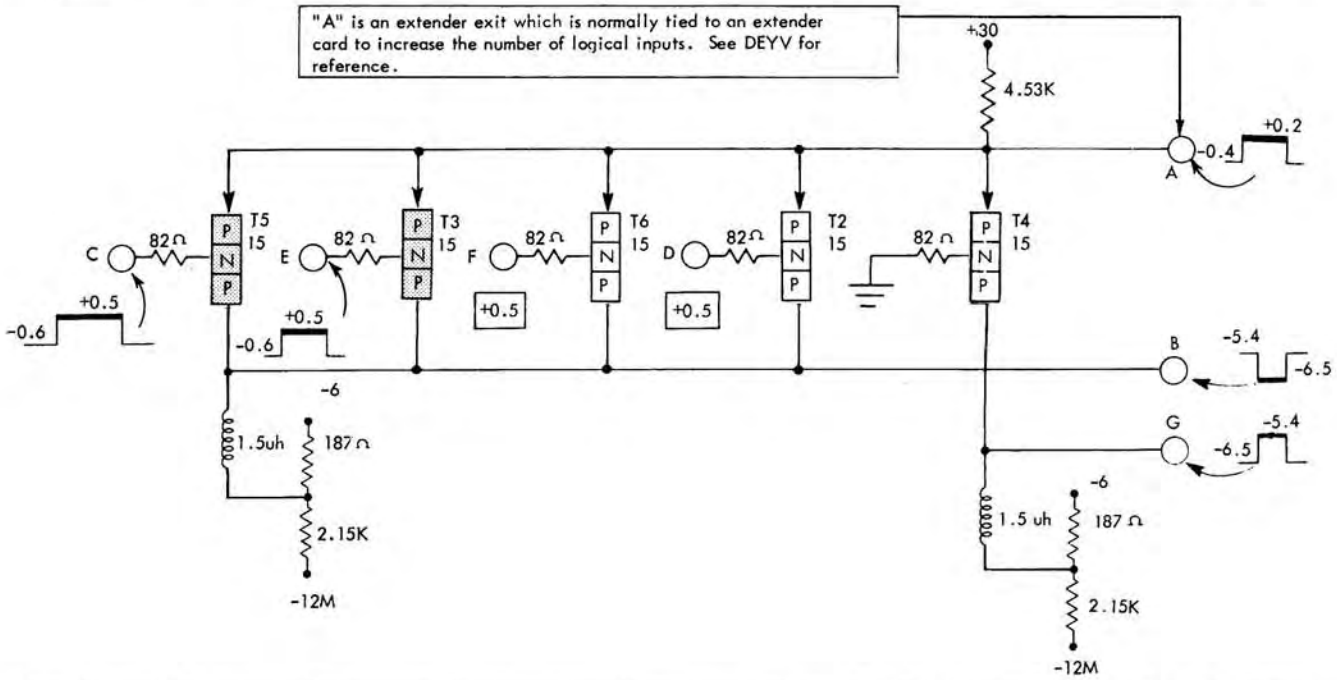
This circuit uses three transistors (T2, T6 and T3) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (6v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network, and output B is at a +P because of current flow (7.2ma) out of its coupling network through T2 and T6 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a −P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit because it provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v).

Application

For some applications, the circuit driven by this logic block requires a special input coupling network. In such cases cap code ZC is used (see chart). This circuit is also combined with an OR circuit to make up a trigger, and with other AND circuit blocks to obtain DOT functions.





Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DEZJ	1314	Yes	Yes	+A	-O	+0.4 -0.4	See driver for max Output Levels	-5.6 -6.4	-5.2 -6.5	-5.6 -6.4	-5.1 -6.5					
DEZH	1315	Yes	No	+AO	-OA							Min.	5.97	6.04	8	4
DEZG	1316	No	Yes	+TA	-TO							Nom.	6.56	6.69	15	9
DEZF	1317	No	No									Max.	7.14	7.34	24	15

Diffused Junction Four-Way AND, Type B

The four-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of four +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit.

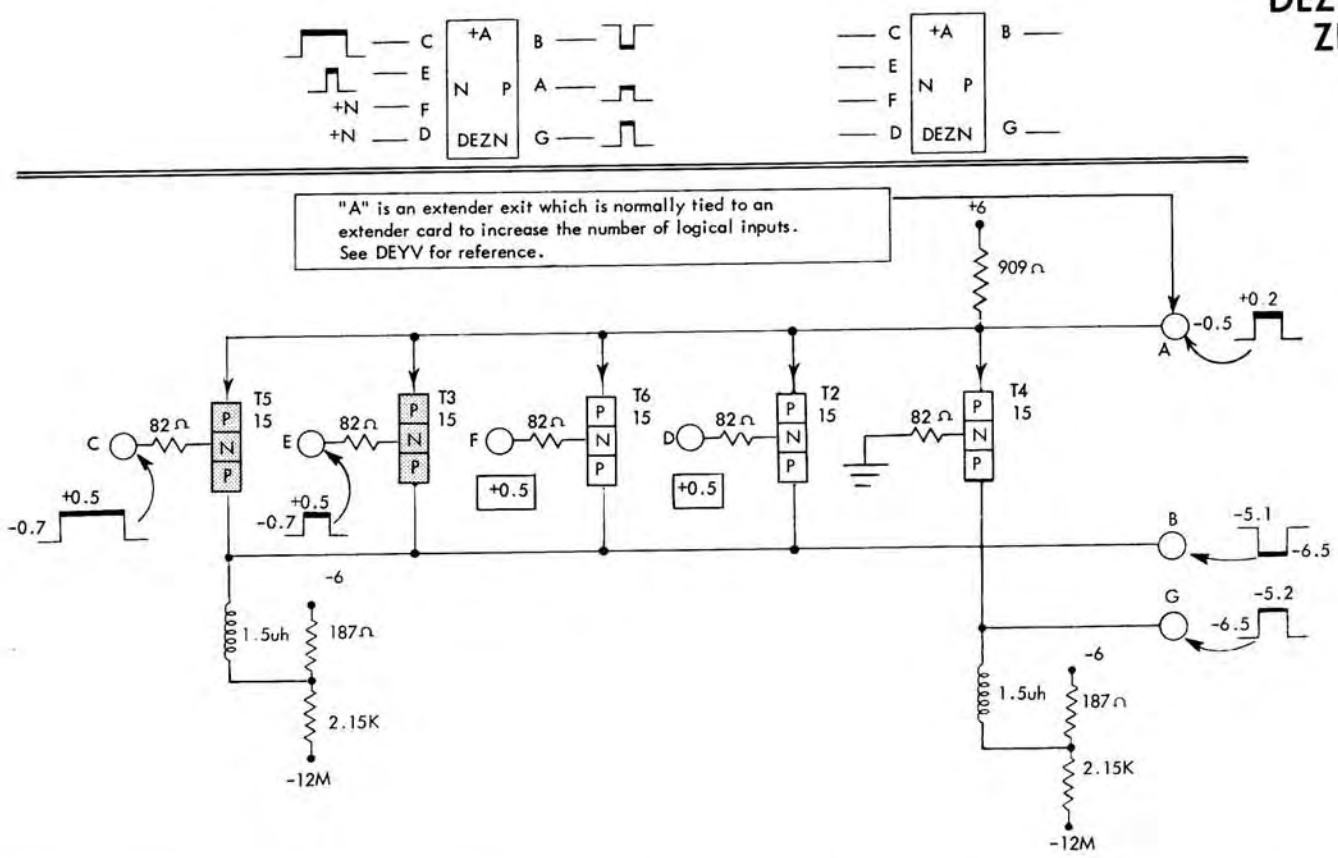
Circuit Description

This circuit uses four transistors (T5, T3, T6, and T2) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (30v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network, and output B is at a +P because of current flow (6.7ma) out of its coupling network through T5 and T3 to +30v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a −P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical.

Application

For some applications, the circuit driven by this logic block requires a special input coupling network. In such cases cap diodes ZF, ZG and ZH are used as required. This circuit is also combined with an OR circuit to make up a trigger, and with other AND blocks to obtain DOT functions.



Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
DEZN	1312	Yes	Yes	+A	-O	+0.4 / -0.4	See driver for max Output Levels	-5.6 / -6.4	-4.9 / -6.6	-5.6 / -6.4	-4.6 / -6.6
DEZL	1313	No	Yes	+AO	-OA						
				+TA	-TO						

Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	Turn Off
Min.	5.62	5.98	8	4
Nom.	6.25	7.22	15	2
Max.	6.87	8.46	24	15

Diffused Junction Four-Way AND, Type A

The four-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

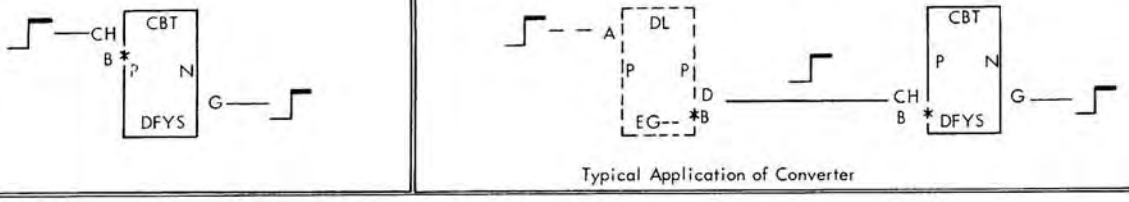
The AND circuit logic block shows that the coincidence of four +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit.

Circuit Description

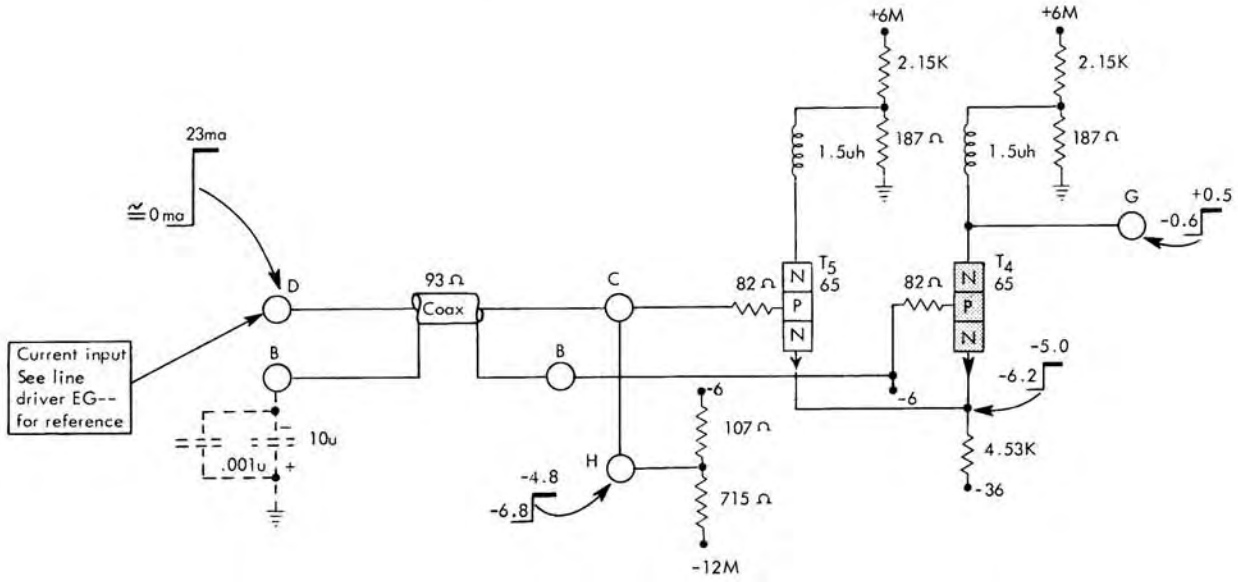
This circuit uses four transistors (T5, T3, T6 and T2) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (6v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network, and output B is at a +P because of current flow (7.2ma) out of its coupling network through T5 and T3 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a −P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v).

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap code ZL is used (see chart). This circuit is also combined with an OR circuit to make up a trigger, and with other AND circuit blocks to obtain DOT functions.



Typical Application of Converter



Card Code	Part No. 37 ----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	T5 Collector Min.	T5 Collector Max.
DFYS	1347	Yes	Yes	CBT		-5.6 / -6.4	See driver for max. Output Levels	+0.4 / -0.4	+0.5 / -0.8	+0.4 / -0.4	+0.5 / -0.9
DFYR	1348	No	Yes								

Ma. Output	In Ø	T_5	musec Block Delay Turn On	Turn Off
Min.	5.97	6.04	4	4
Nom.	6.56	6.69	14	12
Max.	7.14	7.34	24	20

Diffused Junction P-to-N Terminator-Buffer-Converter

This circuit is designed to terminate a coaxial line and to provide an in-phase N-line output for a P-line input. The input circuit has a coupling network whose equivalent resistance is 93 ohms. This network terminates the coaxial line in its characteristic impedance and converts input current to P-line signal levels.

Circuit Description

This circuit configuration is that of a one-way OR circuit; i.e., the input transistor T5 has its base-to-emitter PN diode returned to a negative supply (−36v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −P level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output G is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network.

When the input to T5 rises above −6v, the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +4 level because of divider current through its coupling network.

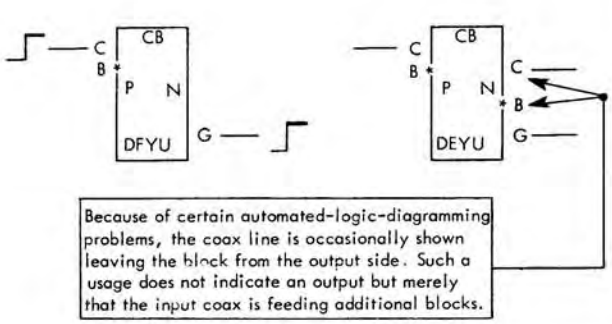
The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, input current is zero and the −N level is established by the network divider current. When the line driver circuit is switched on, 23ma flows from the network to the driver and the input signal rises to a +N level of −4.8v.

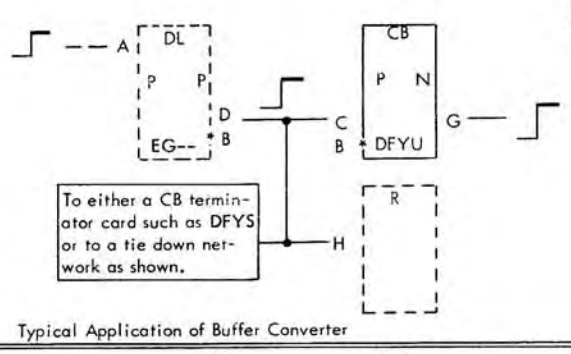
The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling network used.

This circuit is essentially a differential amplifier so that if unwanted power line signals are induced in the coaxial line, these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals reach B and C in-phase and cancellation results.

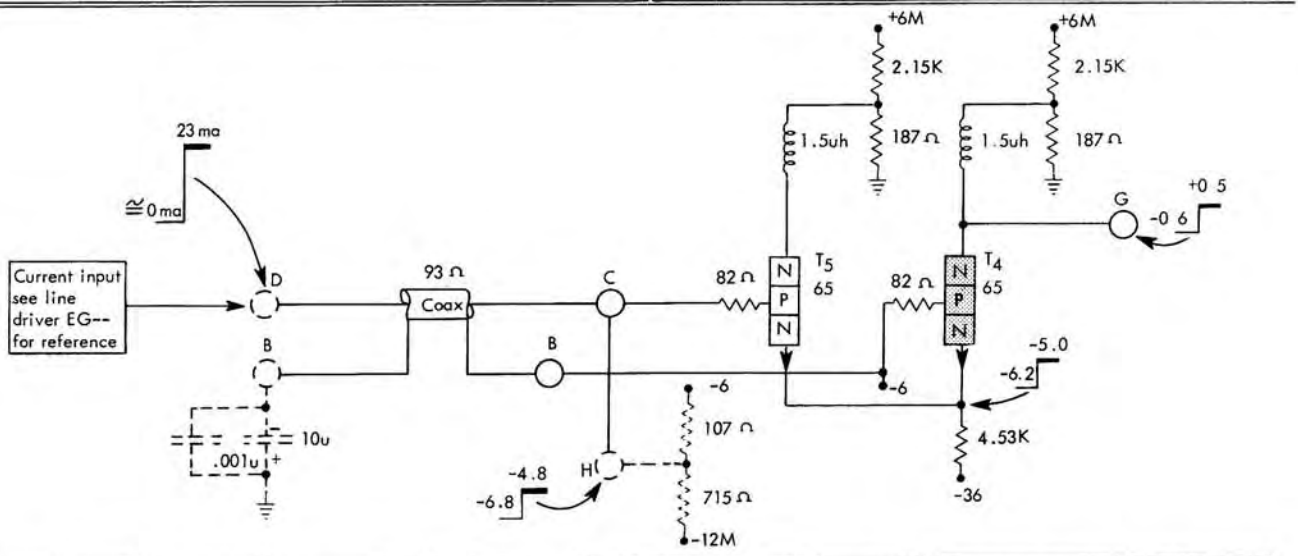
Application

For some applications, the circuit driven by this logic block requires a special input coupling network. In such cases, cap code YR is used (see chart).





Typical Application of Buffer Converter



Card Code	Part No 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	T_5 Collector Min.	T_5 Collector Max.	Ma. Output	Ma. Output In Ø	Ma. Output T_5	musec Block Delay Turn On	musec Block Delay Turn Off
DFYU	1345	Yes	Yes	CB		-5.6 / -6.4	See driver for max. Output Levels	+0.4 / -0.4	+0.5 / -0.8	+0.4 / -0.4	+0.5 / -0.9	Min.	5.97	6.04	4	4
DFYT	1346	No	Yes									Nom.	6.56	6.69	14	12
												Max.	7.14	7.34	24	20

Diffused Junction P-to-N Buffer Converter

This circuit is designed to act as a buffer stage between a line driver and local logic blocks. It accepts a P-line input and provides an in-phase N-line output. A CB circuit does not provide a termination for the line driver because several of these circuits are usually driven by the same driver. Therefore, a CBT block or an R block must be tied to the output of the line driver to terminate it.

Circuit Description

This circuit configuration is that of a one-way OR circuit; i.e., the input transistor T5 has its base-to-emitter PN diode returned to a negative supply (−36v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −6 level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output G is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network.

When the input to T5 rises above −6v, T4 is reverse-biased and cuts off. Output G rises to a +N level because of divider current through its coupling network.

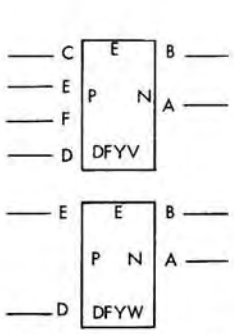
The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, input current is zero and the −N level is established by the network divider current. When the line driver circuit is switched on, 23ma flows from the network to the driver and the input signal rises to a +N level of −4.8v.

The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling network used.

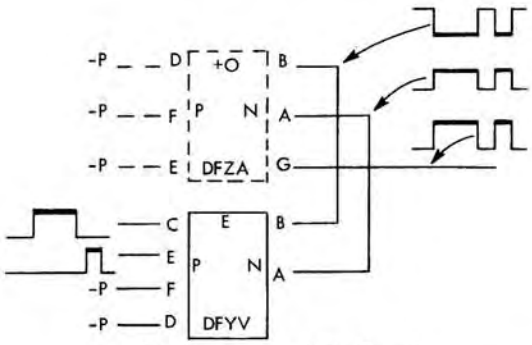
This circuit is essentially a differential amplifier so that, if unwanted power line signals are induced in the coaxial line, these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals appear at input B and C in-phase, and cancellation results.

Application

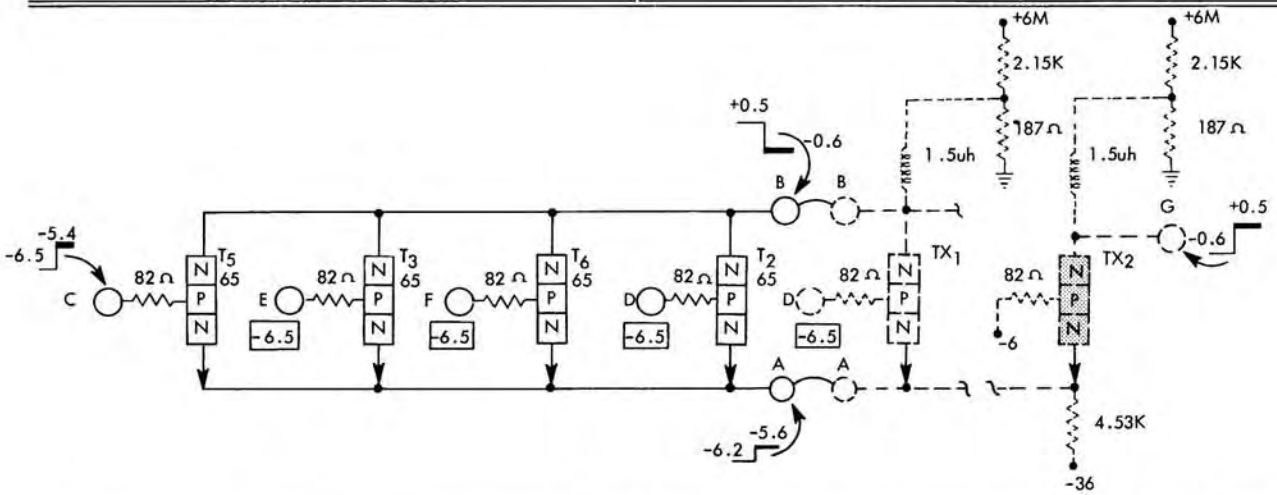
For some applications, the circuit driven by this logic block requires a special input coupling network. In such cases, cap code YT is used (see chart).



2-Way and 4-Way OR-Block Extenders



Typical Application of a 4-Way Extender



Card Code	Part No. 37----	No. of Inputs	Circuits Used as	Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DFYV	1336	4	OR-Block Extender	-5.6 / -6.4	See driver for max. Output Levels	+0.4 / -0.4	+0.5 / -0.8	+0.4 / -0.4	+0.5 / -0.9	Min.	5.97	6.04	7	5
DFYW	1344	2								Nom.	6.56	6.69	15	10
										Max.	7.14	7.34	26	16

Diffused Junction Two-Way and Four-Way OR-Block Extenders

This type of extender card is used in combination with an OR circuit to increase the number of input legs to the OR. As shown above, a three-way OR is increased to a seven-way OR by using the four-way extender DFYV. Had the two-way extender DFYW been used, the three-way OR would be increased to a five-way OR. The circuit above works as a seven-way OR, which means that the +OR function is satisfied when any of seven inputs is positive. As in any +OR circuit, the in-phase output (G) follows the sign of the function and is positive when any input is positive. If the —AND function is desired, the in-phase output is negative when all inputs are negative.

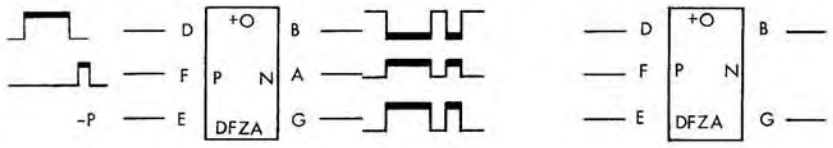
Circuit Description

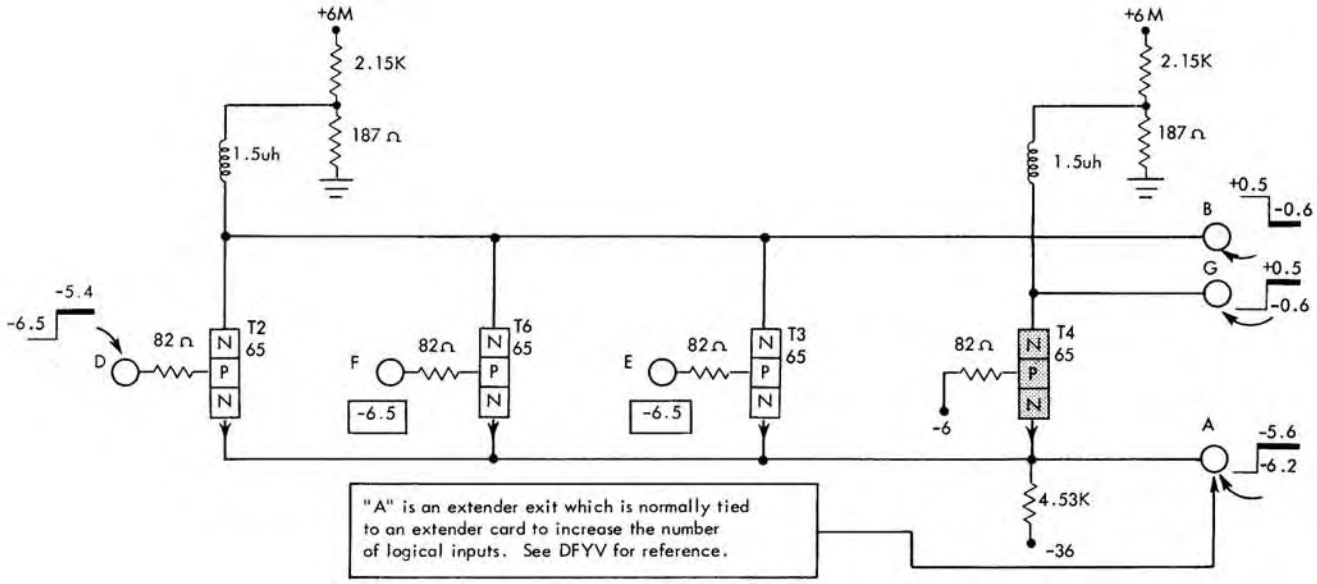
The extender increases the number of inputs by connecting additional input transistors in parallel with the input transistors of the OR circuit. For example, in the circuit above, back panel wiring A-A and B-B connects T5, T3, T6 and T2 in parallel with TX1 of the OR circuit card DFZA. When all inputs are at a —P as shown, the emitter line attempts to fall to the —P level. When the emitter of TX2 falls below —6v it becomes forward-biased and clamps to its base potential of —6v. Output G is at a —N level of —0.6v because of current flow (6.6ma) through TX2 into its coupling network. Output B is at a +N level of +0.5v because of divider current through its coupling network.

When any input rises above —6v (see input C) the emitter line follows it and TX2 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a —N level of —0.6v because of current flow (6.7ma) through an input transistor into its coupling network.

Application

Extenders are used as +OR block extenders or —AND block extenders.





Card Code	Part No 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DFZA	1340	Yes	Yes	+O	-A	-5.6 / -6.4	See driver for max Output Levels	+0.4 / -0.4	+0.5 / -0.8	+0.4 / -0.4	+0.5 / -0.9					
DFYZ	1341	Yes	No	+OA	-AO							Min.	5.97	6.04	6	4
DFYY	1342	No	Yes	+TO	-TA							Nom.	6.56	6.69	15	11
DFYX	1343	No	No									Max.	7.14	7.34	25	18

Diffused Junction Three-Way OR, Type B

The three-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output. Output A is an extender exit.

Circuit Description

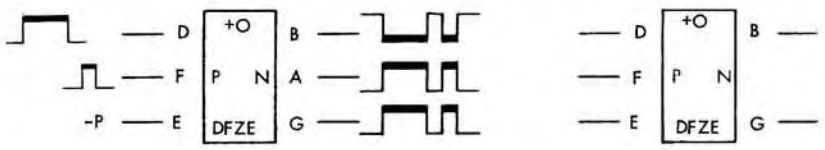
This circuit uses three transistors (T2, T6 and T3) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−36v). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. All inputs are −P as shown and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v.

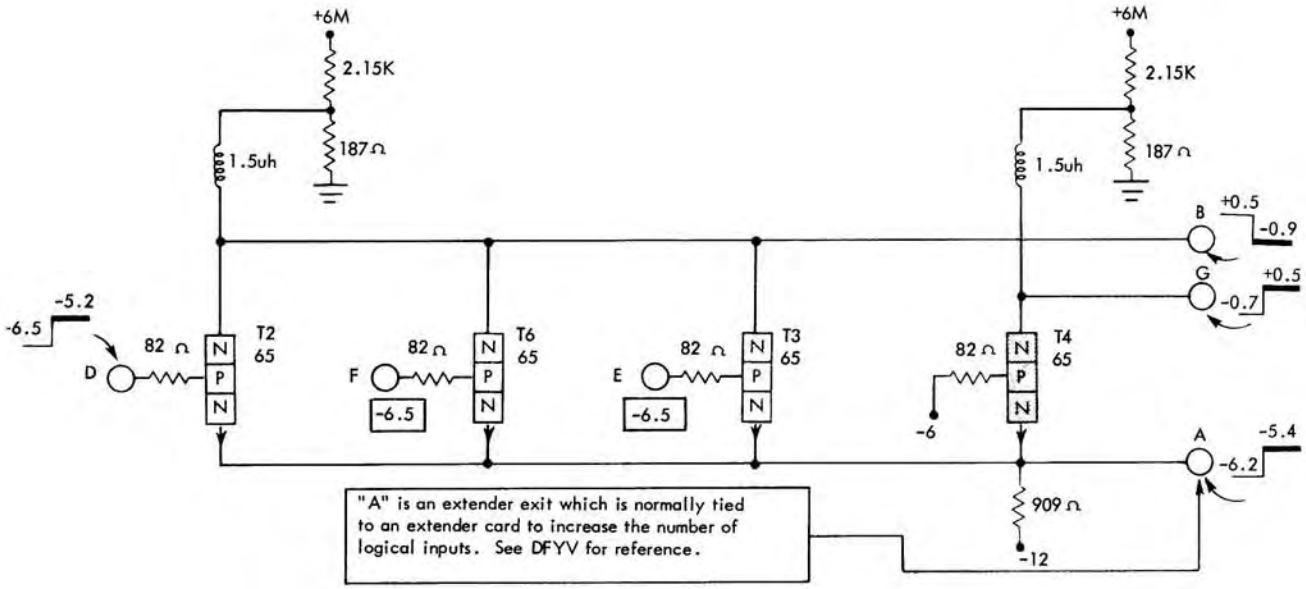
Output G is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network. Output B is at a +N level of +0.5v because of divider current through its coupling network.

When any input rises above −6v (see input D) the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a −N level because of current flow (6.7ma) through an input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v) so that transistor parameters are less critical.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap codes YX, YY, and YZ are used as required (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions.





Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
DFZE	1337	Yes	Yes	+O	-A	-5.6	See driver for max Output Levels	+0.4	+0.6	+0.4	+0.6
DFZC	1338	No	Yes	+OA	-AO	-6.4		-0.4	-1.1	-0.4	-1.4
				+TO	-TA						

Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	Turn Off
Min.	5.62	5.98	6	4
Nom.	6.25	7.22	15	11
Max.	6.87	8.46	25	18

Diffused Junction Three-Way OR, Type A

The three-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output. Output A is an extender exit for extender card use.

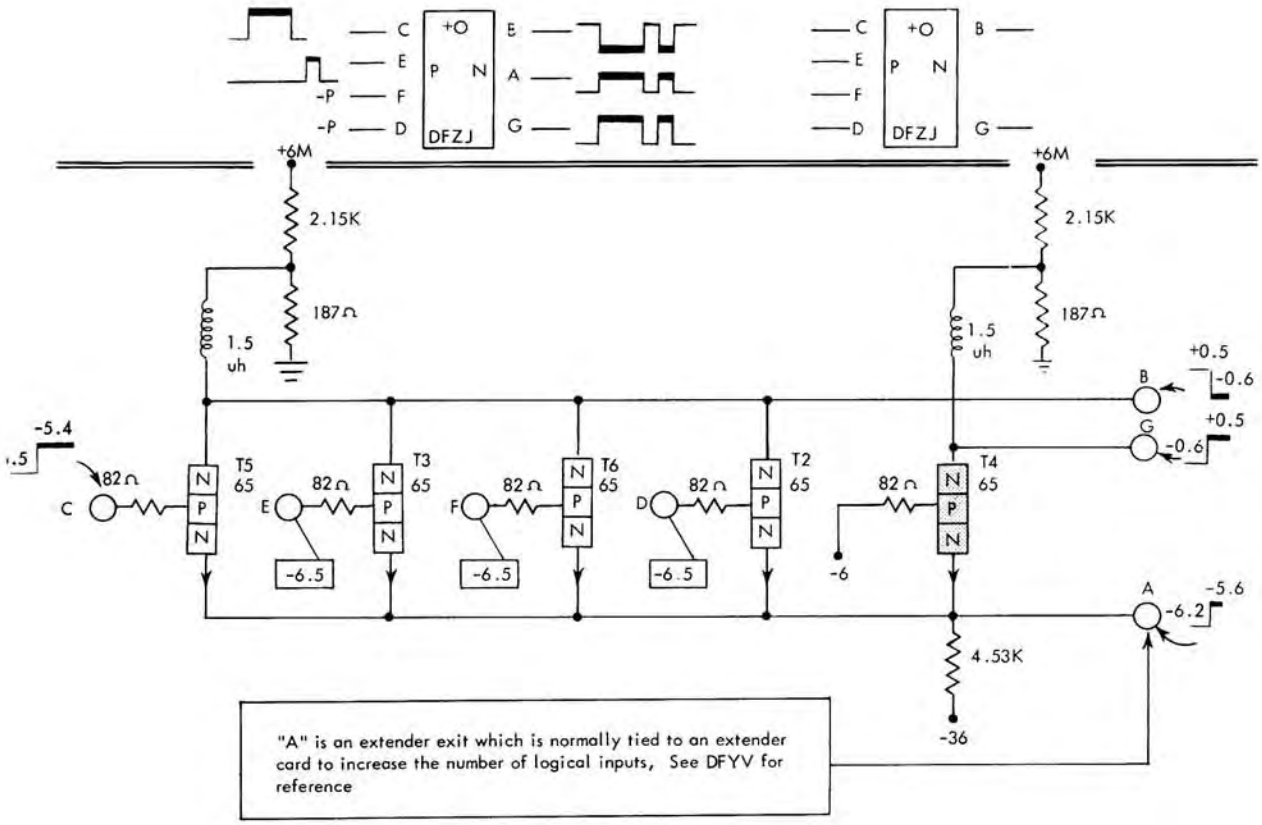
Circuit Description

This circuit uses three transistors (T2, T6, and T3) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. When all inputs are −P, T4 is forward-biased and clamps to −6v. Output G is at a −N level of −0.7v because of current flow (6.3ma) through T4 into its coupling network. Output B is at a +N level of 0.5v because of divider current through its coupling network.

When any input rises above −6v (see input D) the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a −N level of −0.9v because of current flow (7.2ma) through an input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit because it provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v).

Application

For some applications, the circuit driven by this logic block requires a special input coupling network. In such cases cap code ZC is used (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions.



Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
DFZJ	1332	Yes	Yes	+O	-A	-5.6	See driver for max. Output Levels	+0.4	+0.5	+0.4	+0.5
DFZH	1333	Yes	No	+OA	-AO			-0.4	-0.8	-0.4	-0.9
DGZG	1334	No	Yes	+TO	- TA	-6.4					
DFZF	1335	No	No								

Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	Turn Off
Min.	5.97	6.04	7	5
Nom.	6.56	6.69	15	10
Max.	7.14	7.34	26	16

Diffused Junction Four-Way OR, Type B

The four-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and −N out-of-phase output. Output A is an extender exit for extender card use.

Circuit Description

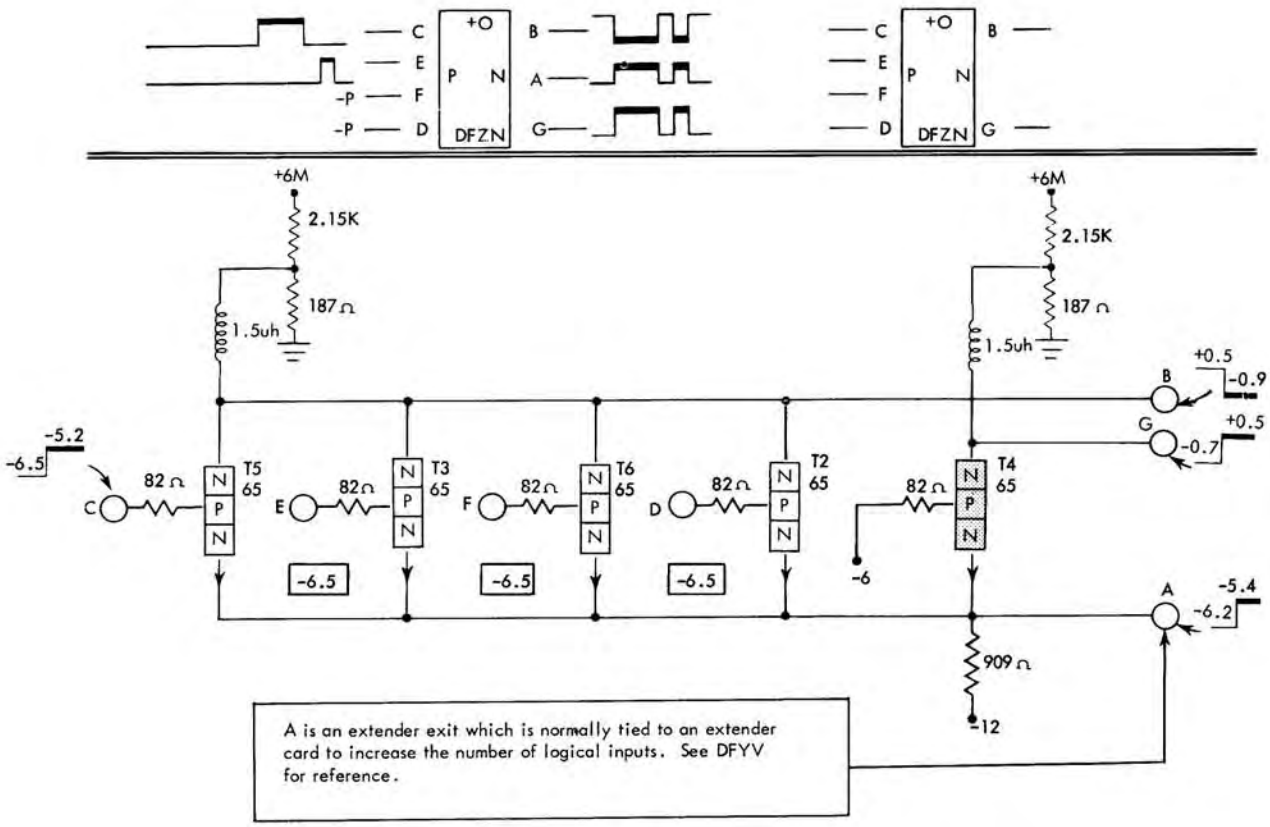
This circuit uses four transistors (T5, T3, T6, and T2) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−36v). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. All inputs are −P as shown and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to −6v.

Output G is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network. Output B is at a +N level of +0.5v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a −N level because of current flow (6.7ma) through an input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v) so that transistor parameters are less critical than in type A.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap codes ZF, ZG and ZH are used as required (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions.



Card Code	Part No. 3/----	Cplg Network		Circuit Used As		Input Levels		In-phase Output		Out-phase Output		Ma Output			musec BlockDelay	
		In Ø	Out Ø			Min	Max	Min	Max	Min	Max		In Ø	Out Ø	Turn On	Turn Off
DFZN	1330	Yes	Yes	+O	-A	-5.6 / -6.4	See driver for max. output levels	+0.4 / -0.4	+0.6 / -1.1	+0.4 / -0.4	+0.6 / -1.4	Min	5.62	5.98	7	5
DFZL	1331	No	Yes	+OA	-AO							Nom	6.25	7.22	15	10
				+TO	-TA							Max	6.87	8.46	26	16

Diffused Junction Four-Way OR, Type A

The four-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output. Output A is an extender exit for extender card use.

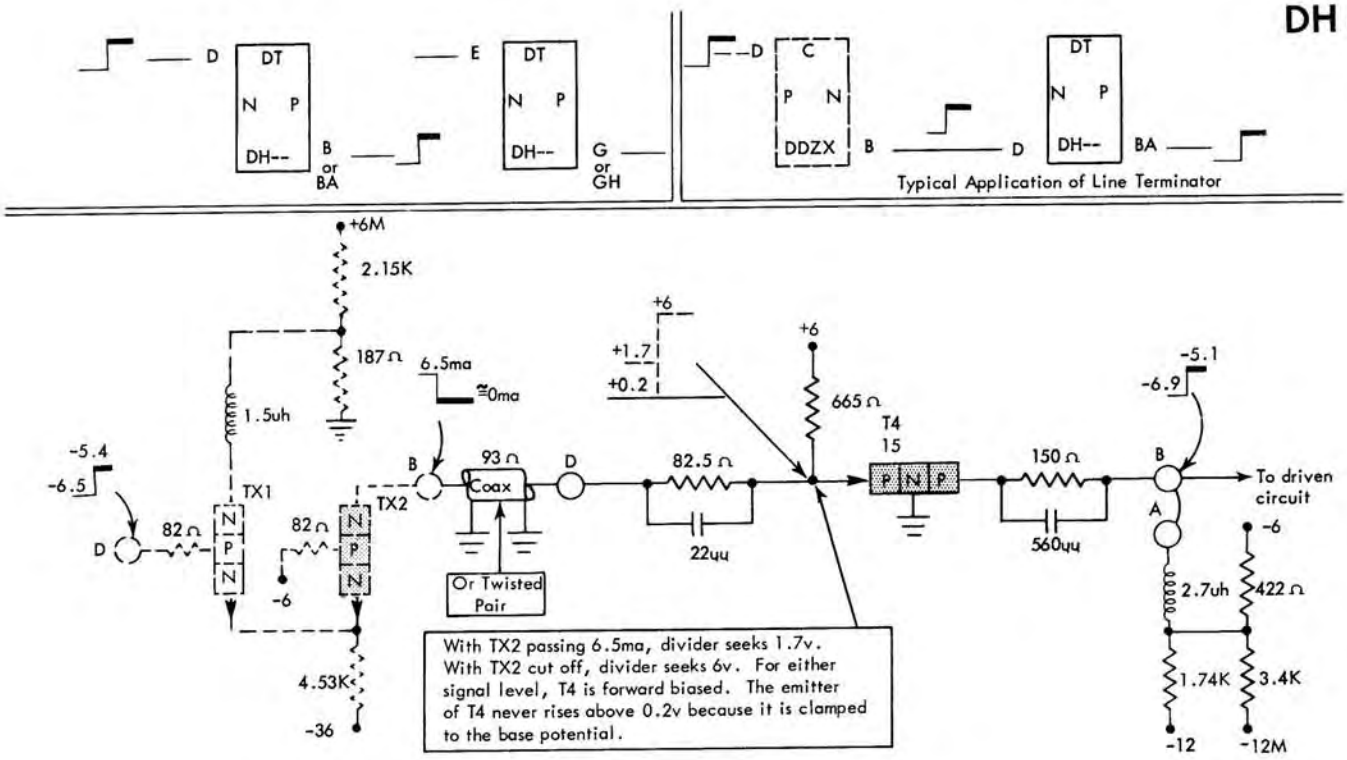
Circuit Description

This circuit uses 4 transistors (T5, T3, T6 and T2) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. All inputs are −P as shown and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output G is at a −N level of −0.7v because of current flow (6.3ma) through T4 into its coupling network. Output B is at a +N level of 0.5v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a −N level of −0.9v because of current flow (7.2ma) through an input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v).

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap code ZL is used (see chart). This circuit is also combined with an AND circuit to make up a trigger and with other OR circuit blocks to obtain DOT functions.



Card Code	Part No. 37----	Circuit Used as	Output Levels Min.	Output Levels Max.	musec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven By	Output Can Drive Into	
DH--	1138	DT	-5.6 / -6.4	-4.6 / -7.4				Type B Block, In Ø Output	3	Type A Block
								Type B Block, Out Ø Output	3	Type B Block
					Min.	15	10		3	Single Shot
					Nom.	28	18		3	Exclusive OR
					Max.	40	26		1	Power Driver (Note 2)

Note 1. Delays are measured from input terminal D of the terminator to the output of the logic block driven by the terminator.
Note 2. The terminator coupling network is not used when driving into a power driver, because the power driver has a special input network which requires a current input.

Diffused Junction N-to-P Line Terminator

This circuit provides an in-phase P-line output for an N-line input. It is designed to terminate the 93 ohm coaxial line when a single circuit termination is required. It can drive up to three logic blocks. This circuit requires that the driving source be restricted to driving this circuit only. When desired, the terminator may be used for local logic as an N-to-P line translator, in which case it may or may not be driven by coaxial line.

Circuit Description

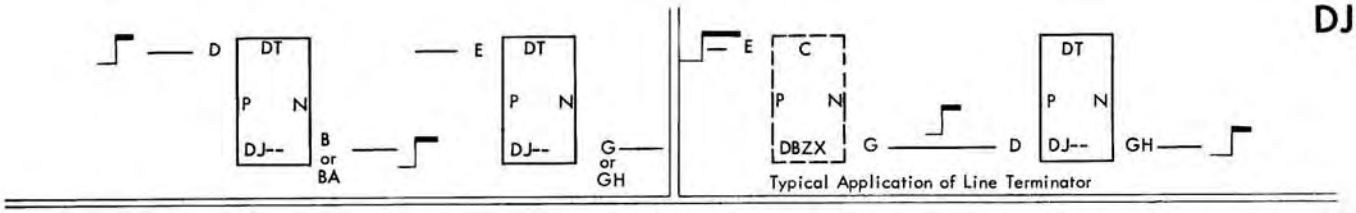
The DT circuit uses a single transistor in a grounded base configuration which is driven class A. In the state shown, TX2 is forward-biased and 6.5ma flows through TX2, 82.5 ohms, and 655 ohms to +6v. This input current develops a 4.3v drop across the 665 ohm resistor which sets the bias of T4 at +1.7v. Such a bias causes a current flow of 2.2ma out of the coupling network, through T4 to +6v. Output B is at a −P level of −6.9v because of this current flow. Although the emitter bias potential is set by input current, the emitter never rises above +0.2v because it clamps to its base potential of ground.

When the input signal to the converter rises, TX2 is cut off and the current fed to the terminator is reduced to zero. In this state the emitter level sees a 6v bias and the current flow through T4 is increased to 8.7ma which causes output B to rise to a +P level of −5.1v.

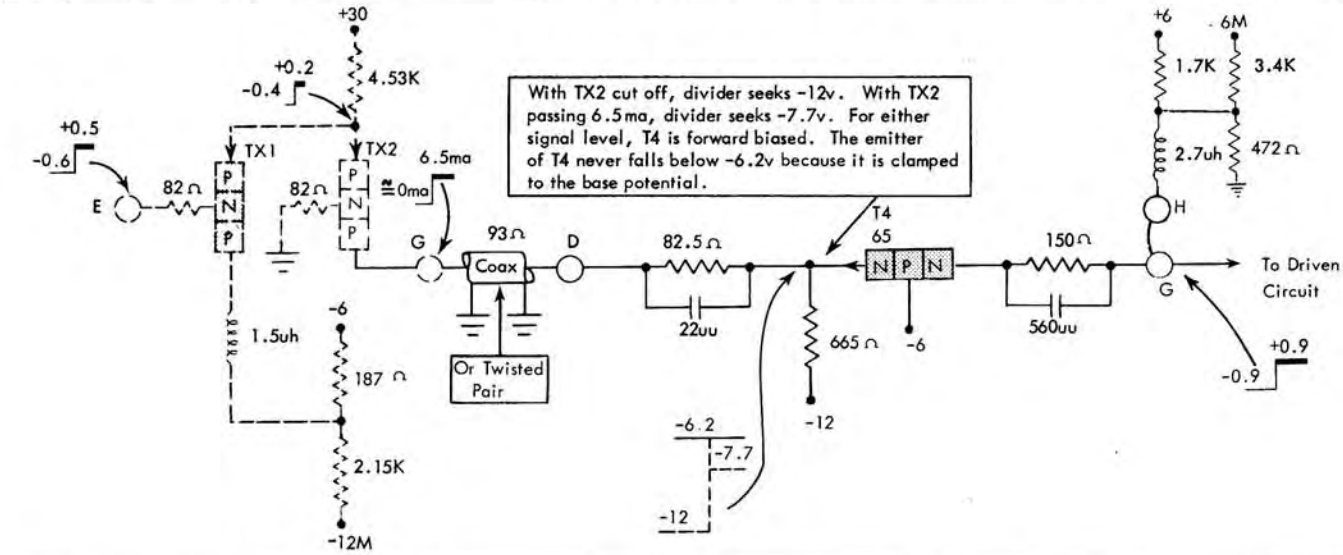
To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

Application

When this circuit drives a power driver the coupling network (2.7μh, 422 ohms, 1.74K, and 3.4K) shown is not used. In such cases output B drives directly into the special input coupling network of the power driver.



Typical Application of Line Terminator



Card Code	Part No. 37----	Circuit Used as	Output Level Min.	Output Level Max.	musec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven By	Output Can Drive Into	
DJ--	1139	DT	+0.4 -0.4	+1.4 -1.4				Type B Block, In Ø Output	3	Type A Block
								Type B Block, Out Ø Output	3	Type B Block
					Min.	15	10		3	Single Shot
					Nom.	28	18		3	Exclusive OR
					Max.	40	26		1	Power Driver (Note 2)

Note 1. Delays are measured from input terminal D of the terminator to the output of the logic block driven by the terminator.
Note 2. The terminator coupling network is not used when driving into a power driver, because the power driver has a special input network which requires a current input.

Diffused Junction P-to-N Line Terminator

This circuit provides an in-phase N-line output for a P-line input. It is designed to terminate the 93 ohm coaxial line when a single circuit termination is required. It can drive up to three logic blocks. This circuit requires that the driving source be restricted to driving this circuit only. When desired, the terminator may be used for local logic as a P-to-N line translator, in which case it may or may not be driven by coaxial line.

Circuit Description

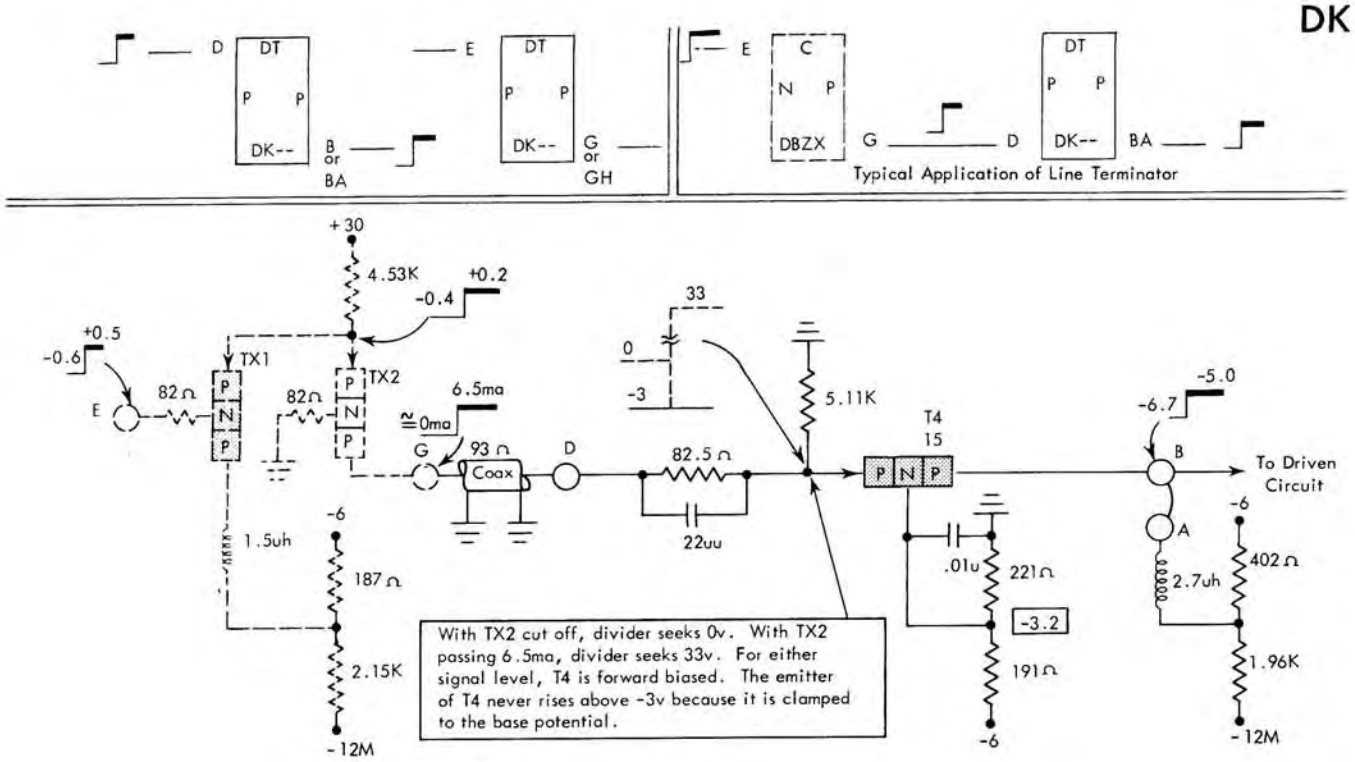
The DT circuit uses a single transistor (T4) in a grounded-base configuration which is driven class A. In the state shown, TX2 is cut off and the input current to the terminator is zero. The emitter-to-base bias is 6v because the emitter is returned to −12v and the base to −6v. Such a bias causes a current flow of 8.7ma from −12v through T4 into the coupling network. Output G is at a −N level of −0.9v because of this current flow into the coupling network. The emitter potential of T4 is −6.2v because the emitter clamps to its base potential of −6v.

When the input to the converter rises, TX2 is forward-biased and 6.5ma flows from −12v through 665 ohms, 82.5 ohms and TX2 to +30v. This input current develops a 4.3v drop across the 665 ohms which sets the emitter *bias potential* at−7.7v. Thus, T4 now sees a bias of only 1.7v instead of the 6v bias it saw when the input current was zero. This reduced forward bias reduces the current through T4 to 2.2ma, which causes output G to rise to a +N level of +0.9v.

To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

Application

When this circuit drives a power driver, the coupling network shown (2.7μh, 422 ohms, 1.74K and 3.4K) is not used. In such cases output B drives directly into the special input coupling network of the power driver.



Card Code	Part No. 37----	Circuit Used as	Output Levels Min.	Output Levels Max.	musec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven By	Output Can Drive Into	
DK--	1140	DT	-5.6 / -6.4	-4.4 / -6.9				Type A Block, In Ø Output	3	Type A Block
								Type B Block, In Ø Output	3	Type B Block
					Min.	21	13	Special Usage Only of Type B Block,	3	Single Shot
					Nom.	25	17	Out Ø Output	3	Exclusive OR
					Max.	31	20		1	Power Driver (Note 2)

Note 1. Delays are measured from input terminal D of the terminator to the output of the logic block driven by the terminator.
Note 2. The terminator coupling network is not used when driving into a power driver, because the power driver has a special input network which requires a current input.

Diffused Junction P-to-P Line Terminator

This circuit is designed to terminate the 93 ohm coaxial line when a single circuit termination is required. It provides an in-phase P line output for a P line input. The logic block output driving into this circuit cannot drive other circuits.

Circuit Description

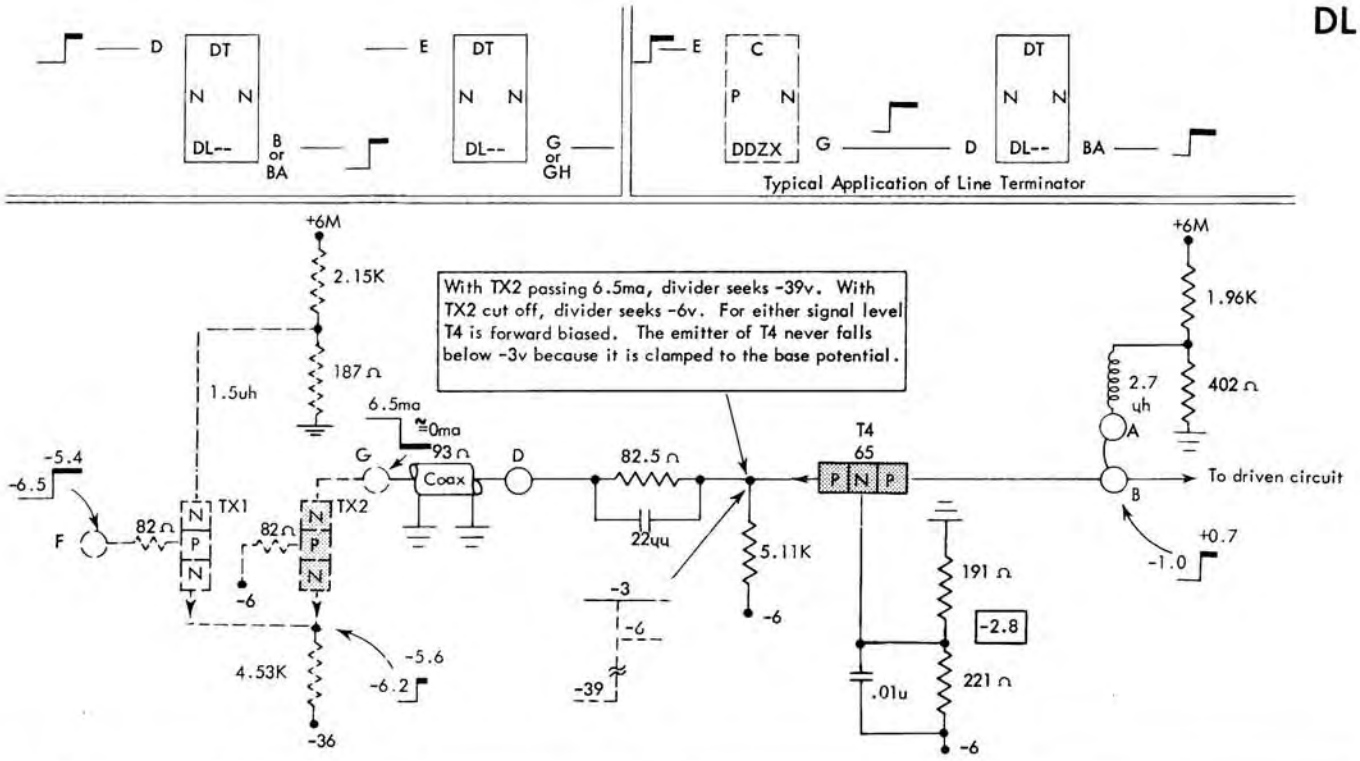
The DT circuit uses a single transistor (T4) in a grounded base configuration which is driven class A. In the state shown, TX2 is cut off and the input current to the terminator is zero. The emitter-to-base bias is 3.2v because the emitter is returned to ground while the base sees a −3.2v. Such a bias causes a current of 0.6ma to flow out of the coupling network through T4 to ground, which sets the output level of B at −6.7v. The emitter potential of T4 is −3v because the emitter clamps to its base potential of −3.2v.

When the input to the converter rises, TX2 is forward-biased and seeks to draw 6.5ma out of the terminator circuit, through TX2 to +30v. In this state the bias of T4 is increased because the emitter attempts to rise to a more positive level than ground. This condition exists because the emitter now sees the 5.11K ground resistor paralleled by approximately 5K to +30v. With the increased bias, the current flow through T4 increases to 7ma. This current is drawn out of the coupling network and the load, flows through T4, where it divides into current flow through TX2 to +30v and current flow through the 5.11K resistor to ground. Output G rises to a +P because of the increased current flow out of the coupling network.

To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

Application

When this circuit drives a power driver, the coupling network (2.7 μh, 402 ohms and 1.96K) is not used. In such cases output B drives the power driver directly.



Card Code	Part No. 37----	Circuit Used as	Output Levels Min.	Output Levels Max.	musec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven By		Output Can Drive Into
DL--	1141	DT	+0.4 / -0.4	+0.9 / -1.6				Type A Block, In Ø Output	3	Type A Block
								Type B Block, In Ø Output	3	Type B Block
					Min.	15	10	Special Usage Only of Type B Block,	3	Single Shot
					Nom.	28	18	Out Ø Output	3	Exclusive Or
					Max.	40	26		1	Power Driver (Note 2)

Note 1. Delays are measured from input terminal D of the terminator to the output of the logic block driven by the terminator.
Note 2. The terminator coupling network is not used when driving into a power driver, because the power driver has a special input network which requires a current input.

Diffused Junction N-to-N Line Terminator

This circuit is designed to terminate the 93 ohm coaxial line when only a single circuit termination is required. It provides an in-phase N line output for an N line input. The logic block output driving into this circuit cannot drive other circuits.

Circuit Description

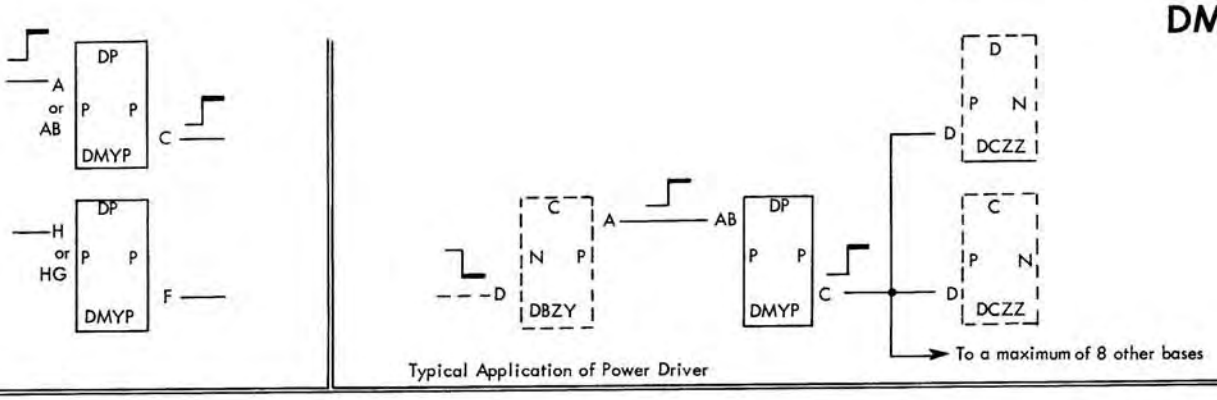
The DT circuit utilizes a single transistor (T4) in a grounded base configuration which is driven class A. In the state shown, TX2 is forward-biased and 6.5ma flows from −36v through TX2 and into the terminator. At this time the bias of T4 is greatest because its emitter no longer sees only a 5.11K resistor tied to −6v but it also sees approximately 5K to −36v. Such a bias causes 7.1ma to flow through T4 (6.5ma fed by TX2 and .6ma through the 5.11K) into the coupling network and into the load. Output B is at a −N level of −1v because of this current flow. The emitter potential is −3v because the emitter clamps to the base potential of −2.8v.

When the input to the converter rises, TX2 is cut off and the current fed to the terminator is reduced to zero. In this state, the bias of T4 is reduced because its emitter now sees only the −6v level tied to the 5.11K resistor. The current flow through T4 is reduced to .6ma and output B rises to a +N level of 0.7v because of divider current through the coupling network.

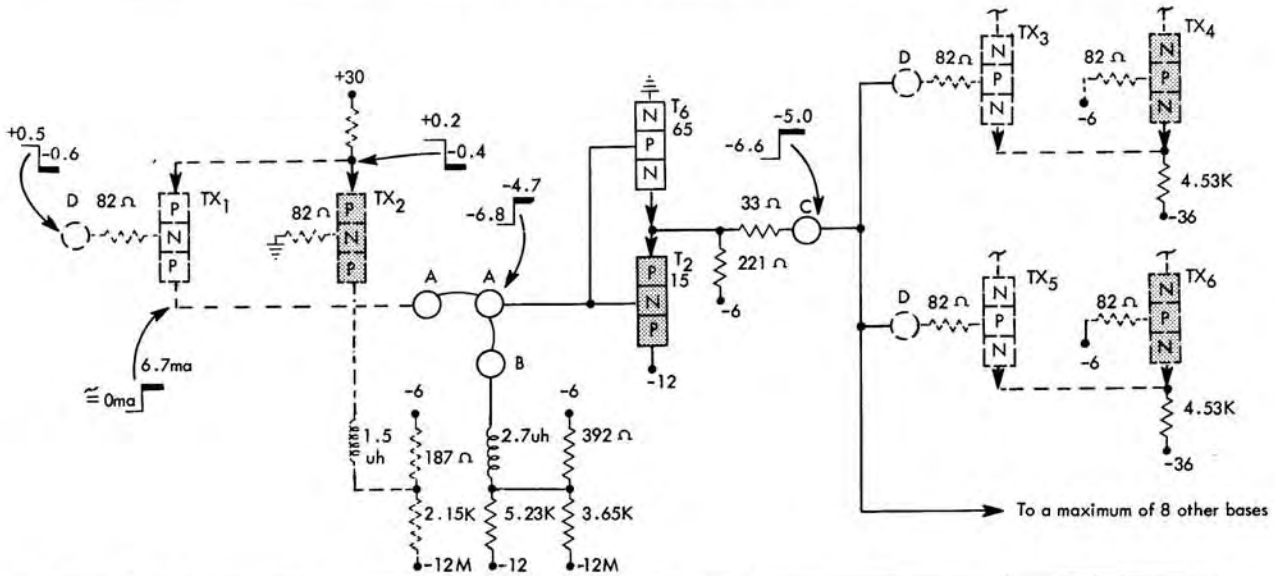
To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

Application

When this circuit drives a power driver, the coupling network (2.7μh, 402 ohms and 1.96K) is not used. In such cases output B drives directly into the special input coupling network of the power driver.



Typical Application of Power Driver



Card Code	Part No. 37----	Circuit Used as	Input Levels Min.	Input Levels Max.	Output Levels Min.	Output Levels Max.
DMYP	1350	DP	-5.1	-4.3	-5.6	-4.5
			-6.7	-6.9	-6.4	-6.7

musec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven by	Min. Pulse Width
			Type A Block, In Ø Output	50 musec
Min.	15	13	Type A Block, Out Ø Output (Only	
Nom.	31	21	When DP Input Clamp Ckt is Used)	
Max.	45	31	Type B Block, Either Output	

Note 1: Delays are measured from input terminal A of the power driver to the output of a logic block driven by the driver.

Diffused Junction P-to-P Power Driver (4-10 Bases)

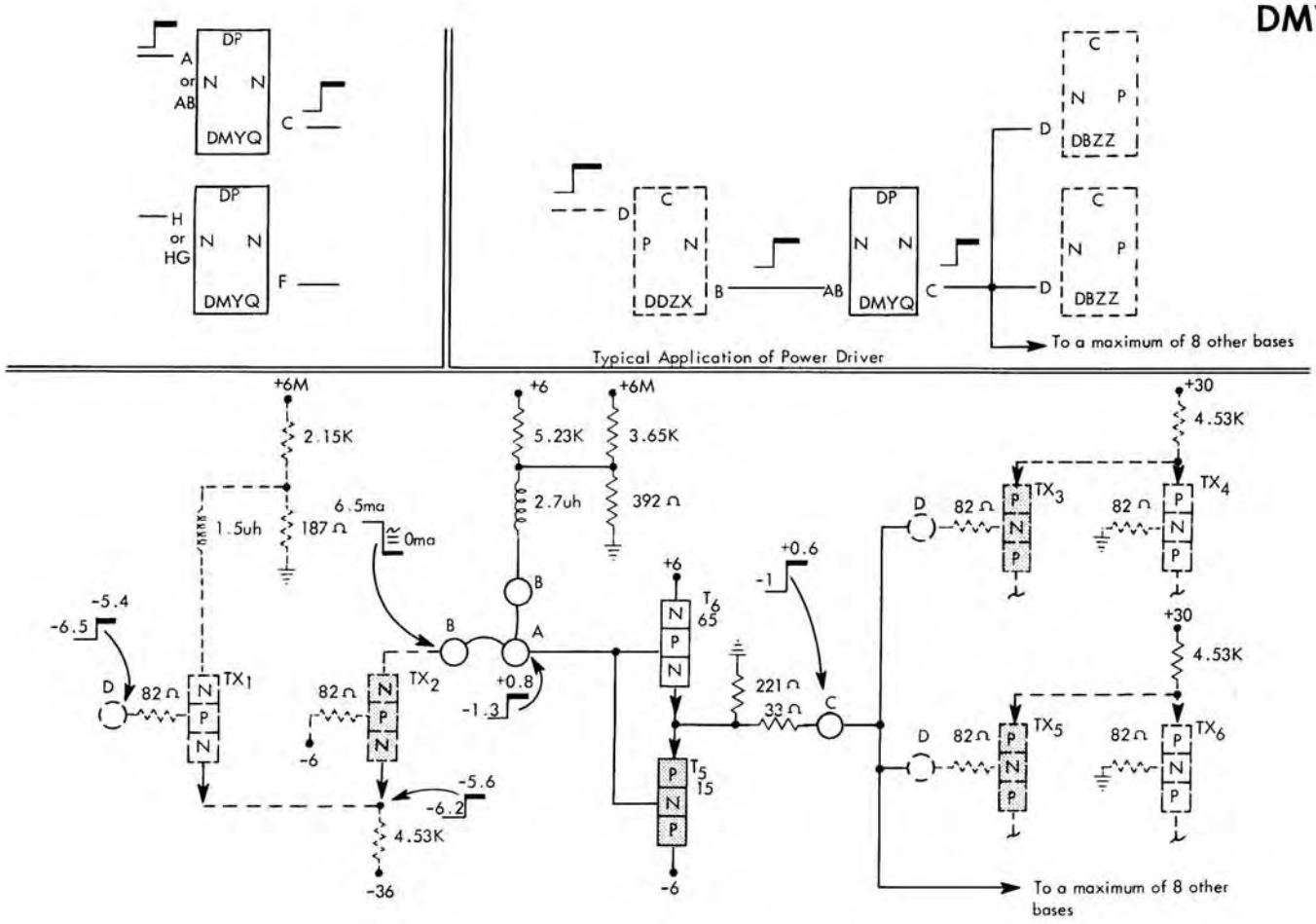
This power driver is used when it is required to drive from four to ten bases (logic circuits of the type shown in the above application). It provides an in-phase P line output for a P line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special coupling network is built into its input. This network converts an input current into the P line signal levels required.

Circuit Description

In the state shown, TX1 is cut off and the input current to the power driver is zero. Divider current through the coupling network (392 ohms, 3.65K, 5.23K) establishes a −P input level of −6.8v. T2 is forward-biased because its emitter is tied to a −6 return through a 221 ohm resistor. Current flows from −12v through T2 and 221 ohms to −6v. The emitter of T2 clamps to the −6.8v input potential and output C is at a −P level of −6.6v. Back currents for a maximum of ten TX3's also flow through T2.

When the input to the converter falls, TX1 is forward-biased and 6.7ma flows out of the coupling network through TX1 to +30v. The input level rises to −4.7v which cuts off T2 and forward-biases T6. Current through T6 flows from −6v through the 221 ohm resistor, which causes the emitter level of T6 to rise and clamp to its base potential. When the emitter potential of T6 rises above −6v, forward base current for a maximum of ten TX3's flows from −36v, emitter-base diodes of TX3's, through T6 to ground.

The input network peaking coil compensates for line capacitance so that optimum square wave response is realized. The 33 ohm output resistance is an oscillation suppressor which is necessary because of the inductive coupling network used.



Card Code	Part No. 37----	Circuit Used as	Input Levels Min.	Input Levels Max.	Output Levels Min.	Output Levels Max.	musec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven By	Min. Pulse Width
DMYQ	1349	DP	+0.7 -0.9	+0.9 -1.7	+0.4 -1.5	+0.7					
							Min.	15	13	Type A Block, In Ø Output	50 musec
							Nom.	31	21	Type A Block, Out Ø Output (Only When DP Input Clamp Ckt is Used)	
							Max.	45	31	Type B Block, Either Output	

Note 1. Delays are measured from input terminal A of the power driver to the output of a logic block driven by the driver.

Diffused Junction, N-to-N Power Driver (4-10 Bases)

This power driver is used in order to drive from four to ten bases (logic circuits of the type shown in the above application). It provides an in-phase N line output for an N line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special coupling network is built into its input. This network converts an input current into the N line signal levels required.

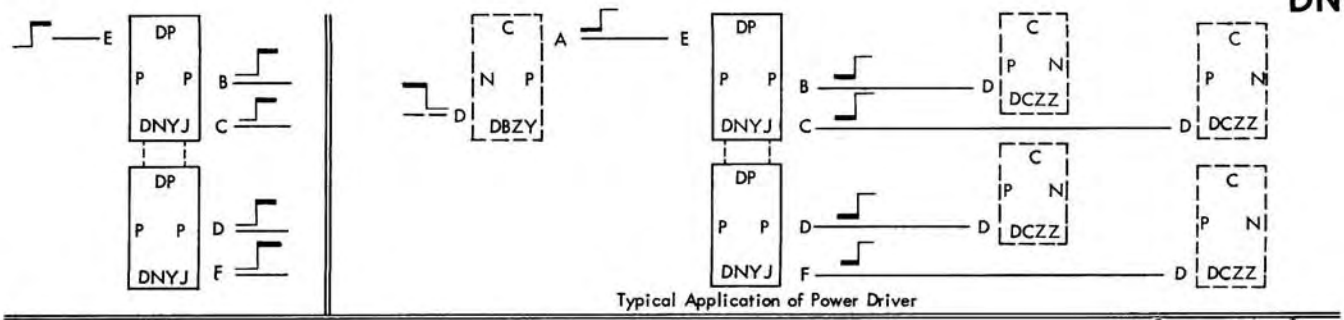
Circuit Description

In the state shown, TX2 is forward-biased and 6.5ma flows from −36v through TX2 into the coupling network to +6v and ground. Current flow into this coupling network establishes the input level at −1.3v. T5 is forward-biased because its emitter is tied to ground through the 221 ohm resistor. Current flows from −6v through T5 and 221 ohm to ground. The emitter clamps to its base potential and output C is at a −N level of −1v. Forward base current for a minimum of 10 TX3's supplied from −6v through T5, 33 ohm, base-emitter diodes of TX3's to +30v.

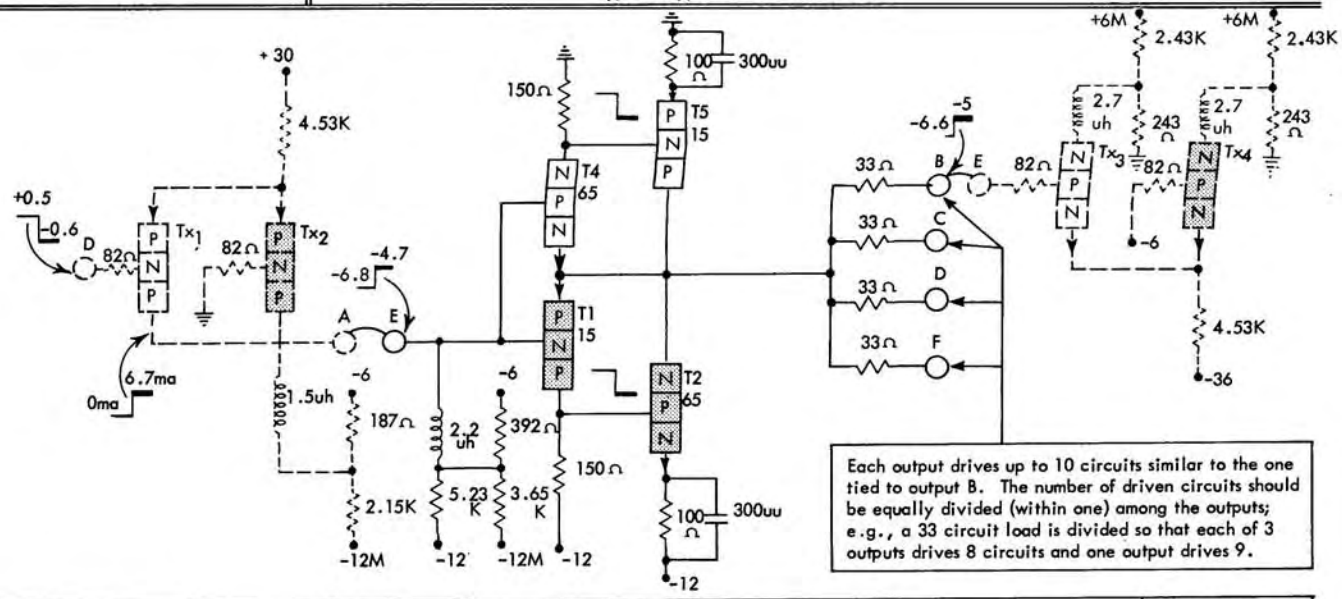
When the input to the converter rises, TX2 is cut off and the input current to the driver falls to zero. Divider currents through the coupling network cause the input level to rise to +0.8v. When the input level rises above ground, T5 is cut off and T6 is forward-biased. Current flows from ground through 221 ohms and T6 to +6v, and the emitter clamps to the base potential. The output level is +0.6v which reverse-biases the TX3 load transistors. Back currents for the TX3 transistors flow out of their bases through T6 to +6v.

The input network peaking coil compensates for line capacitance, so that optimum square wave response is realized. The 33 ohm output resistance is an oscillation suppressor that is necessary because of the inductive coupling network used.

DNYJ



Typical Application of Power Driver



Card Code	Part No. 37----	Circuit Used As	Input Levels Min.	Input Levels Max.	Output Levels Min.	Output Levels Max.	mu sec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven By	Min. Pulse Width
DNYJ	1354	DP	-5.1	-4.3	-5.5	-4.5	Min.	15	13	Type A Block, in Ø output	A ± drive pulse of 50 musec followed by a 100 musec recovery time.
			-6.7	-6.9	-6.4	-6.7	Nom.	31	21	Type A Block, out Ø output (only when DP input clamp circuit is used).	
							Max.	45	31	Type B Block, either output	

Note 1. Delays are measured from input terminal E of the power driver to the output of a logic block driven by the driver. The delays shown are those of the 4-10 base driver and are only approximate values for the 11-40 base driver.

See next page for purpose and circuit description.

Diffused Junction P-to-P Power Driver (11-40 bases)

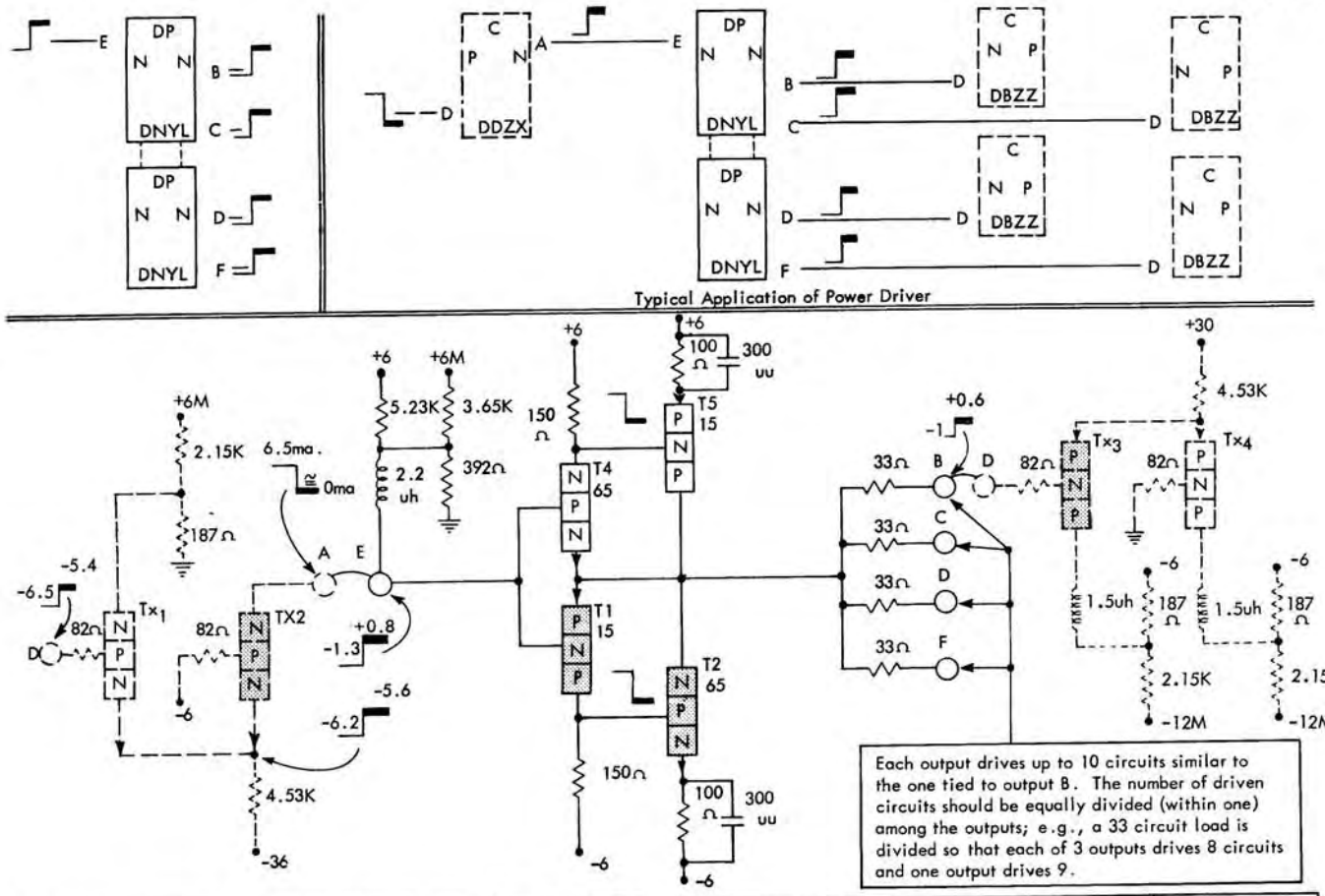
This power driver is used when it is required to drive from 11 to 40 bases (logic circuits of the type shown in the above application). It provides an in-phase P line output for a P line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special coupling network is built into its input. This network converts an input current into the P line signal levels required. In order to keep skew of the output signal to a minimum, the length of the output lines should be as equal as possible and the number of circuits driven by each line should be equal to within one circuit. For example, a load of 33 circuits is divided so that each of three outputs drives eight circuits and one output drives nine.

Circuit Description

In the state shown, TX1 is cut off and the input current to the power driver is zero. Divider current through the coupling network (392 ohms, 3.65K, 5.23K) establishes a −P input level of −6.8v. This input level forward-biases T1. In the status shown, T1 conducts and the back current for a maximum of 40 TX3's flows from −12v, through T1, the base-collector diode of TX3's, into an N line coupling network. The emitter of T1 clamps to the −6.8v input level and outputs B, C, D and F are at a −P level of −6.6v. Current through T1 develops a voltage drop across its 150 ohm collector resistor which raises the base potential of T2 above −12v. Thus, T1 and T2 conduct in parallel to set the −P level.

When the input to the converter falls, TX1 is forward-biased and 6.7ma flows out of the coupling network, through TX1 to +30v. Current flow out of the network causes the input level to rise to −4.7v. When the input level rises above −6v, T4 is forward-biased and T1 and T2 are cut off. The emitter of T4 follows its base above −6v, which forward-biases the TX3 load transistors. Load current flows from −36v through the emitter-base diodes of TX3's and T4 to ground. Current flow through the 150 ohm collector resistor of T4 feeds a below-ground signal to T5, which forward-biases T5. Thus, T4 and T5 conduct in parallel and set the +P output level at −5v.

The input network peaking coil compensates for line capacitance so that optimum square-wave response is realized. The 33 ohm output resistance is an oscillation suppressor which is necessary because of the inductive coupling network used. The effect of output capacitance is reduced by using 300$\mu\mu$fd bypass capacitors which cause T5 to be overdriven on the leading edge of a positive-going signal and T2 to be overdriven on the leading edge of a negative-going signal.



Card Code	Part No. 37----	Circuit used as	Input levels Min.	Input levels Max.	Output Levels Min.	Output Levels Max.
DNYL	1351	DP	-5.1 to -6.7	-4.3 to -6.9	-5.5 to -6.4	-4.3 to -6.7

usec Block Delay (Note 1)	Turn On	Turn Off
Min.	15	13
Nom.	31	21
Max.	45	31

Input Current Driven by	Min. Pulse Width
Type A Block, in Ø output	A ± drive pulse of 50 musec followed by a 100 musec recovery time.
Type A Block, out Ø output (only when DP input clamp is used)	
Type B Block, either output	

Note 1. Delays are measured from input terminal E of the power driver to the output of a logic block driven by the driver. The delays shown are those of the 4-10 base driver and are only approximate values for the 11-40 base driver.

Diffused Junction N-to-N Power Driver (11-40 Bases)

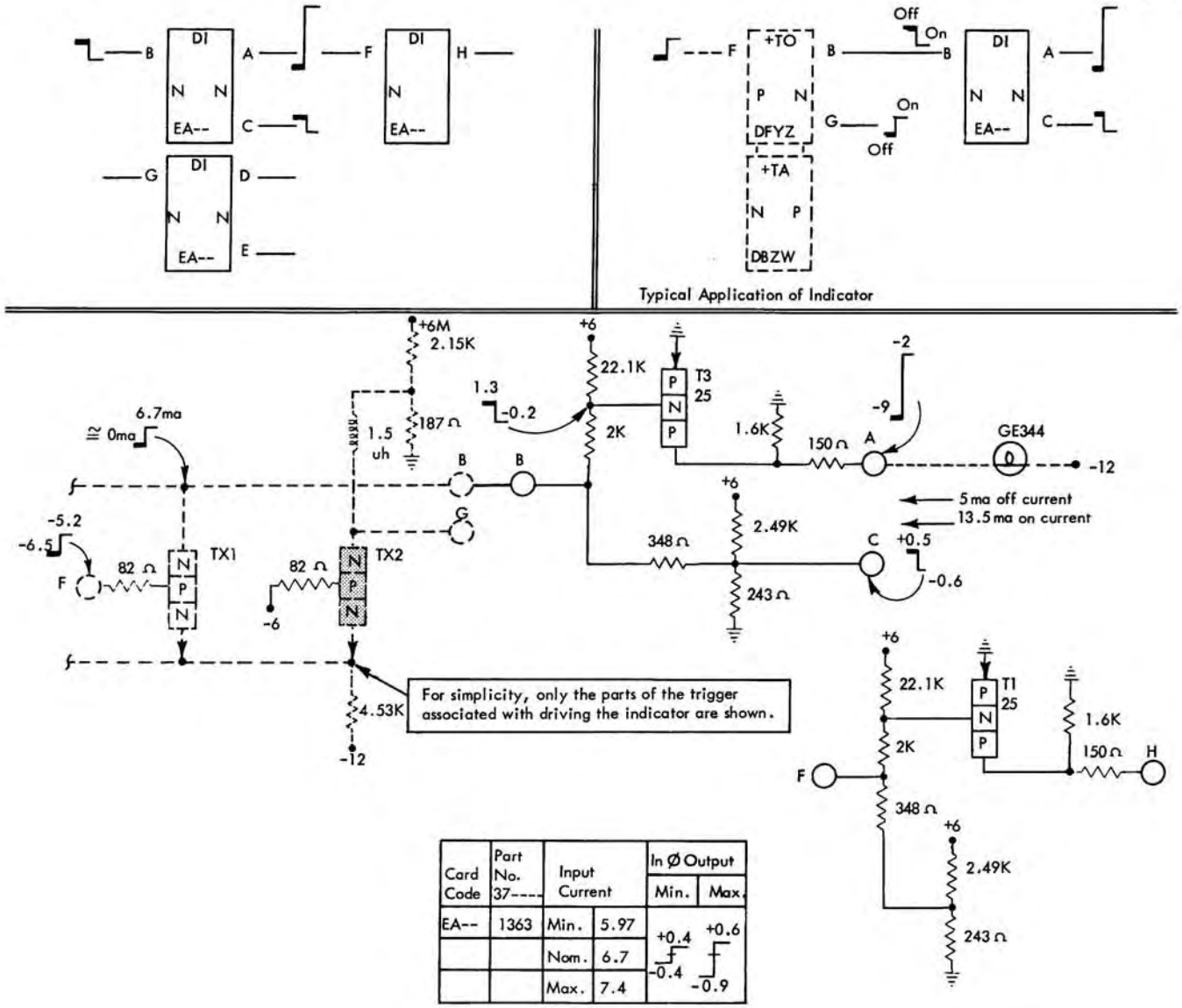
This power driver is used when it is required to drive from 11 to 40 bases (logic circuits of the type shown above.) It provides an in-phase N-line output for an N-line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special network is built into its input. This network converts an input current into the N-line signal levels required. To keep skew of the output signal to a minimum, the length of output lines should be as equal as possible and the number of circuits driven by each line should be equal to within one circuit. (See note.)

Circuit Description

In the state shown, TX2 is forward-biased and 6.5ma flows from −36v through TX2 into the coupling network to +6v and ground. Current flow into this coupling network establishes the input level at −1.3v. T1 is forward-biased and its emitter clamps to the −1.3v input. Forward load current flows from −6v through T1, base-emitter diode of TX3's to +30v. Current through T1 develops a voltage drop across its 150 ohm collector resistor, which raises the base potential of T2 above −6v. Thus, T1 and T2 conduct in parallel and outputs B, C, D and F are at a −N level of −1v.

When the input to the converter rises, TX2 is cut off and the input current to the driver falls to zero. Divider current through the coupling network causes the input level to rise to +0.8v. When the input level rises above ground, T4 is forward-biased and T1 and T2 are cut off. The emitter of T4 follows its base above ground, which reverse-biases the TX3 load transistors. Back current from the load transistors flows out of the collector-base diode of the TX3's, through T4 to +6v. The collector potential of T4 falls, and forward-biases T5. Thus, T4 and T5 conduct in parallel and the driver output is at a +N level of 0.6v.

The input network peaking coil compensates for line capacitance so that optimum square-wave response is realized. The 33 ohm output resistance is an oscillation suppressor which is necessary because of the inductive coupling network used. The effect of output capacitance is reduced by using 300 $\mu\mu$fd bypass capacitors.



Card Code	Part No. 37----	Input Current		In Ø Output Min.	In Ø Output Max.
EA--	1363	Min.	5.97	+0.4 -0.4	+0.6 -0.9
		Nom.	6.7		
		Max.	7.4		

Diffused Junction, —N Line Indicator

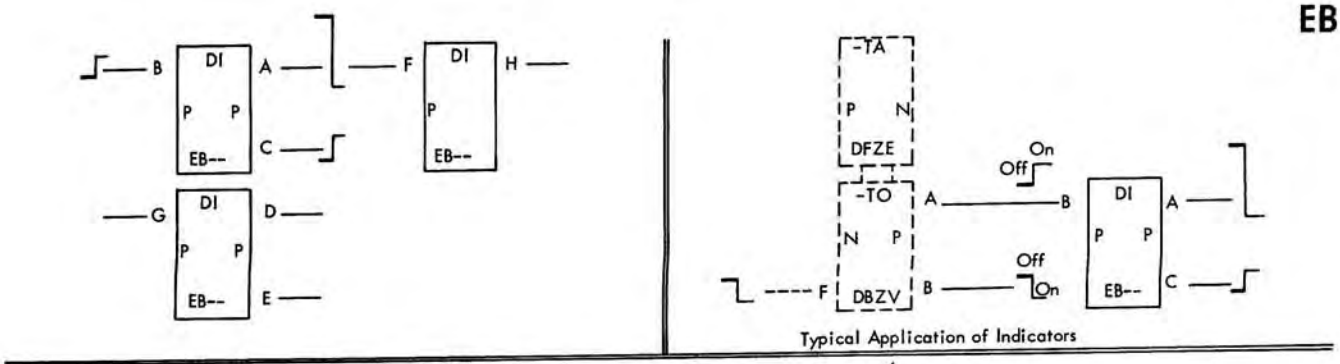
The EA-- card consists of three indicator circuits. Each circuit requires a —N line input to turn on the indicator lamp connected to the out-of-phase output. Two of these circuits also provide an in-phase N line output capable of driving two N type logic blocks. Note that the indicator above with no in-phase output has no N line output designation within the logic block. The N line notation is missing because the indicator signal levels (—2v to —9v) are not N levels but are special purpose levels.

Circuit Description

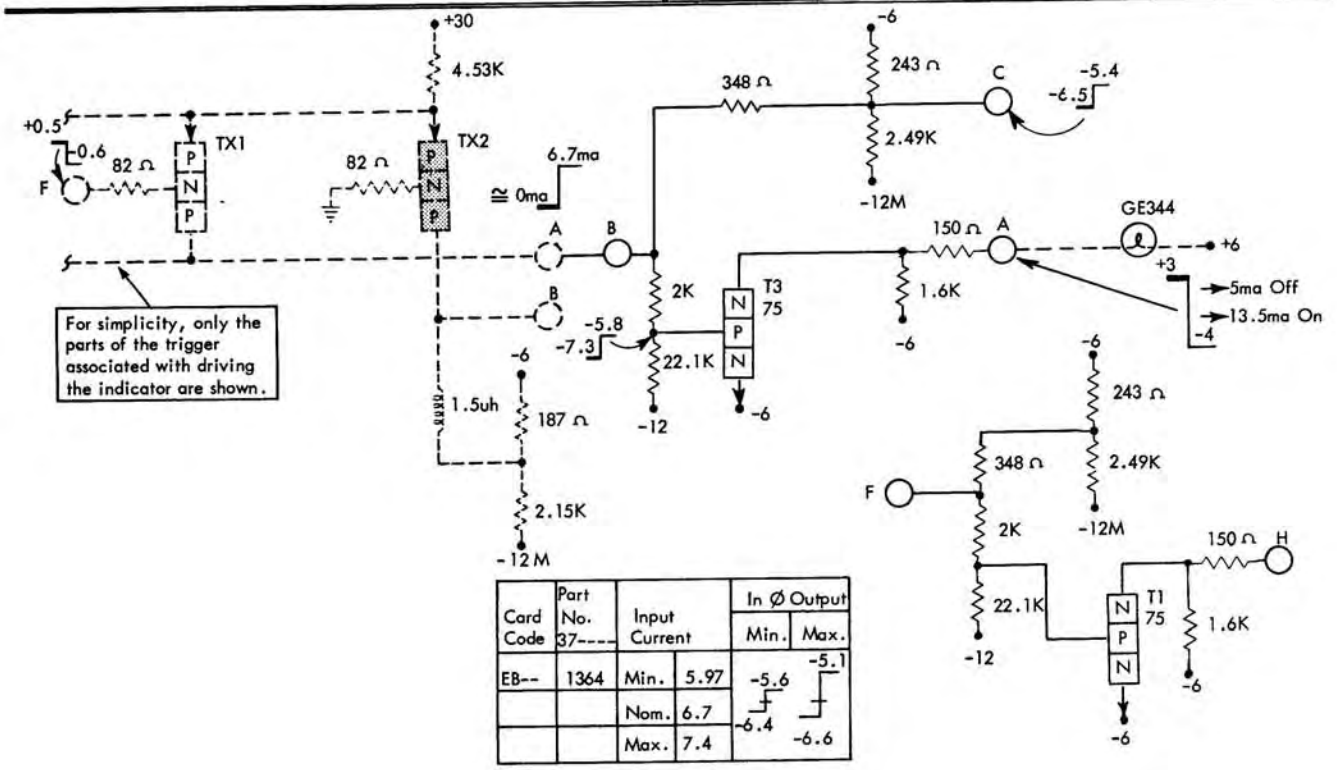
In the state shown, TX1 is reverse-biased and input current to the indicator is zero. Divider current through the 243 ohm, 2.49K coupling network establishes output C at a +N level of +0.5v. Current flow out of this network through the 22.1K to +6v sets the base level of T3 at +1.3v and T3 is reverse-biased. The 5ma current flow from —12v through the lamp and 1.6K to ground is not enough to light the lamp. This current flow sets output A at a —9v level.

When the input to TX1 rises, TX1 is forward-biased and 6.7ma flows from —12v through TX1 into the indicator where it divides into two components of current. One component flows into the coupling network which establishes output C at a —N level of —0.6v; while the other flows through the 2K and 22.1K to +6v which drives the base of T3 below ground. T3 is forward-biased and the 13.5ma which flows from —12v through the lamp, 150 ohm resistor, and T3 to ground is enough to light the lamp. The voltage drop across the 150 ohm and T3 is 2v so output A is at a —2v level.

The third indicator is identical to the one described except that an N line output is not provided. This output is missing only because all eight locations on the card for input and output line connections (terminals A-H) have already been assigned.



Typical Application of Indicators



Card Code	Part No. 37----	Input Current		In Ø Output Min.	In Ø Output Max.
EB--	1364	Min.	5.97	-5.6	-5.1
		Nom.	6.7	-6.4	-6.6
		Max.	7.4		

Diffused Junction, +P Line Indicator

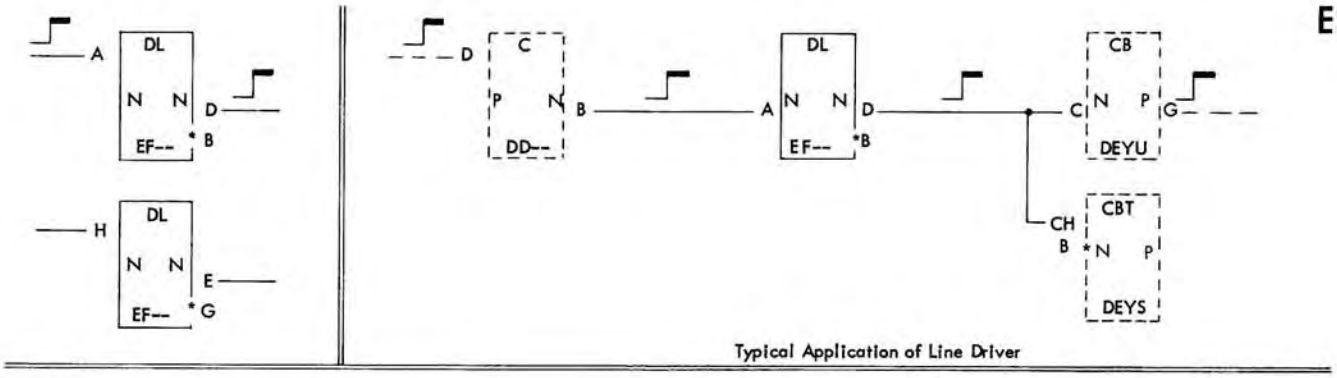
The EB - - card consists of three indicator circuits. Each circuit requires a +P line input to turn on the indicator lamp connected to the out-of-phase output. Two of these circuits also provide an in-phase P line output capable of driving two P type logic blocks. Note that the indicator above with no in-phase output, has no P line output designation within the logic block. The P line notation is missing because the indicator signal levels (+3v to −4v) are not P levels but are special purpose levels.

Circuit Description

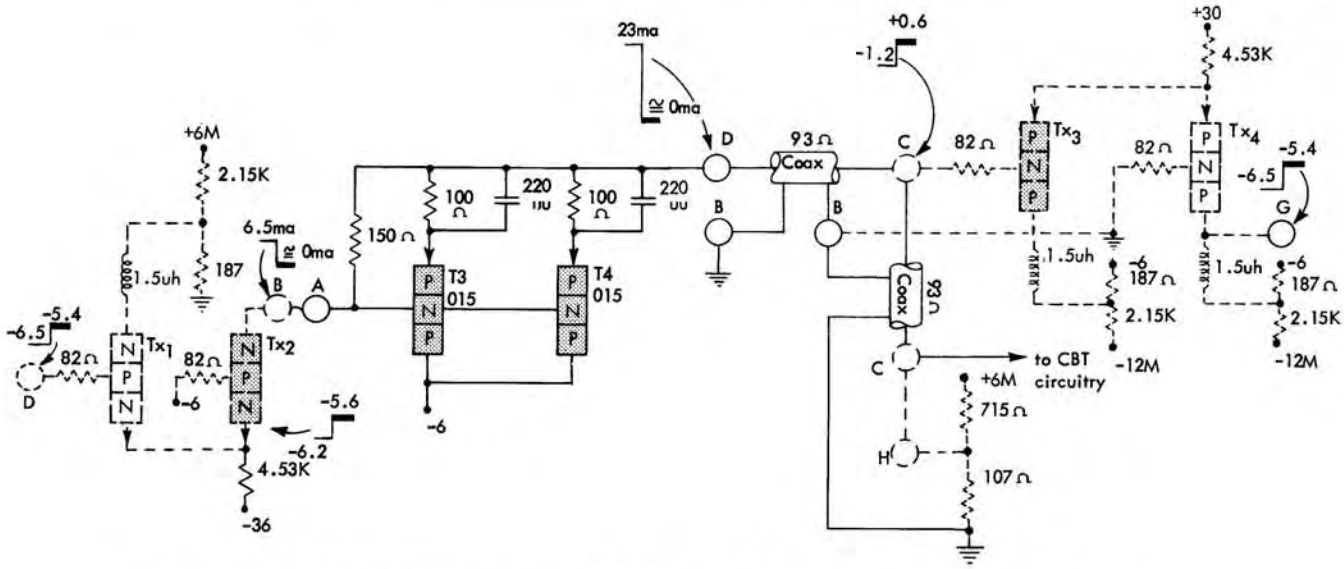
As shown, TX1 is reverse-biased and input current to the indicator is zero. Divider current through the 243 ohm, 2.49K coupling network establishes output C at a −P level of −6.5v. Current flow, from −12v through the 22.1K and 2K into the coupling network, sets the base level of T3 at −7.3v and T3 is reverse-biased. The 5ma current flow from −6v through the 1.6K and the lamp to +6 is not enough to light the lamp. The current flow establishes output A at a +3v level.

When the input to TX1 falls, TX1 is forward-biased and 6.7ma flows out of the driver through TX1 to +30v. This 6.7ma has two components of current. One component flows out of the coupling network to input B which establishes output C at a +P level of −5.4v; the other flows from −12v through the 22.1K and 2K to input B which drives the base of T3 above −6v. T3 is forward-biased and the 13.5ma which flows from −6v through T3 and the lamp to +6v is enough to light the lamp. The voltage drop across T3 and the 150 ohm resistor is 2v so output A is at a −4v level.

The third indicator is identical to the one described except that an N line output is not provided. This output is missing only because all eight locations on the card for input and output line connections (terminals A-H) have already been assigned.



Typical Application of Line Driver



Card Code	Part No. 37----	Circuit Used As	Output Levels Min.	Output Levels Max.	musec Block Delay (Note 1)	Turn On	Turn Off	Input Current Driven By	Output Can Drive Into
EF--	1171	DL	+0.4 -0.4	+0.8 -2.0	Min.	136	124	Type B logic block or its equivalent	Single input logic block only (max. of 5)
					Nom.	148	141		
					Max.	160	155		

Note 1. Delays are measured from the DL input terminal A to the output of a logic block driven by the line driver. Delay time was measured using 90 ft. of coax which has an approximate delay of 1.25 musec per foot.

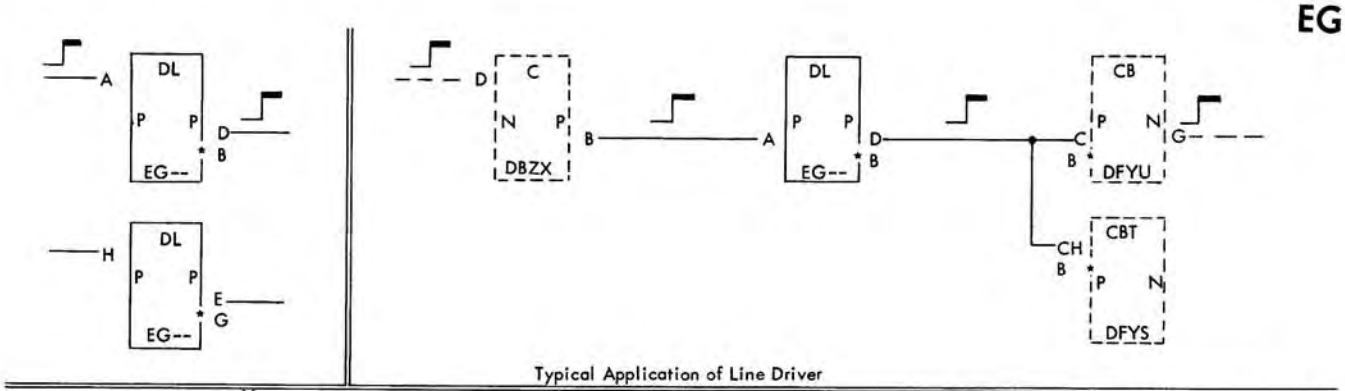
Diffused Junction, N-to-N Line Driver

The line driver couples information between two widely separated points over a 93 ohm coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive up to five circuits dispersed at random distances along the coaxial line. Line levels are established by the coupling network which terminates the line. Considering these line levels, the driver develops an in-phase N line output for an N line input.

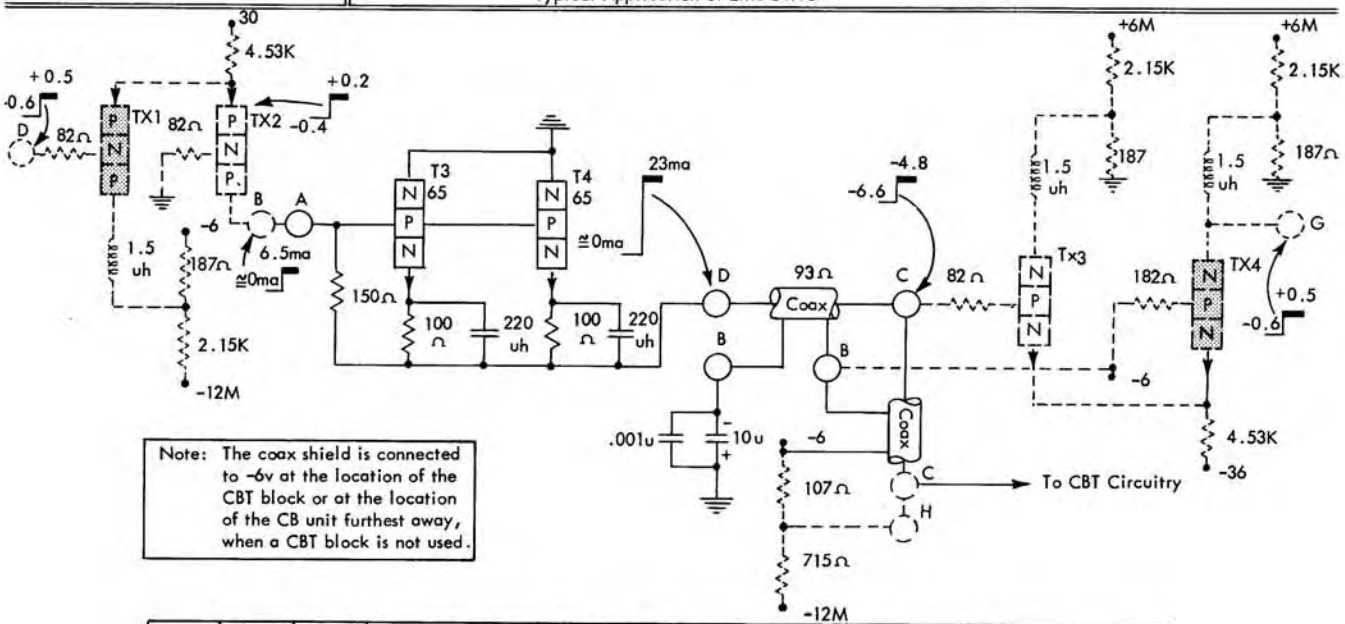
Circuit Description

As shown, TX2 is forward-biased and 6.5ma flows from −36v, through TX2, 150 ohms, the coaxial line and into the 107 ohm, 715 ohm coupling network. The voltage drop across the 150 ohm resistor develops a forward-bias for T3 and T4. Therefore the coaxial line is also supplied current from −6v through T3 and T4. In this state, a nominal current of 23ma flows through the coaxial line into the coupling network which establishes a −N level of −1.2v. Base current for T3 and T4 is supplied by the driving current of TX2. The 100 ohm emitter resistors provide degeneration so T3 and T4 tend to divide load current equally. The effects of line capacitance are reduced by the use of 220$\mu\mu$fd bypass capacitors. These capacitors cause T3 and T4 to be overdriven on the leading edge of the negative-going signal to permit line capacitance to quickly charge to the negative level. The coupling network is located at the end of the coaxial line furthest from the driver.

When the input signal to the converter rises, TX2 is cut off and the current fed to the line driver is reduced to zero. In this state, T3 and T4 have a zero bias and cut off. The output of the coaxial line rises to a +N level of +0.6v because of divider current through the coupling network.



Typical Application of Line Driver



Card Code	Part No 37----	Circuit used as	Output Levels Min.	Output Levels Max.	musec Block Delay (Note 1)	Turn On	Turn Off	Input Current driven by	Output can drive into
EG--	1375	DL	-5.6 / -6.4	-4.0 / -6.8	Min.	136	124	Type B logic block or its equivalent	Single input logic block only (max. of 5)
					Nom.	148	141		
					Max.	166	155		

Note 1. Delays are measured from the DL input terminal A to the output of a logic block driven by the line driver. Delay time was measured using 90 ft. of Coax which has an approximate delay of 1.25 musec per foot.

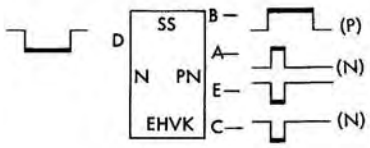
Diffused Junction, P-to-P Line Driver

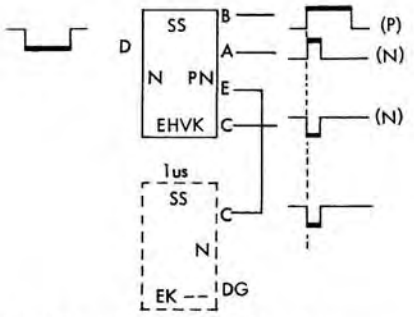
The line driver couples information between two widely separated points over a 93 coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive up to five circuits dispersed at random distances along the line. Line levels are established by the coupling network which terminates the coaxial line. Considering these line levels, the driver develops an in-phase P line output for a P line input.

Circuit Description

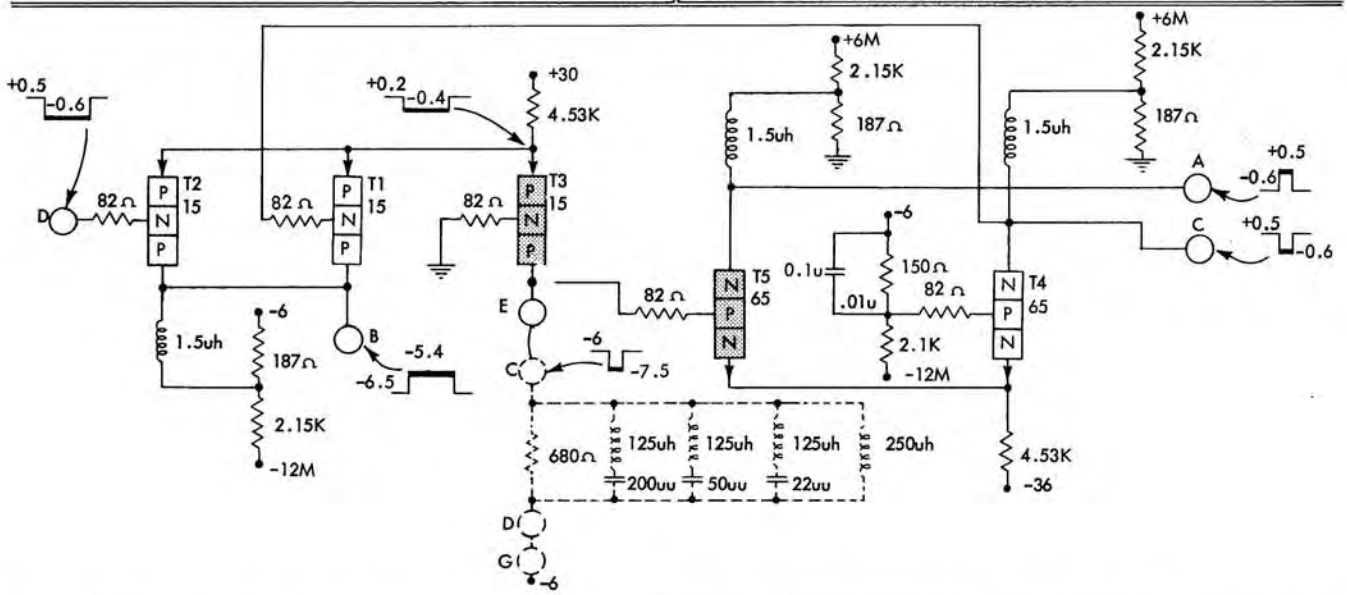
As shown, TX2 is cut off and the input current to the line driver is zero. The emitter and base of T3 and T4 are at the same level (bias is zero) and they are cut off. The output of the coaxial is at −P level of −6.6v because of divider current through the 107 ohm, 715 ohm coupling network.

When the input signal to the converter rises, TX2 is forward-biased and 6.5ma flows out of the coupling network, through the coaxial line, 150 ohm resistor, and TX2 to +30v. The voltage drop across the 150 ohm resistor develops a forward bias for T3 and T4. Therefore, additional line current is drawn out of the coupling network and flows through T3 and T4 to ground. In this state a nominal line current of 23ma flows out of the coupling network and the load to establish a +P level of −4.8v. Base current for T3 and T4 flows through TX2. The 100 ohm emitter resistors provide degeneration so T3 and T4 tend to divide load current equally. The effects of line capacitance are reduced by the use of 220$\mu\mu$fd bypass capacitors. The capacitors cause T3 and T4 to be overdriven on the leading edge of the positive going signal to permit line capacitance to quickly charge to the positive level. The coupling network is located at the end of the coaxial line furthest from the driver.





Single Shot and Timing Control Circuit



Card Code	Part No. 37----	Cplg Network		Input Levels		In-phase Output		Out-phase Output		Term. B Output		Ma Output			
		In Ø	Out Ø	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		In Ø	Out Ø	Term. B
EHVK	1368	Yes	Yes	+0.4	See driver for max. output levels	+0.4	+0.5	+0.4	+0.5	+0.5	+0.5	Min.	5.88	5.97	6.04
EHVL	1367	Yes	No												
EHVM	1366	No	Yes	-0.4		-0.4	-0.8	-0.4	-0.8	-0.4	-0.9	Nom.	6.47	6.66	6.70
EH--	1369	No	No									Max.	7.05	7.14	7.35

Diffused Junction, N Line Single-Shot

The single-shot card EHVK is used with a pulse forming card such as the EK - - card shown. Pulse forming cards are available in the 50 millimicrosecond to 50 microsecond range. The single-shot time duration is determined by the timing card used. The fall of the input N line starts the single-shot. Once started, the single-shot develops an in-phase N line timed output, an out-of-phase N line timed output, and a P line output pulse whose width is equal to the input pulse width or the timing card pulse width, whichever is greater. The input pulse width may be less than or greater than the timed output pulse. A recovery time of at least the timed pulse width is required before the input may be pulsed again.

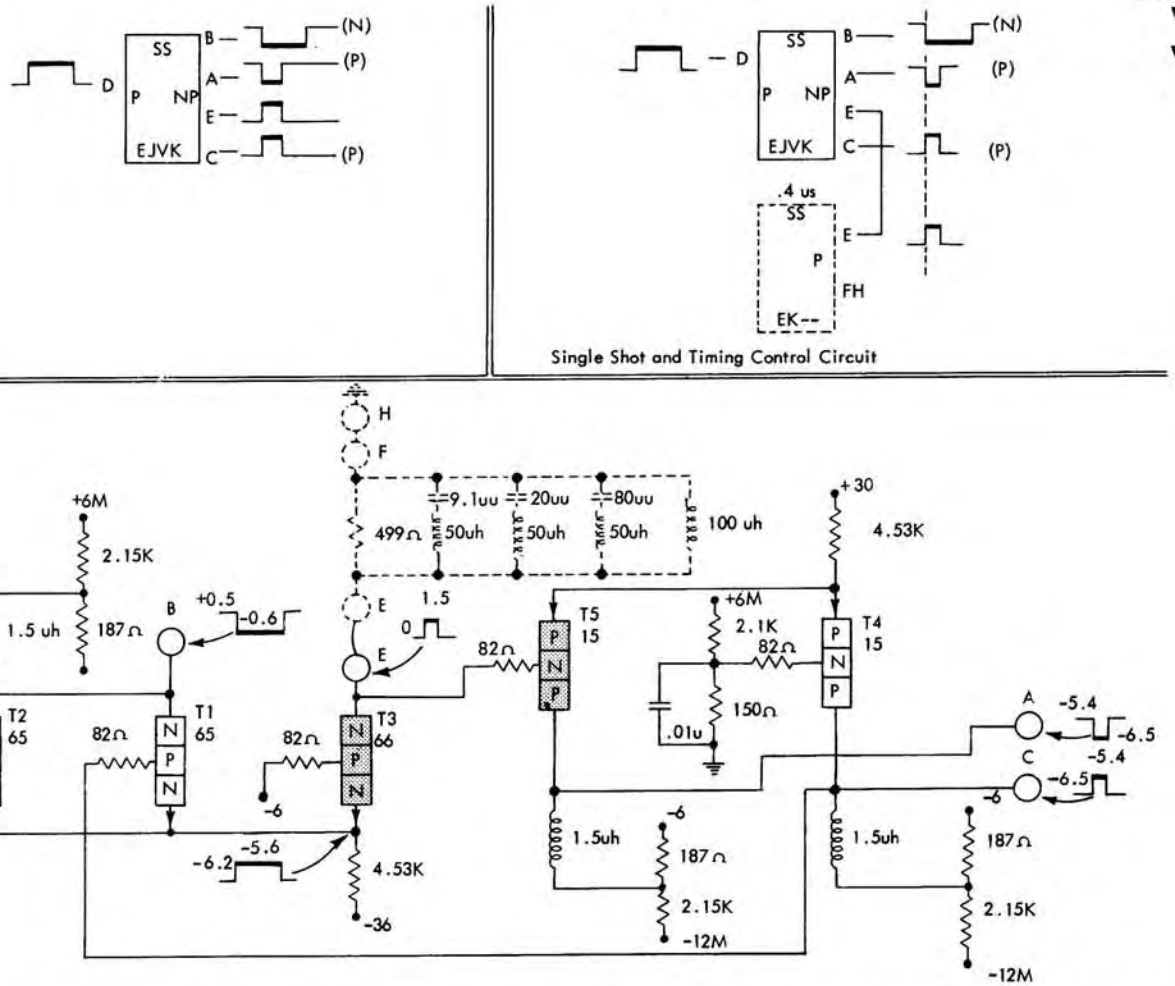
The timing card is made up of lumped constants in a shorted delay line configuration. Basically the pulse forming network is a summation of odd order harmonics.

Circuit Description

As shown, T2 is reverse-biased and T3 is forward-biased. Current flows from −6v through 680 ohms and 250μh in parallel and through T3 to +30v. The low DC resistance of the 250μh coil establishes the collector of T3 at about −6v. T5 is forward-biased and current flows from −36v through T5 into its coupling network to establish output A at a −N level of −0.6v. Output C is at a +N level of +0.5v because of divider current. Output B is at a −P.

When the input to T2 falls, T2 is forward-biased and T3 cuts off. Current flow out of the coupling network through T2 to +30v establishes output B at a +P level of −5.4v. The field in the 250μh coil collapses and a 1.5v signal is developed. This signal drives the base of T5 to −7.5v which forward-biases T4 and cuts off T5. Current flow through T4 into its coupling network establishes output C at a −N level of −0.6v, which forward-biases T1. T1 holds T3 cut off during the timing pulse. This arrangement permits the single-shot to be pulsed by an input whose duration is less than the single-shot timing. Output A rises to a +N level of +0.5v because of divider current.

When the pulse forming network times out, T5 is again forward-biased and T4 is cut off. Output A and C return to their original state and T1 is cut off. When the input signal rises, T3 is forward-biased and T2 is cut off. Output B falls to −P.



Single Shot and Timing Control Circuit

Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Input Levels Min.	Input Levels Max.	In-phase Output Min.	In-phase Output Max.	Out-phase Output Min.	Out-phase Output Max.	Term. B Output Min.	Term. B Output Max.
EJVK	1373	Yes	Yes	-5.6 / -6.4	See driver for max. output levels	-5.6 / -6.4	-5.2 / 5.6	-5.6 / -6.4	-5.2 / 6.5	-5.6 / -6.4	-5.1 / 6.5
EJVL	1372	Yes	No								
EJVM	1371	No	Yes								
EJ--	1374	No	No								

Ma. Output	In Ø	Out Ø	Term B
Min.	5.88	5.97	6.04
Nom.	6.47	6.66	6.70
Max.	7.05	7.14	7.35

Diffused Junction, P Line Single-Shot

The single-shot card EJVK is used with a pulse forming card such as the EK- - card shown. Pulse forming cards are available in the 50 millimicrosecond to 50 microsecond range. The single-shot time duration is determined by the timing card used. The rise of the input P line starts the single-shot. Once started, the single-shot develops an in-phase P line timed output, an out-of-phase P line timed output, and an N line output pulse whose width is equal to the input pulse width or the timing card pulse width, whichever is greater. The input pulse width may be less than or greater than the timed output pulse. A recovery time of at least the timed pulse width is required.

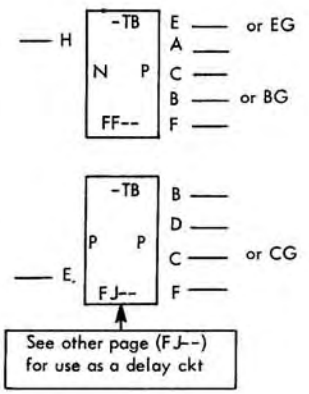
The timing card is made up of lumped constants in a shorted delay line configuration. Basically the pulse forming network is a summation of odd order harmonics.

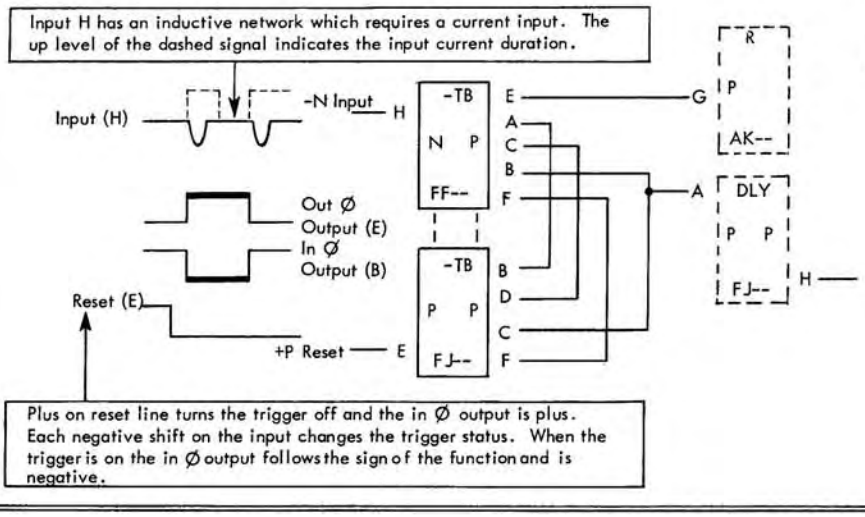
Circuit Description

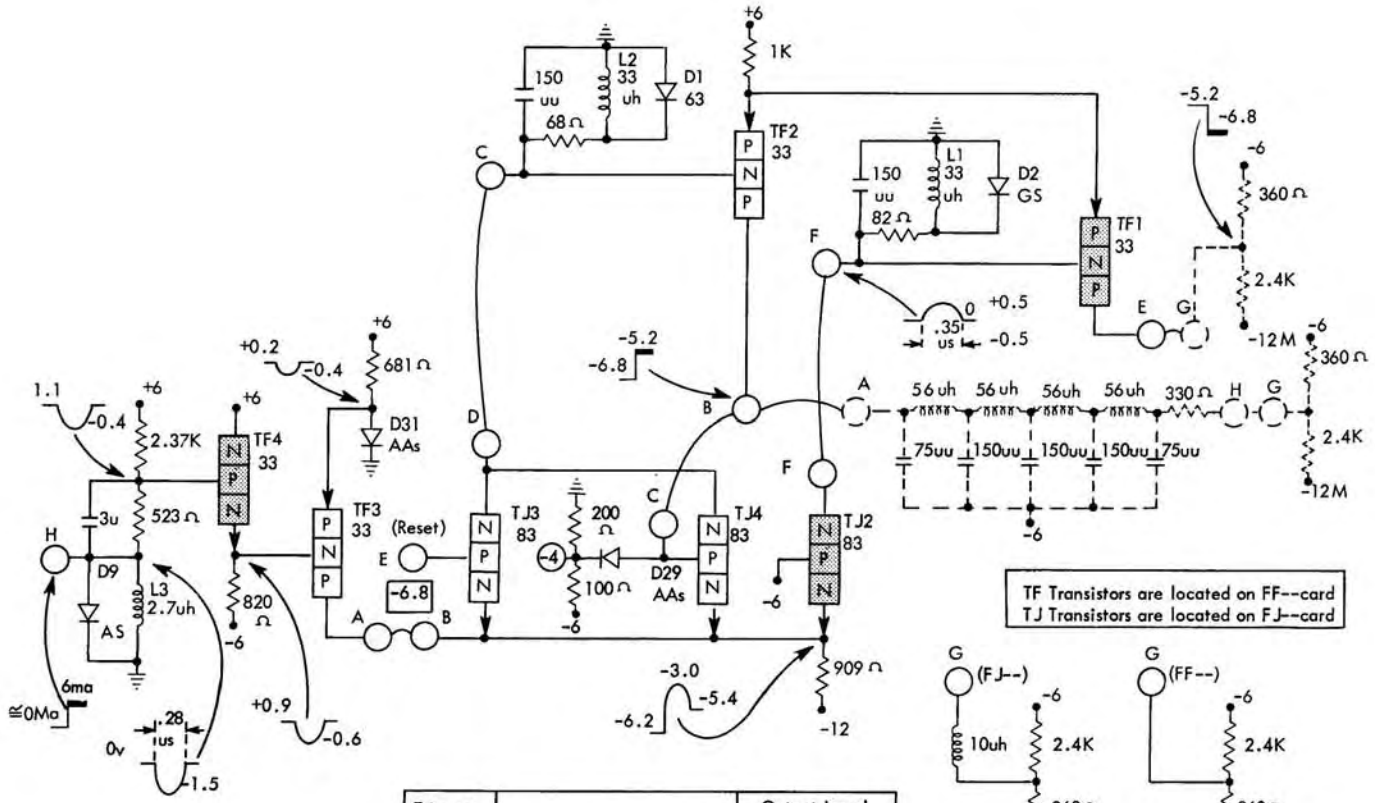
As shown, T2 is reverse-biased and T3 is forward-biased. Current flows from −36v through T3, and through 499 ohms and 100μh in parallel to ground. The low DC resistance of the 100μh coil establishes the collector of T3 at about 0v. T5 is forward-biased and current flows out of its network, through T5 to +30v, and establishes output A at a +P level of −5.4. Output C is at a −P because of divider current and output B is at a +N.

When the input to T2 rises, T2 is forward-biased and T3 cuts off. Current flow through T2 into its coupling network establishes output B at a −N level of −0.6v. The field in the 100μh coil collapses and a 1.5v signal is developed. This signal drives the base of T5 to +1.5v which forward-biases T4 and cuts off T5. Current flow out of the coupling network, through T4 to +30 establishes output C at a +P level of −5.4v which forward-biases T1. T1 is desiged to hold T3 cut off for the duration of the timing pulse. This arrangement permits the single-shot to be pulsed by an input whose duration is less than the single-shot timing. Output A falls to a −P level of −6.5v.

When the pulse forming network times out, T5 is again forward-biased and T4 is cut off. Output A and C return to their original state and T1 cuts off. When the input signal falls T3 is forward-biased and T2 is cut off. Output B rises to +N.







Trigger Status	Transistors Conducting are:	Output Level	
		In Ø	Out Ø
OFF	TF2,4, TJ4	+	-
ON	TF1,4, TJ2	-	+

Sequence	Turn Off	TF4 decr → TF3 on → TJ2 off → TF1 off → TF2 on → Input times out → TF4 incr → TF3 off → TJ4 on → TJ4 Keeps TF2 on
	Turn On	TF4 decr → TF3 on → TJ4 off → TF2 off → TF1 on → Input times out → TF4 incr → TF3 off → TJ2 on → TJ2 Keeps TF1 on

FF--	371411	Current Mode, Negative Binary Trigger Card 1
FJ--	371412	Current Mode, Negative Binary Trigger Card 2

Current Mode, Negative Binary Trigger, Cards 1 and 2

The FF - - card and the FJ - - card are connected to form a negative binary trigger (see logic application). A +P to input E of FJ - - resets the trigger off; the in-phase output is +P and the out-of-phase output is −P. Each −N input to FF - - alters the trigger status, so the first −N input after reset turns the trigger on. The in-phase output falls to a −P and the out-of-phase output rises to a +P. Note that when the trigger is on, its in-phase output follows the sign of the function (−TB function has a negative sign and the in-phase output is negative).

The input signal in the logic application is a dashed square wave *current* input and an inductive AC voltage resulting from this current input (see note associated with input signal). Such an input is necessary because the design of a binary trigger requires that the trigger operate on AC signals only and be isolated from the DC component of the signals. The input inductive network is designed to develop a negative signal when the input current rises from zero. The fall of the current back to zero has no effect. The trigger is designed to operate at 1 megacycle.

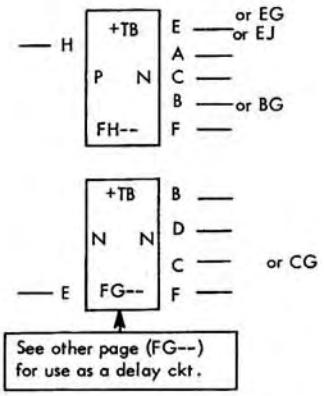
Circuit Description

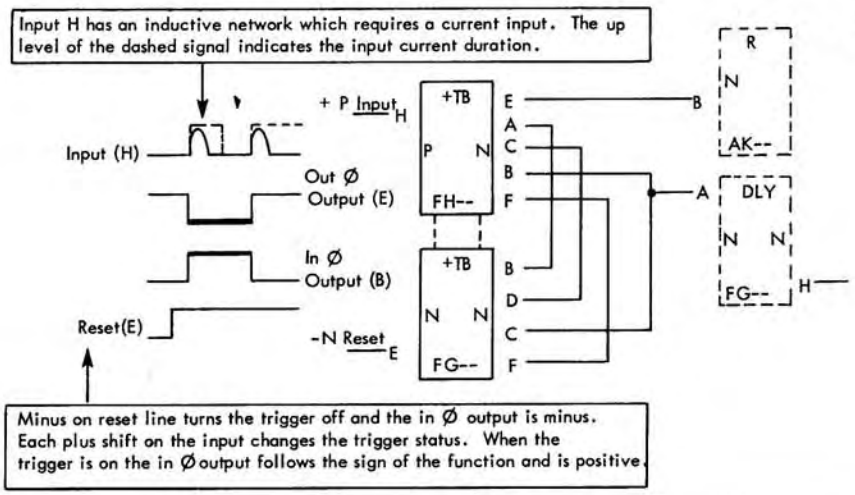
Before studying the circuit in detail, take an overall look at the schematic. Note the trigger status chart and sequence chart which summarize the over-all sequence of events. The trigger status chart shows that the trigger is on in the state shown (TF1, TF4, and TJ2 conducting).

The trigger is flipped by increasing input current from zero to 6ma. Input current flows from the negative source of the driving circuit into input H where it divides into two components of current. One component flows through 523 ohms and 3μfd in parallel and through 2.37K to +6v. The second component flows through the 27μh coil L3 to ground. It is the changing current through this coil which develops the 1.5v signal shown. This 1.5v signal is passed by the 3μfd capacitor and the forward bias of TF4 is reduced. The emitter of TF4 follows its base and TF3 conducts when its base falls below +0.2v. Current flows from −12v through TF3 and 681 ohms to +6v which raises the emitter of TJ2 above −6v and cuts off TJ2. With TJ2 cut off, current flow through coil L1 falls to zero and develops a 1v signal. The base of TF1 rises to a +1v which forward-biases TF2 and cuts off TF1. Current flows out of the coupling network and the delay line, through TF2 to +6v which establishes the in-phase output B at a +P level of −5.2v. Output E falls to a −P level of −6.8v because of divider current through the coupling network.

When the input signal to the base of TF4 times out and returns to +1.1v, current through TF4 is increased and the base of TF3 rises to +0.9v. Current flow through TF3 is reduced to zero and TJ4 is forward-biased when its emitter signal falls below −5.2v. Current flows from −12v through TJ4 and into L2 and D1 in parallel to ground which maintains TF2 forward-biased. D2 short circuits the negative excursion of the signal developed by L1. The time base of the signal developed by L1 is greater than that of the input network to insure that the base signal of TF2 is driven positive (current flows through TJ4) before the base of TF1 again falls negative.

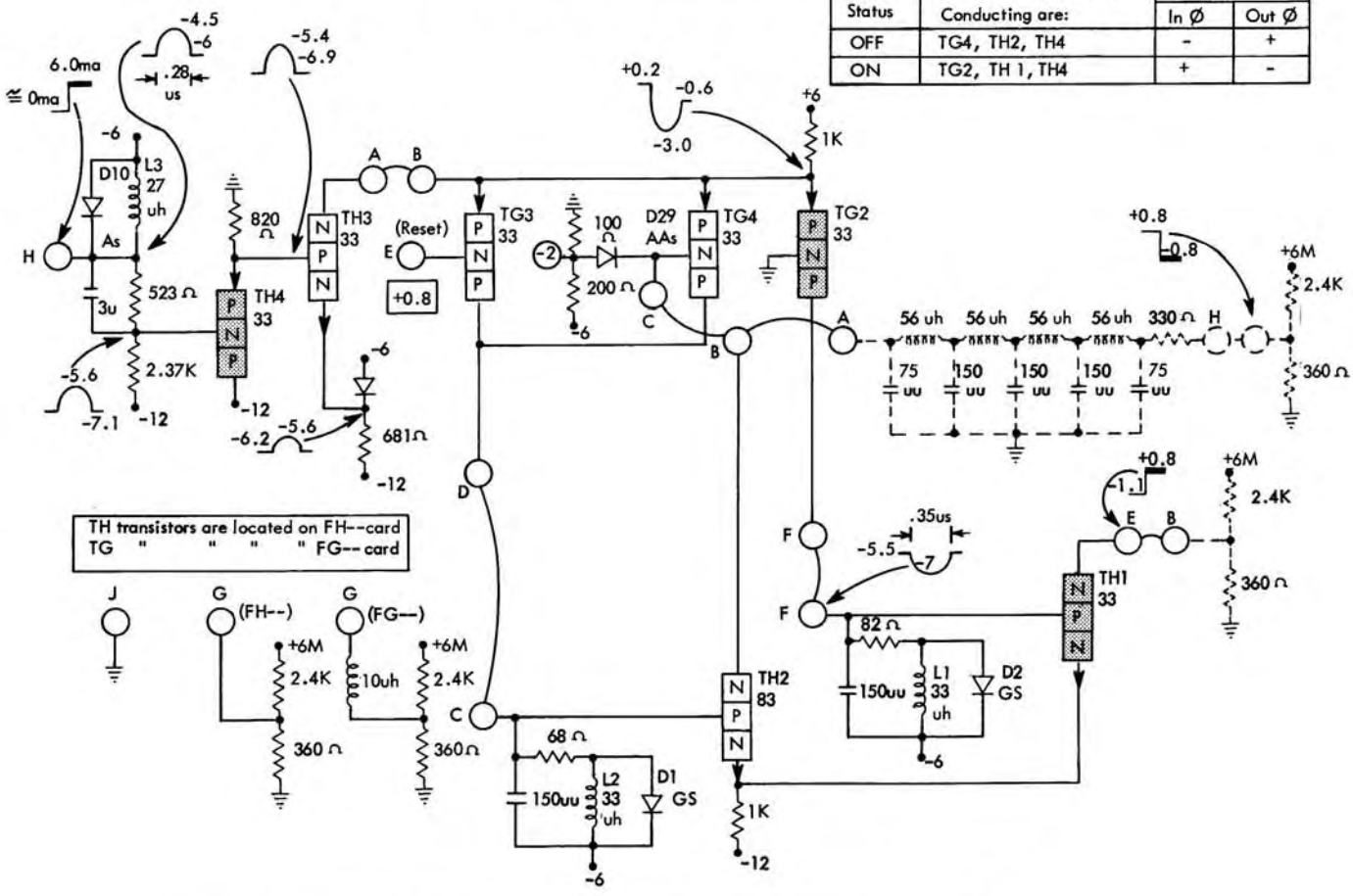
The trigger is now off (in-phase output is +P) and remains in this state until a new current input signal is received. For a turn-on sequence, refer to the sequence chart. Reset is accomplished by a +P signal to input E which forward biases TJ3 and cuts off TJ2. With TJ2 cut off, TF1 cuts off and TF2 turns on.





Sequence		
	Turn Off	TH4 decr→ TH3 on→ TG2 off→ TH1 off→ TH2 on→ Input times out→ TH4 incr→ TH3 off→ TG4 on→ TG4 keeps TH2 on
	Turn On	TH4 decr→ TH3 on→ TG4 off→ TH2 off→ TH1 on, Input times out→ TH4 incr→ TH3 off→ TG2 on→ Keeps TH1 on

Trigger Status	Transistors Conducting are:	Output Level In Ø	Output Level Out Ø
OFF	TG4, TH2, TH4	-	+
ON	TG2, TH 1, TH4	+	-



FH--	371413	Current Mode, Positive Binary, Trigger Card 1
FG--	371414	Current Mode, Positive Binary, Trigger Card 2

Current Mode, Positive Binary Trigger, Cards 1 and 2

The FH - - card and the FG - - card are interconnected to form a plus binary trigger (see logic application). A −N level to input E of FG - - resets the trigger off; the in-phase output is −N and the out-of-phase output is +N. Each +P input to FH - - alters the trigger status, so the first +P input after reset turns the trigger on. The in-phase ouput rises to a +N and the out-of-phase output falls to a −N. Note that when the trigger is on, its in-phase output follows the sign of the function (+TB function has a plus sign and the in-phase output is plus).

The input signal in the logic application consists of a dashed square wave *current* input and an inductive AC voltage resulting from this current input (see note associated with input signal). Such an input is necessary because the design of a binary trigger requires that the trigger operate on AC signals only and be isolated from the DC component of the signals. The input inductive network is designed to develop a positive signal when the input current rises from zero. The fall of the current back to zero has no effect. This trigger is designed to operate at 1 megacycle.

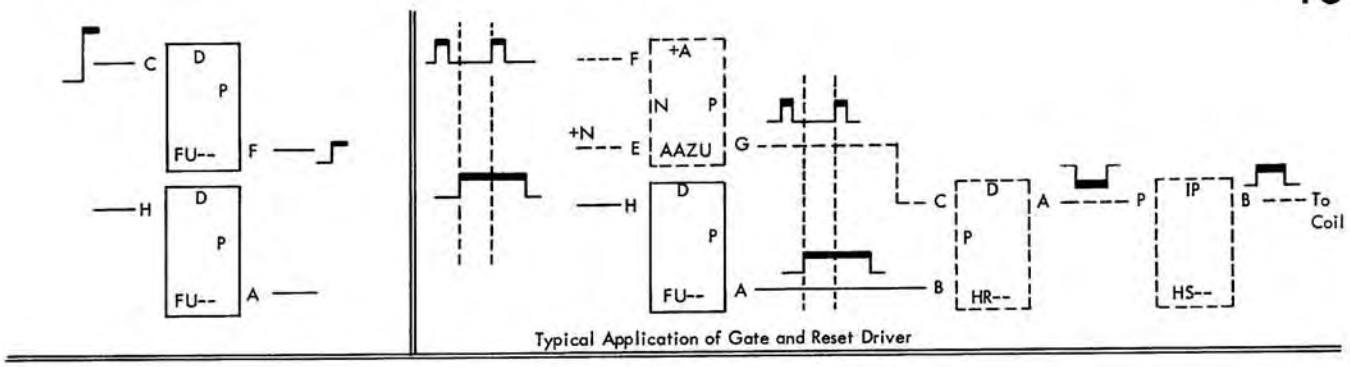
Circuit Description

Before studying the circuit in detail, take an overall look at the schematic. Note the trigger status chart and sequence chart which summarize the over-all sequence of events. The trigger status chart shows that the trigger is on in the state shown (TG2, TH1, and TH4 conducting).

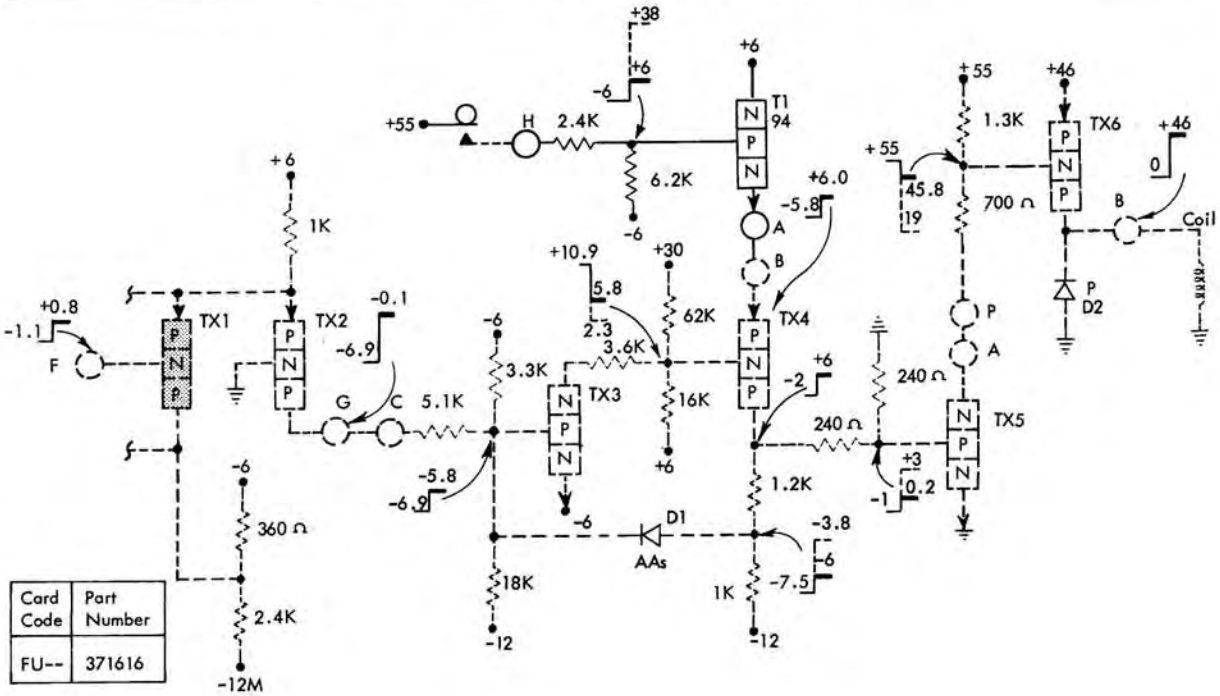
The trigger is flipped by causing current to input H to rise from zero to 6ma. This input causes one component of current to flow from −12v through 2.37K, 523 ohms and 3μfd in parallel to input H and to the positive return of the driving circuit. A second component of current flows from −6v through the 27μh coil L3 to input H. It is the changing current through this coil which develops the 1.5v signal shown. This 1.5v signal is passed by the 3μfd capacitor and the forward bias of TH4 is reduced. The emitter of TH4 follows its base and TH3 conducts when its base rises above −6.2v. Current flows from −12v through 681 ohms, and TH3 to +6v which lowers the emitter of TG2 below ground and cuts off TG2. With TG2 cut off, current flow through coil L1 falls to zero and develops a 1v signal. The base of TH1 falls to −7v which forward-biases TH2 and cuts off TH1. Current flows from −12v through TH2 into the delay line and coupling network which establishes the in-phase output B at a −N level of −0.8v. Output E rises to a +N level of +0.8v because of divider current through the coupling network.

When the input signal to the base of TH4 times out and returns to −7.1v, current through TH4 increases and the base of TH3 falls to −6.9v. Current flow through TH3 is reduced to zero, and TG4 is forward-biased when its emitter signal rises above −0.8v. Current flows from −6v through D1 and L2 in parallel and through TG4 to +6v which maintains TH2 forward-biased. D2 short circuits the positive excursion of the signal developed by L1. The time base of the signal developed by L1 is greater than that of the input network to insure that the base signal of TH2 is driven positive (current flows through TG4) before the base of TH1 again rises positive.
which forward-biases TG3 and cuts off TG2. With TG2 cut off, TH1 cuts off and TH2 turns on.

The trigger is now off (in-phase output is −N) and remains in this state until a new current input signal is received. For a turn-on sequence, refer to the sequence chart. Reset is accomplished by a −N signal to input E.



Typical Application of Gate and Reset Driver



Card Code	Part Number
FU--	371616

Current Mode, Coil Driver Gate and Reset Driver

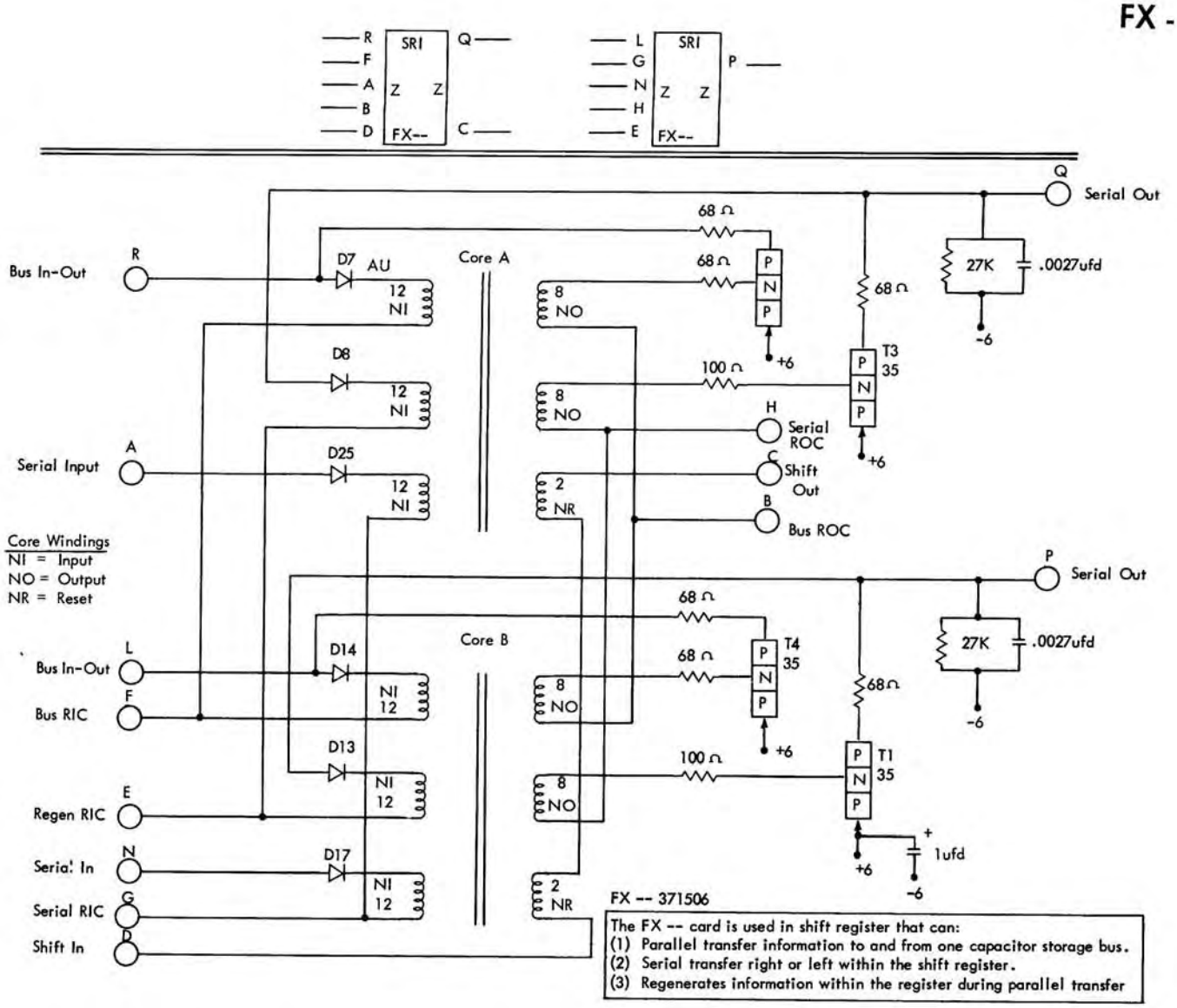
The FU - - card is designed to work with the HR - - coil driver latch circuit. It accepts a +55v input and provides a +6v output to gate the HR - - card (see logic application above). The FU - - card is presented here as a part of a multicard coil driver circuit so over-all function and purpose are better visualized. Driver HR - - develops a negative output when it recognizes a coincidence of plus inputs. Once picked, it latches for the duration of the gate signal fed to its input B. Note that its output pulse length is equal to the remainder of the gate signal fed to input B. Thus, the function of the FU - - driver is to gate HR - - and to drop it out when required. The HS - - card is a power inverter which, when impulsed by HR - -, develops a +46v output and provides enough current to pick a coil.

Circuit Description

As shown, TX1 is forward-biased and TX2 is reverse-biased. Tx3, TX4, and TX5 are reverse-biased because divider currents have established their base levels as shown. T1 and TX6 are reverse-biased by their base return potential. The output of TX6 is 0v and the coil is not picked.

When the CB closes, the base divider of T1 attempts to rise to +38v, but its collector-to-base is forward-biased and the base clamps to +6v. The emitter of T1 follows its base upward so the emitter of TX4 is now gated to receive an input to its base. When the input to TX1 rises, TX2 is forward-biased and TX1 is cut off. Current flow from −12v through 18K, 5.1K, and TX2 to +6v raises the base potential of TX3 and it conducts. Current flow from −6v through TX3, 3.6K and 62K to +30v attempts to lower the base of TX4 to +2.3v which forward-biases TX4. Current flow from −12v through 1K, 1.2K, TX4 and T1 to +6v raises the base level of TX5 and it conducts. The drop across the 1K resistor attempts to raise the anode of D1 to −3.8v which forward-biases D1. Current flows from −12v through 18K, D1, 1.2K, TX4 and T1 to +6v. Thus, the base of TX3 remains forward-biased after TX2 is cut off because TX3 is now latched by D1. This latch is maintained until the +55v CB source is removed. Current flow through TX6 to +55v lowers the base level of TX6 and it conducts. Current flows through the coil and TX6 to +46v and the coil picks. D2 absorbs the coil voltage on dropout.

The circuit is dropped out by opening the CB which lowers the base and emitter potential of T1 to −6v which drops out TX4 and T1. With TX4 cut off, D1, TX3, TX5, and TX6 cut off.



Magnetic Core Shift Register

The FX - - card consists of two magnetic core shift register positions, each capable of storing one bit of information. Each core position has three input windings, a read-out winding and two output windings.

The input windings are driven by core mode Z lines from either a capacitor storage network or from a special bit insert driver. These input windings are gated on by selecting the read-in driver circuits (HG - - or GZ - - cards).

Normally, all reset windings of a shift register are serially connected and receive a constant current read-out pulse from one read-out driver (GY - - card). The output windings are biased by read-out control drivers (HF - - card), that control the status of the output transistors.

The FX - - card contains the basic circuits used to form shift registers of various sizes capable of storing and regenerating data bits within a register; serially transferring data bits right or left within a register; and parallel transferring data bits between two different registers.

Circuit Description

MAGNETIC CORE SHIFT REGISTER OPERATION

Understanding the use of the shift register cards requires knowledge of the magnetic core shift register operation.

Figure FX-1 shows three positions of a theoretical magnetic core shift register and illustrates the principle of serial shifting and regeneration of a stored bit within the register position. Each core position consists of a transistor, three diodes, a capacitor storage network, and a magnetic core and its associated windings. The transistor is used with the output winding to charge the capacitor without excessive core loading. The diodes in the input winding circuits provide isolation from the read-in driver circuits.

Normal shift register operation is at 250kc and consists of alternated read-out and read-in pulses to the core position. A 4 microsecond duty cycle pattern consisting of a A, B, C, and D pulse, each 1 microsecond wide, is

normally used in shift register operation. The read-out pulse is a constant current signal used to reset all cores to zero at A time of each cycle. A constant voltage read-in pulse occurs at C time to set a core if a read-in control driver is gated on. Data may be read into a shift register from other logic circuits by use of a bit insert driver or can be parallel transferred into the register.

Cycle 1 Serial Shift Right (Figure FX1). Assume that core position 2 is set on and it is necessary to move this information bit to the right to core position 3. At A time, the read-out driver (ROD) is gated on and provides a constant current pulse to the serially connected read-out windings and resets all cores off.

The read-out control driver (ROCD) for each position is gated on and sets the base level of all output transistors to +6.5v so that if a core is switched the transistors are turned on. When core 2 is flipped to the reset state at A time, about 5v is induced in the output winding of core 2, and T2 is forward-biased on. The 68 ohm collector resistor permits the transistor to saturate quickly, reducing the power dissipation within T2 and allowing the capacitor C2 to rapidly charge to +6 volts. The capacitor is shunted by a 27K resistor that insures that the capacitor is not charged by the I_{co} current through the transistor when it is held off. The capacitor is a temporary storage between read-out and read-in pulses and provides a means of sampling core status.

At read-in-time (C time), the right shift read-in driver (RIC) is gated on and provides a −6v output. Discharge current from −6v through the input winding of core position 3 to C2 (+6v) is sufficient to set core 3 on. Information from core 2 is serially shifted right from core 2 to core 3. During this same time core 1 and core 3 are read out and also shift information bits to the right if they originally contained a stored bit.

Cycle 2 Serial Shift Left (Figure FX-1). Assume that core 2 is set on and it is necessary to shift the information to the left to core 1. Circuit operation for the read-out of core 2 and the charging of C2 are identical to those of cycle 1. At A time all circuits are reset off. With the ROCD on (+6.5v), T2 conducts and charges the capacitor (C2) to +6v. At read-in time, however, the serial left shift read-in control is gated on and provides a −6v output. Conduction through the left shift input windings of core 1 to C2 discharges the capacitor and sets core 1 on. Thus, information from core 2 was shifted left to core 1.

Cycle 3 Regeneration (Figure FX-1). In normal operation, a constant read-out and regeneration feature allows dynamic sensing for indicators and sampling. Again, assume core 2 is set on. At read-out time all cores are reset off. With the ROCD on, the voltage developed in the output winding is enough to drive T2 into saturation and charge C2 to +6v. At read-in time, the regeneration read-in driver is gated on and provides a −6v output. Discharge current through the regeneration input winding of core 2 discharges C2 and sets core 2 on. Information was read out for sampling and then read back into its original core position.

Serial-Parallel Transfer (Figure FX-2). Serial transfer takes place within a given register. Parallel transfer moves the entire contents of one register to the bus capacitor storage circuits, where the information can be sampled or transferred to another register. To parallel transfer between registers it is essential that the registers share common bus capacitor storage circuits.

The theoretical circuit shown in Figure FX-1 cannot accomplish both serial and parallel transfer of information. By adding a second output circuit and an additional input winding to each core position, both types of transfers are accomplished.

Figure FX-2 shows a portion of two shift registers that share common bus capacitor storage circuits. The core positions shown are bit positions within a particular digit of information (for example, 0 bit positions of digits 1 and 2).

A parallel transfer of information bits between register I and register II is made as follows. Assume core 1 of shift register I is set on and it is desired to parallel-shift this information bit to core 1 of shift register II. At read-out time all core positions are reset off. Register I serial ROCD and bus ROCD circuits are on (+6.5v) and permit both transistors (T1 and T2) to conduct when core 1 is reset off. Current flow to the serial capacitor C1 and to the bus capacitor C2 charges both capacitors to +6v.

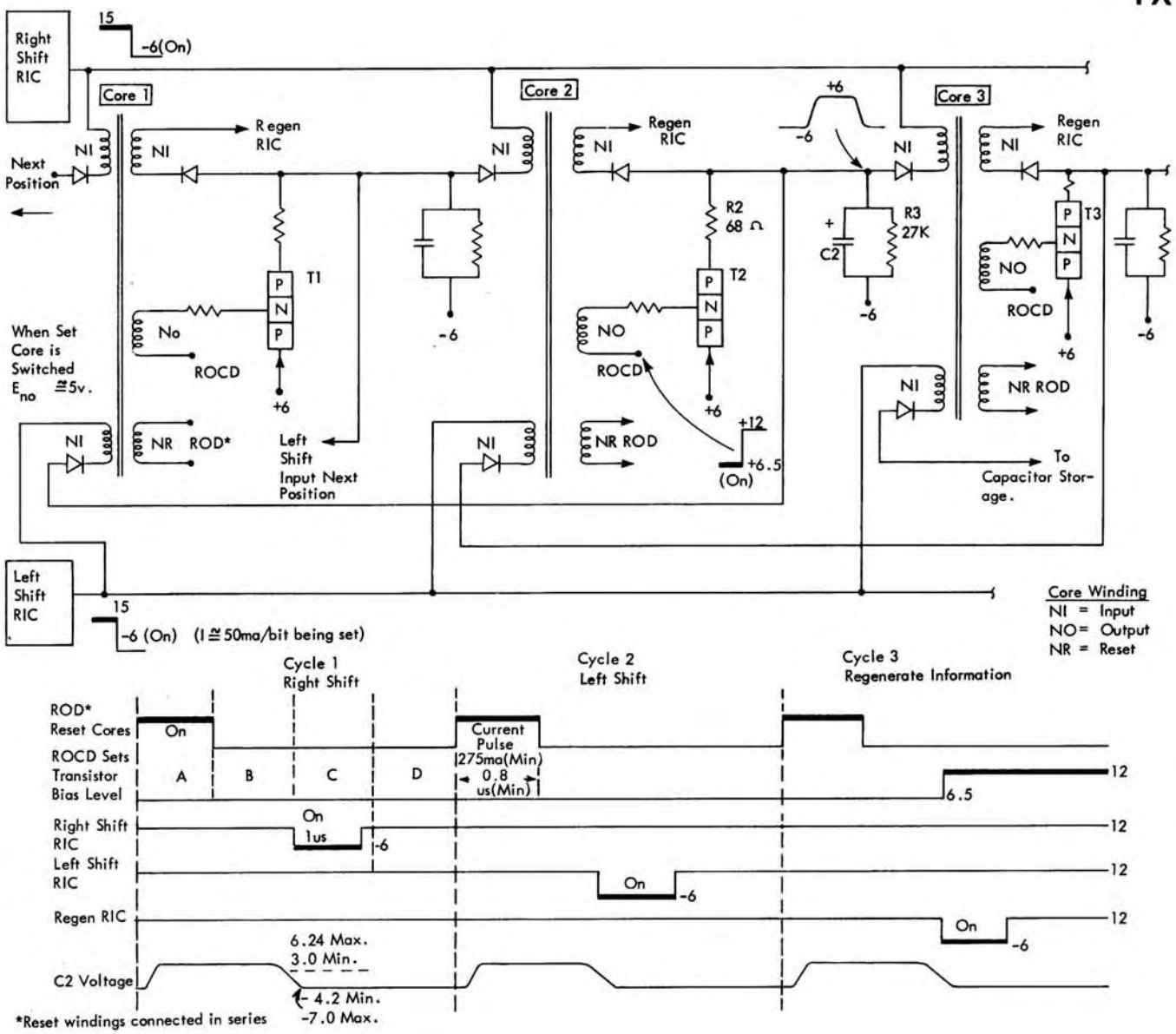
Because register II is to receive the information from register I, it must be cleared during the read-out cycle. This requires that both the serial ROCD and bus ROCD for register II remain off (+12v).

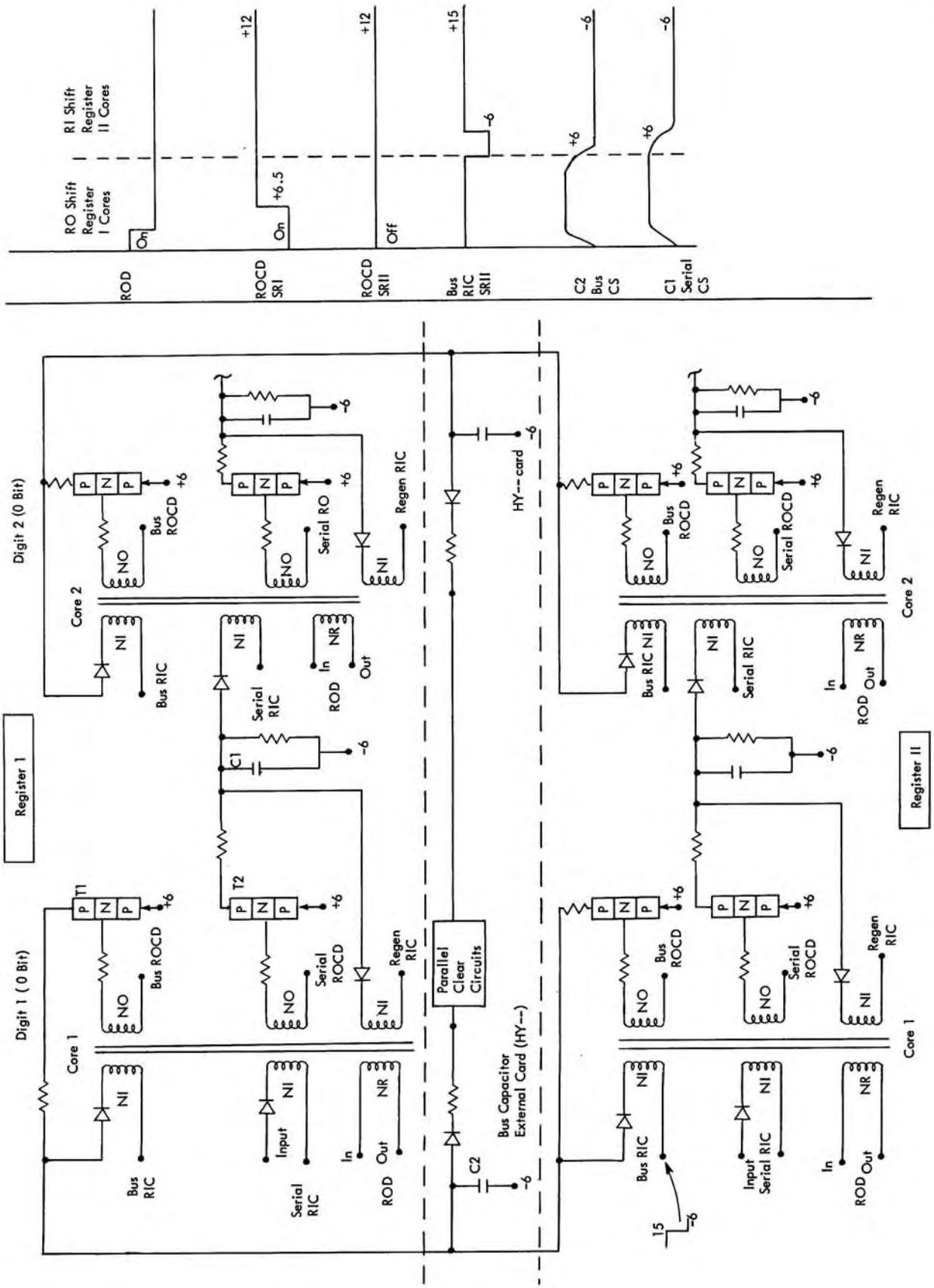
Thus, at read-out time the cores of register II are reset without charging any capacitors because the transistors are held reverse-biased off.

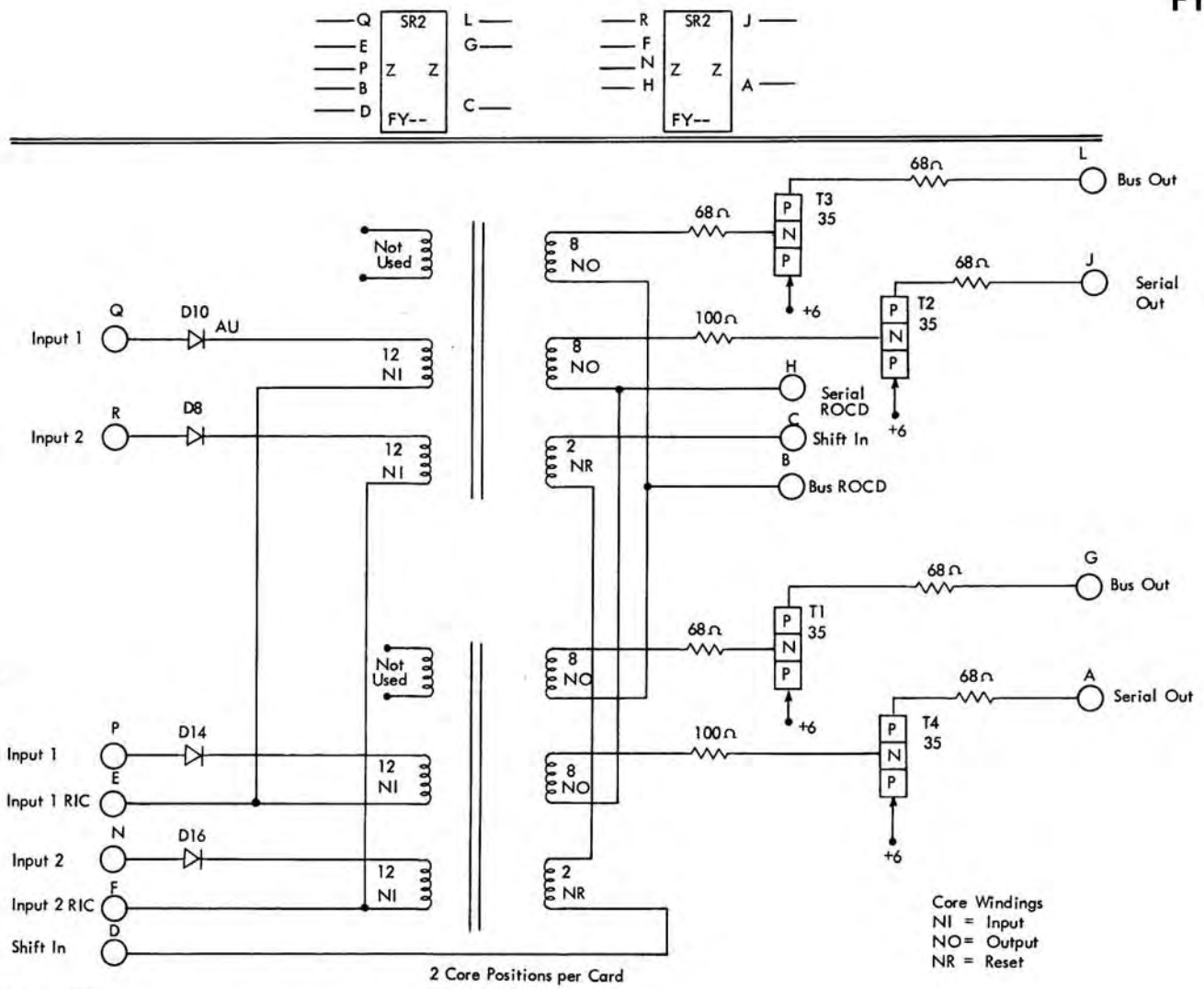
At read-in time, the bus read-in control for register II is turned on (−6v), allowing current flow through the bus input winding of register II (core 1), the isolation diode, to C2 to discharge the capacitor and set core I of register II. Also during read-in time, the information bit stored in C1 of register I may be either regenerated back into core 1 or serially shifted as described previously. On the parallel transfer, if a read-in driver is not gated on to discharge the bus storage capacitor, a special parallel clear line is gated on each cycle to discharge the capacitors. This action prevents the transistor I_{co} from charging the capacitor after a given period of time.

Application

The magnetic core shift register system described is designed to handle the ten-digit 2-of-5 bit word transfers in the 7070. Other coding arrangements and register sizes are possible as long as the driver ratings are not exceeded.


Right Shift RIC
15
-6(On)
Core 1
Core 2
Core 3
Regen RIC
NI
Next Position
No
ROCD
T1
T2
T3
P
N
P
+6
-6
When Set Core is Switched E_{no} ≅5v.
NR ROD*
Left Shift Input Next Position
NO
R2 68 Ω
R3 27K
C2
+12
+6.5
(On)
NR ROD
To Capacitor Storage.
Left Shift RIC
-6 (On) (I ≅ 50ma/bit being set)
Core Winding
NI = Input
NO = Output
NR = Reset
Cycle 1 Right Shift
Cycle 2 Left Shift
Cycle 3 Regenerate Information
ROD* Reset Cores
ROCD Sets Transistor Bias Level
Right Shift RIC
Left Shift RIC
Regen RIC
C2 Voltage
A
B
C
D
On
1us
Current Pulse 275ma(Min)
0.8 us(Min)
6.5
12
6.24 Max.
3.0 Min.
4.2 Min.
-7.0 Max.
*Reset windings connected in series


RO Shift Register I Cores
RI Shift Register II Cores
On
+12
+6.5
On
+12
Off
+15
-6
+6
-6
+6
ROD
ROCD SRI
ROCD SRII
Bus RIC SRII
C2 Bus CS
C1 Serial CS
Digit 2 (0 Bit)
Digit 1 (0 Bit)
Register 1
Register II
Core 1
Core 2
P N P
NO
NI
NR
T1
T2
C1
C2
Bus ROCD
Serial RO
Serial ROCD
Regen RIC
Bus RIC
Serial RIC
Input
In
Out
ROD
HY-- card
Parallel Clear Circuits
Bus Capacitor External Card (HY--)
15



FY-- 371507

The FY-- is used to expand the inputs to the FX-- card.

Magnetic Core Shift Register Extender SR2

The FY - - card expands the number of inputs to the FX - - card. Two magnetic core positions are mounted on each card; each position is capable of storing one bit of information. Each core position contains two input windings, two output windings, and a reset winding.

The input windings are driven by core mode Z lines from either a capacitor storage network or from a special bit insert driver. These input windings are gated on by selecting the read-in driver circuits (HG - - or GZ - - card).

Normally, all the reset windings of a shift register are serially connected and receive a constant current read-out pulse from a read-out driver (GY - - card). The output windings are biased by a read-out control driver (HF - - card), which controls the bias level of the output transistors.

Circuit Description (Extender Operation)

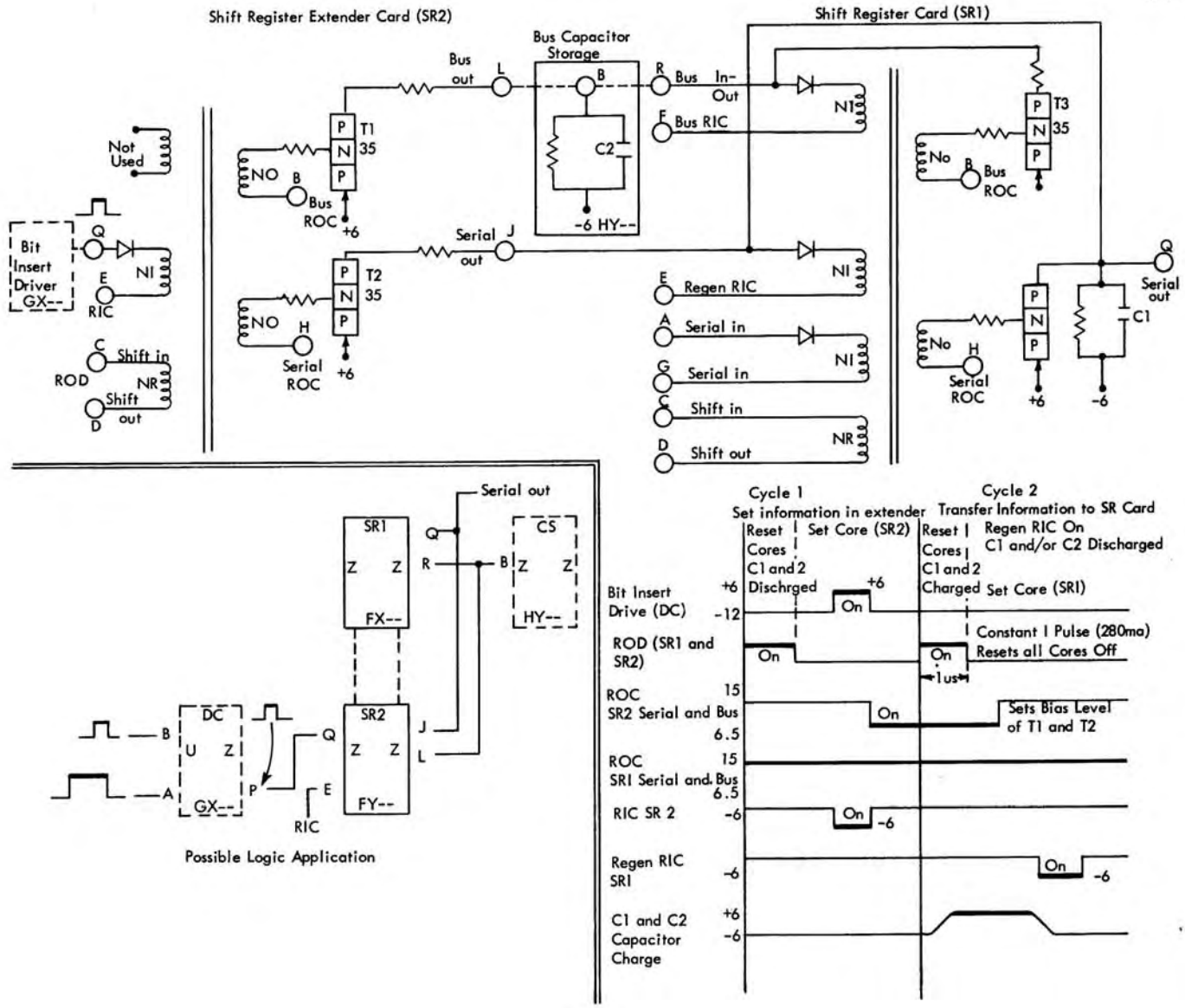
Figure FY-1 shows a part of the SR2 card extending the inputs to an SR1 card. Note that the serial and the bus outputs of the two cards are commoned and feed the register capacitors of the SR1 card. The two core positions function as a single core with an increased number of inputs.

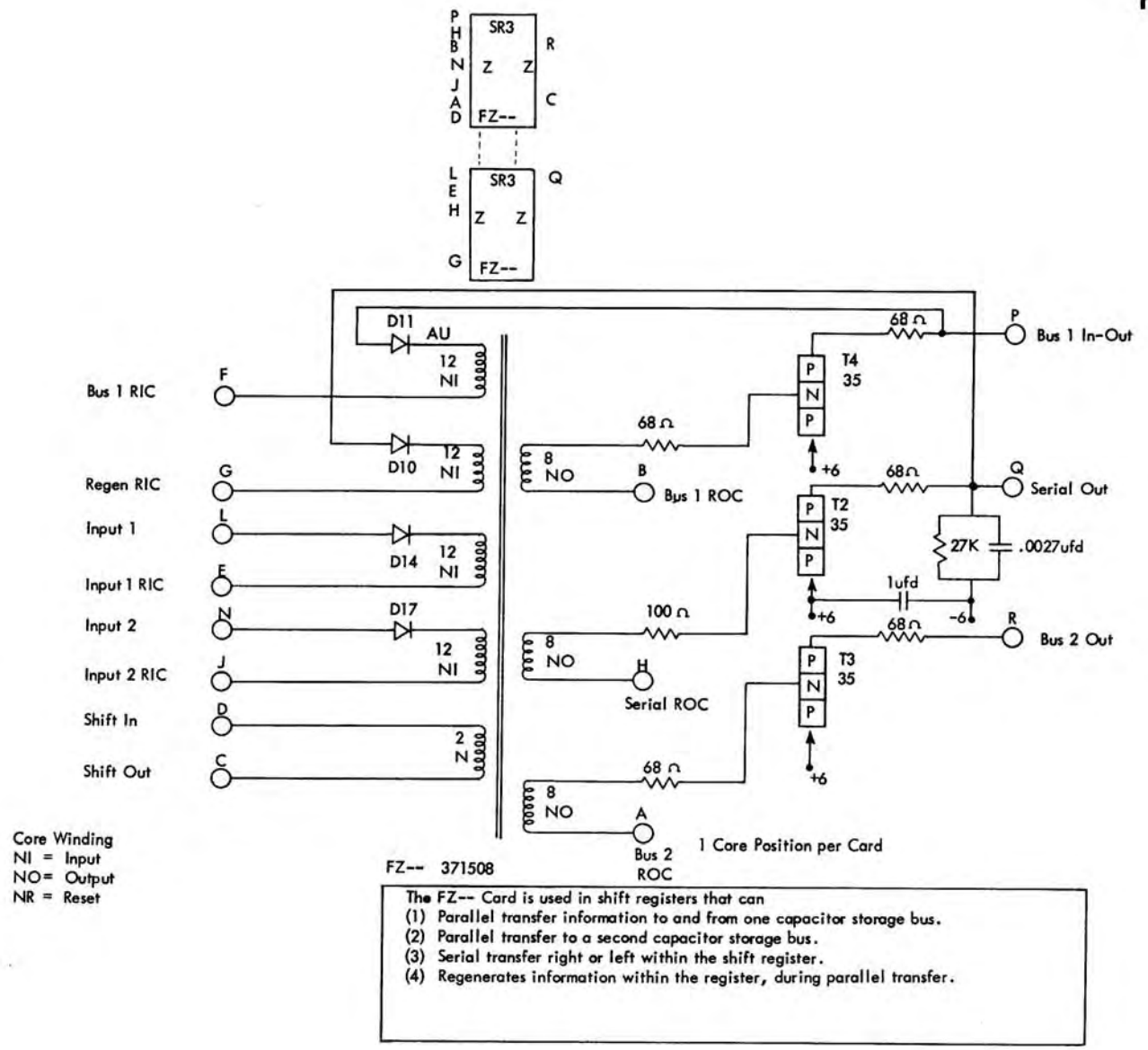
During cycle 1 (Figure FY-1) the read-out driver (ROD) is gated on and resets both core positions to the off status. At this time, the serial and bus read-out control drivers are off for both the SR2 and SR1 output windings and prevent the output transistors from turning on. C1 and C2 remain discharged.

At read-in time, the bit insert driver and the read-in control (RIC) of the SR2 core input winding are gated on. Enough current flows through this winding to set the SR2 core on. All read-in controls for the SR1 core remain off during this cycle.

The ROD is again turned on in cycle 2 and resets both cores off. The serial and bus read-out control for the SR2 core are now on. When the SR2 core is switched off, about 5v is induced in the output windings. T1 and T2 are biased on and charge the bus and serial capacitors associated with the SR1 card to +6v. At read-in time of cycle 2, the capacitors are discharged to regenerate the information bit in the SR1 core, or the information bit may be serial or parallel transferred to another core position.

A bit was thus read into the extender core during cycle 1 and transferred to the register card during cycle 2.


Shift Register Extender Card (SR2)
Shift Register Card (SR1)
Bus Capacitor Storage
Bus out
Bus In-Out
Bus RIC
Not Used
Bit Insert Driver GX--
RIC
Shift in
Shift out
ROD
NO
Bus ROC
Serial out
Serial ROC
Regen RIC
Serial in
Shift in
Shift out
No
C1
C2
-6 HY--
+6
-6
T1
T2
T3
35
NI
NR
Possible Logic Application
SR1
SR2
FX--
FY--
GX--
HY--
CS
DC
Cycle 1
Set information in extender
Reset Cores C1 and 2 Dischrged
Set Core (SR2)
Cycle 2
Transfer Information to SR Card
Reset Cores C1 and 2 Charged
Regen RIC On C1 and/or C2 Discharged
Set Core (SR1)
Bit Insert Drive (DC)
ROD (SR1 and SR2)
Constant I Pulse (280ma) Resets all Cores Off
1us
ROC SR2 Serial and Bus
Sets Bias Level of T1 and T2
ROC SR1 Serial and Bus
RIC SR 2
Regen RIC SR1
C1 and C2 Capacitor Charge
On



The FZ-- Card is used in shift registers that can
(1) Parallel transfer information to and from one capacitor storage bus.
(2) Parallel transfer to a second capacitor storage bus.
(3) Serial transfer right or left within the shift register.
(4) Regenerates information within the register, during parallel transfer.

Magnetic Core Shift Register SR3

The FZ - - card is a single magnetic core position used to store an information bit. This shift register card consists of four input windings, a read-out winding, and three output windings.

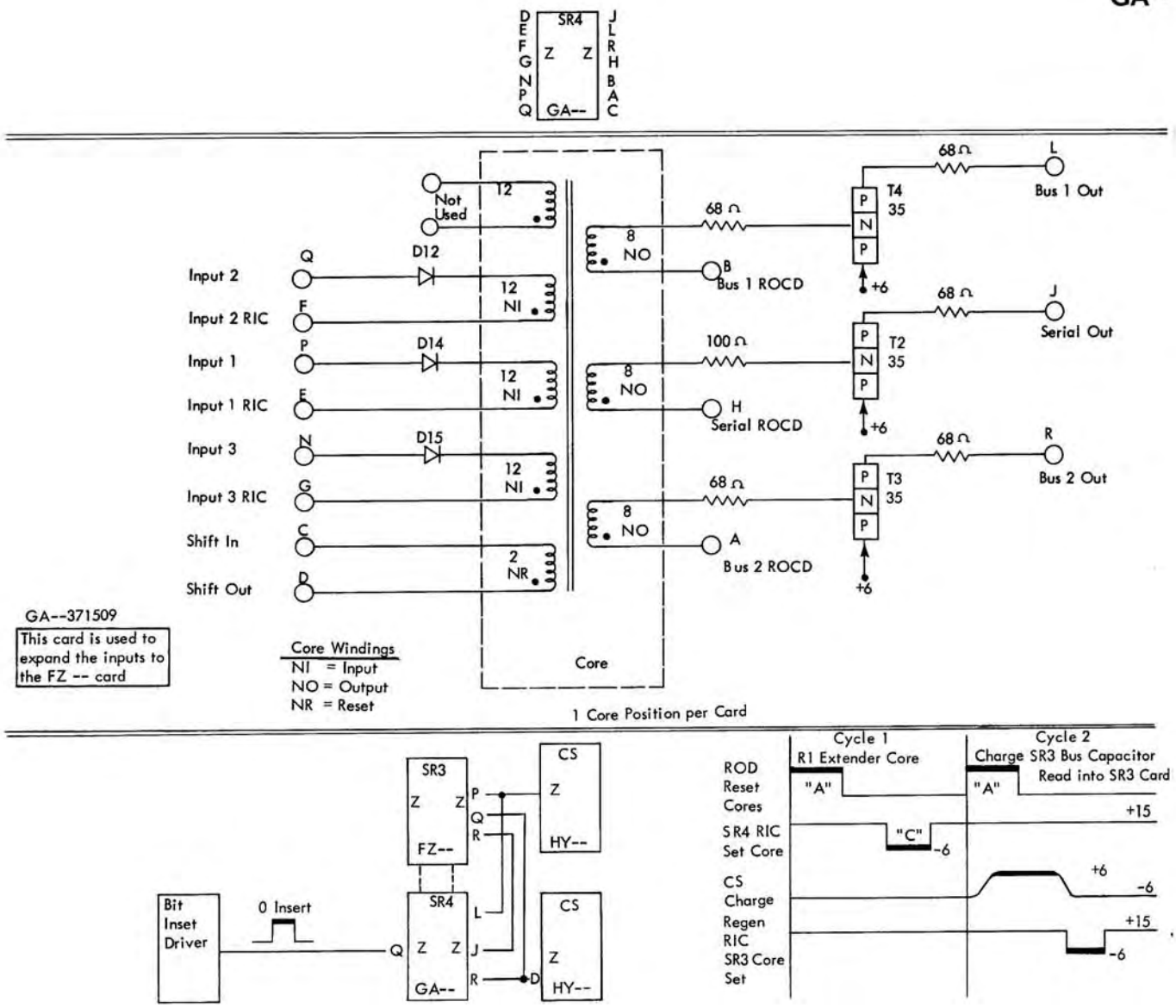
The input windings are driven by core mode Z lines from either a capacitor storage network or from a special bit insert driver. These input windings are gated on by selecting the read-in driver circuits (HG - - or GZ - - card).

Normally, all reset windings of a shift register are serially connected and receive a constant current read-out pulse from a read-out control driver (GY - - card). The output windings are biased by a read-out control driver (HF - - card), and control the status of the output transistors.

The serial output at pin Q allows the FZ - - card to serial shift or regenerate information bits in the register position. The Bus 1 and Bus 2 outputs at pins P and R allow parallel transfer of information to either of two other registers. Shift register operation for this card is similar to that for the FX - - card.

Application

The FZ - - card allows additional flexibility in designing magnetic core shift registers. It provides a core position that can be set by any one of several inputs without using an extender card. This card also permits parallel read-out to 1 of 2 bus lines along with the normal serial transfer and regeneration feature provided by the FX - - card.



Magnetic Core Shift Register Extender SR4

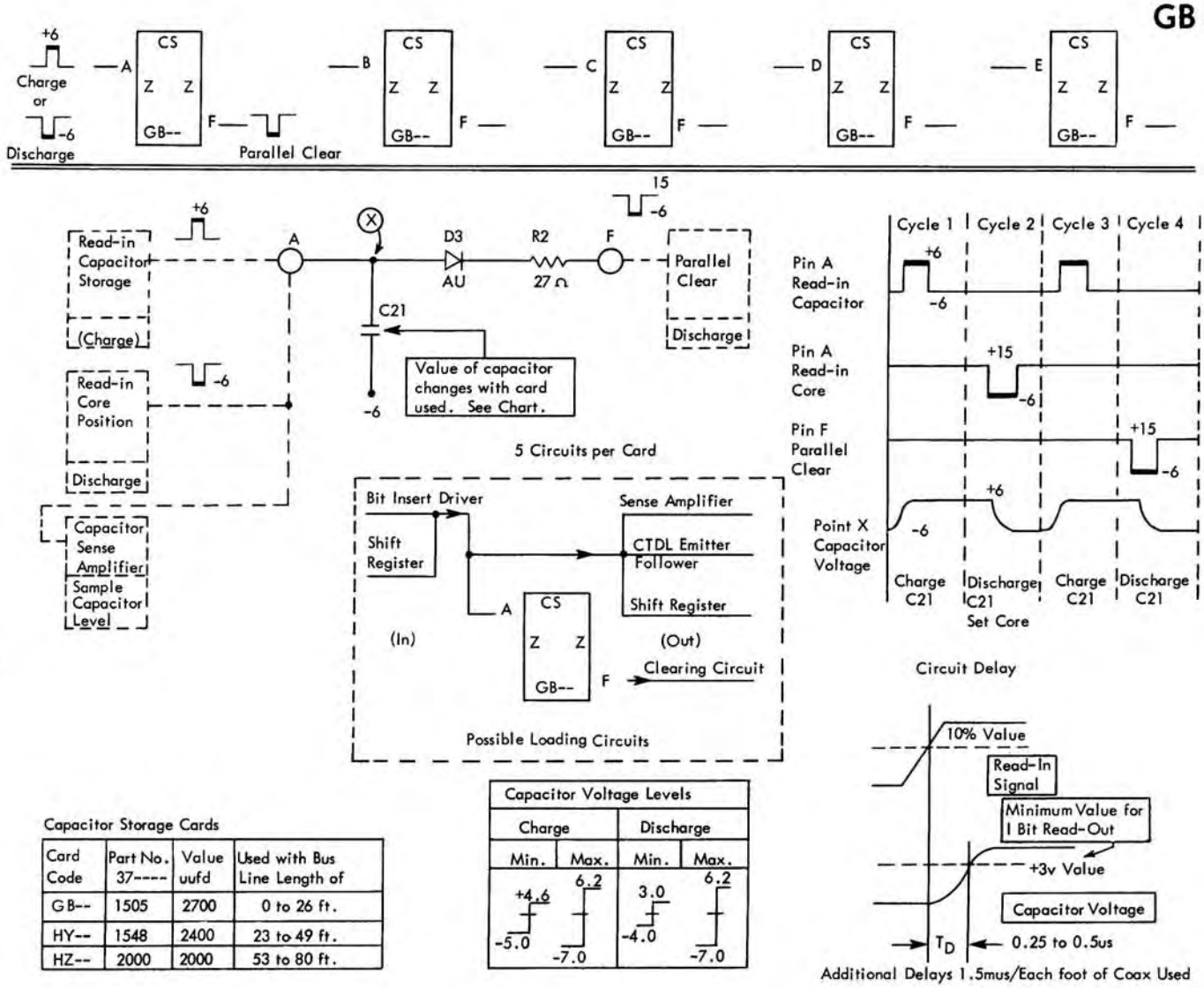
The GA - - card is a single magnetic core position used to expand the number of inputs to the FZ - - card. Each core position has three input windings, three output windings, and a reset winding.

The input windings are driven by core mode Z lines from either a capacitor storage network or from a special bit insert driver. These input windings are gated on by selecting the read-in driver circuits (HG - - or GZ - - card).

Normally, all reset windings of a shift register are serially connected and receive a constant current read-out pulse from a read-out driver (GY - - card). The output windings are biased by a read-out control driver (HF - - card) and control the status of the transistors they are connected to.

When this card is used to extend the FZ - - card, the output pins from this extender card are tied to the respective output pins of the FZ - - card. The two core positions now function as one core with eight different inputs. For example, in the logic application shown above, the bus 1 output (pin L of the SR4 card)is tied to the bus 1 output(pin P) of the SR3 card. During cycle 1, read-in to the extender card by the bit insert driver takes place and sets the core on. At A time of cycle 2 the cores are reset off in both the SR3 and the SR4 cards. When the SR4 core switches off, it charges the SR3 register capacitors to +6v. After the capacitors are charged, read-in control drivers can be selected to regenerate the information bit in the SR3 card; serial transfer the information bit within the register; or parallel transfer the bit to 1 of 2 other registers.

For a detailed description of the extender operation, refer to the FY - - card.



Capacitor Storage Cards

Card Code	Part No. 37----	Value uufd	Used with Bus Line Length of
GB--	1505	2700	0 to 26 ft.
HY--	1548	2400	23 to 49 ft.
HZ--	2000	2000	53 to 80 ft.

Capacitor Voltage Levels

Charge		Discharge	
Min.	Max.	Min.	Max.
+4.6	6.2	3.0	6.2
-5.0	-7.0	-4.0	-7.0

Capacitor Storage

The GB - - card consists of five capacitor storage circuits, each capable of storing one binary bit because of its two possible states, charged and discharged. Normal input to the capacitor storage card is from the parallel output of a register or from a bit insert driver. Capacitor storage status is detected by sensing the voltage level on the capacitor. Capacitor storage outputs drive core register bit positions, sense amplifiers or CTDL emitter followers. The capacitor charge may be removed by a special clearing circuit tied to pin F.

Circuit Description

Assume the capacitor storage circuit is connected as above and that the capacitor is discharged (−6v).

Cycle 1, Charge Capacitor. When the read-in capacitor circuit is gated on (+6v), conduction from C21 (point X) to the read-in capacitor storage circuits charges the capacitor to +6v.

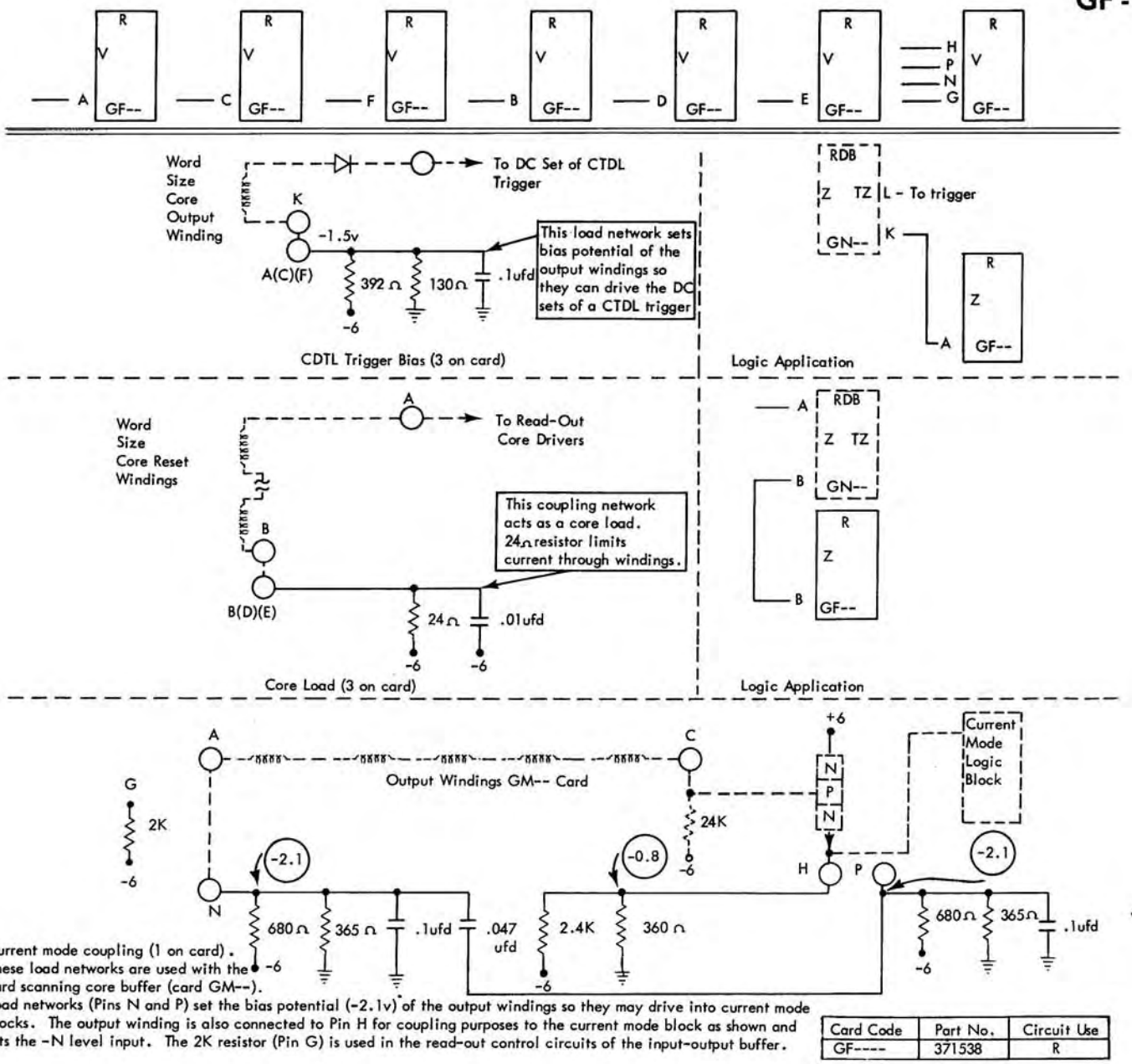
Cycle 2, Discharge Capacitor. The capacitor charge remains at +6v and may be sampled for system use until the read-in core driver circuit drops the voltage at pin A to −6v. The capacitor discharges to this value and the resulting discharge current flow is enough to set a magnetic core of a shift register position to the 1 state.

Cycle 3, Charge Capacitor. Again the read-in capacitor storage circuit causes the voltage at pin A to increase to +6v and charges the capacitor to this value.

Cycle 4, Discharge Capacitor. To prevent the capacitor from being charged by the Ico of the shift register transistor, the parallel clear line is gated on at the end of each read-out cycle to discharge the capacitor. Discharge current from pin F, R2, and forward-biased D3 reduces the voltage at point X to −6v.

Application

In the 7070 system, these cards serve as bus capacitors for transferring information to and from the magnetic core shift registers or memory. The pulse duration of the capacitor charge varies from 2 to 4 microseconds depending on circuit use. Storage cards are used in both 4 and 6 microsecond transfer cycles. To compensate for line capacitance, three capacitor cards (noted in chart) are available for driving different length bus lines.



Current mode coupling (1 on card). These load networks are used with the card scanning core buffer (card GM--).
Load networks (Pins N and P) set the bias potential (-2.1v) of the output windings so they may drive into current mode blocks. The output winding is also connected to Pin H for coupling purposes to the current mode block as shown and sets the -N level input. The 2K resistor (Pin G) is used in the read-out control circuits of the input-output buffer.

Card Code	Part No.	Circuit Use
GF----	371538	R

Bias, Load, and Coupling Networks

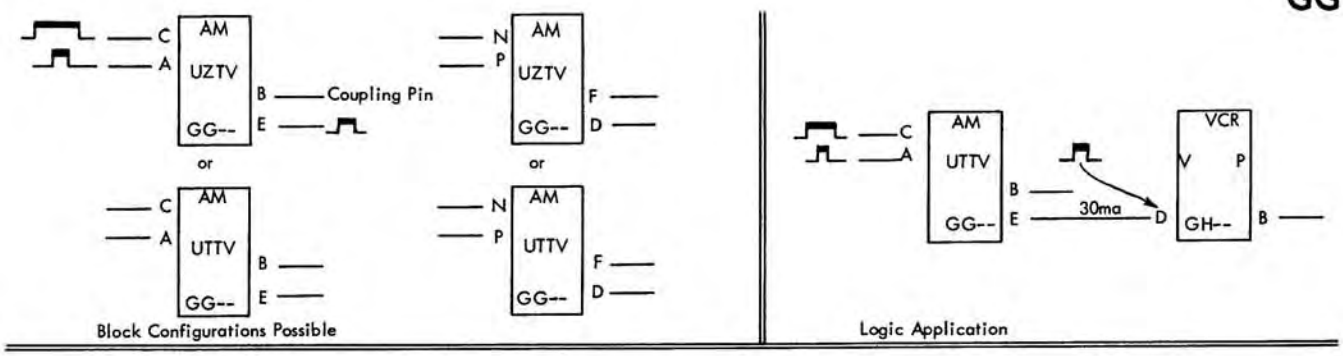
The GF - - card consists of seven resistor-capacitor networks designed for use with the magnetic core input-output buffer cards. These networks serve as bias, load, and coupling circuits for the various windings and circuitry associated with the output core cards.

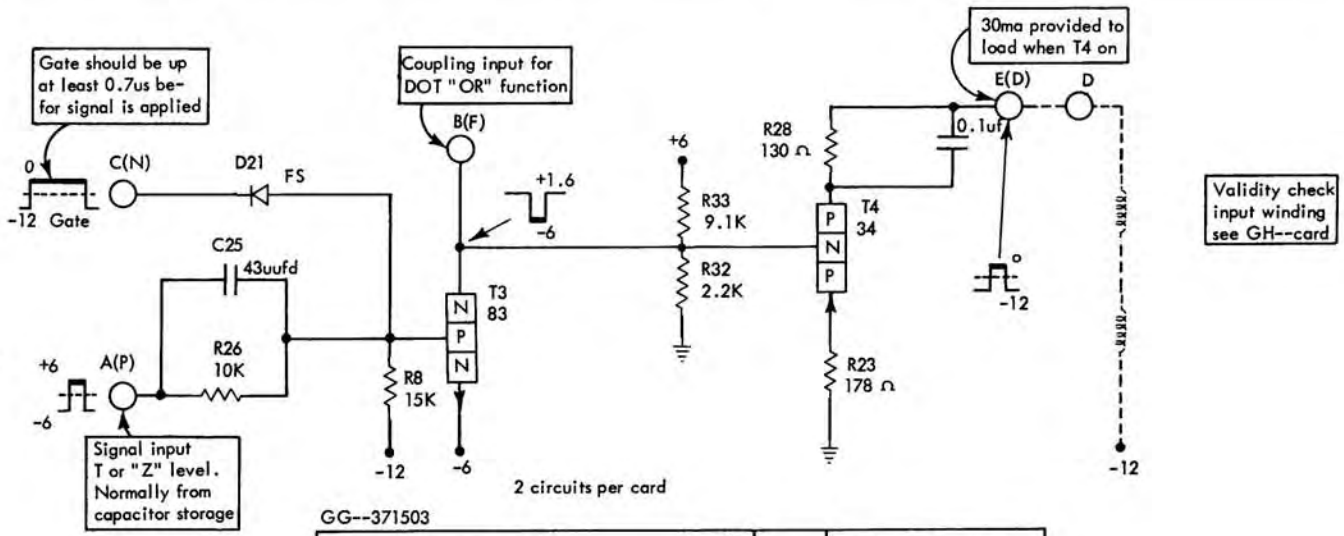
Circuit Description

Typical applications of these networks are illustrated. Circuits with input pins A, C, and F are usually tied to the output windings of the word-size core card (GN - -). The output windings are biased at −1.5v by the divider network. When the core is switched, about 5v is induced in the output which is enough to overcome this bias and to permit direct drive to CTDL trigger circuits. The 0.1μfd capacitor filters transient spikes caused by core switching.

Circuits with input pins at B, D, and E serve as core loads that limit the current through the core windings. The 0.01μfd capacitor across the 24 ohm resistor, filters the transient spikes resulting from core switching.

In the card scanning core buffer application (GM - - card), additional networks are used to obtain a current mode output for driving into logic circuits. The output windings are biased to −2.1v by the connection to pin N or pin P. When a core is switched, about 5v is induced in the output windings. This voltage is enough to overcome the bias potential of the output windings and gives a current mode signal at the base of the transistor. The transistor is normally biased off, because the emitter load (pin H) is set at −0.8v. When the core is switched, the transistor turns on and the current mode output drives into the logic blocks. The 0.047 μfd capacitor between the divider networks stabilizes the voltage at pin N and pin P. The 2K resistor (pin G) is used as a load for the read-out core drivers (not shown above, see GLVH or GLVG cards).





GG--371503

Input Levels						On Output Current	Delays (usec)		
Gate "U" Line		Signal "T" Line		Signal "Z" Line				Per	Circuit
Min.	Max.	Min.	Max.	Min.	Max.				
-5.5	+0.2 to -7.4 / -12.5	2.7	6.2 to -4.0 / -6.2	2.7	6.2 to -4.0 / -6.2	30ma	Turn On	Min.	0.1
								Max.	0.35
							Turn Off	Min.	0.2
								Max.	1.1

Capacitor Sense Amplifier and Driver

The capacitor sense amplifier and driver is used to sense the core register level or amplify a CTDL T line.

There are two identical sense circuits on the GG - - card. Both the gate input and signal input must be up to obtain 30ma of drive current in the output circuit. These drivers supply the current to validity check circuits or to modified core register positions.

The U level gate input (pin C) is driven by a CTDL logic block or an emitter follower and controls the bias potential at the base of T3. The gate is set 0.7μs before the signal input is applied at pin A. Values for the gate and signal inputs are shown on the circuit diagram.

Circuit Description

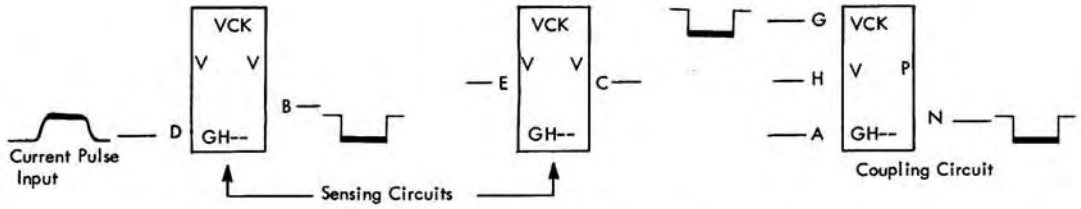
Gate Down-Signal Input Up or Down. Assume that the signal input is up (or down) and the gate input is down (−12v). Conduction through D21 and R26 sets the base of T3 to the −12v gate level. T3 is reverse-biased and off. With T3 off, the collector goes to 1.2v which is set by the divider network of R32 and R33. T4 is reverse-biased off and no current flows in the output circuit.

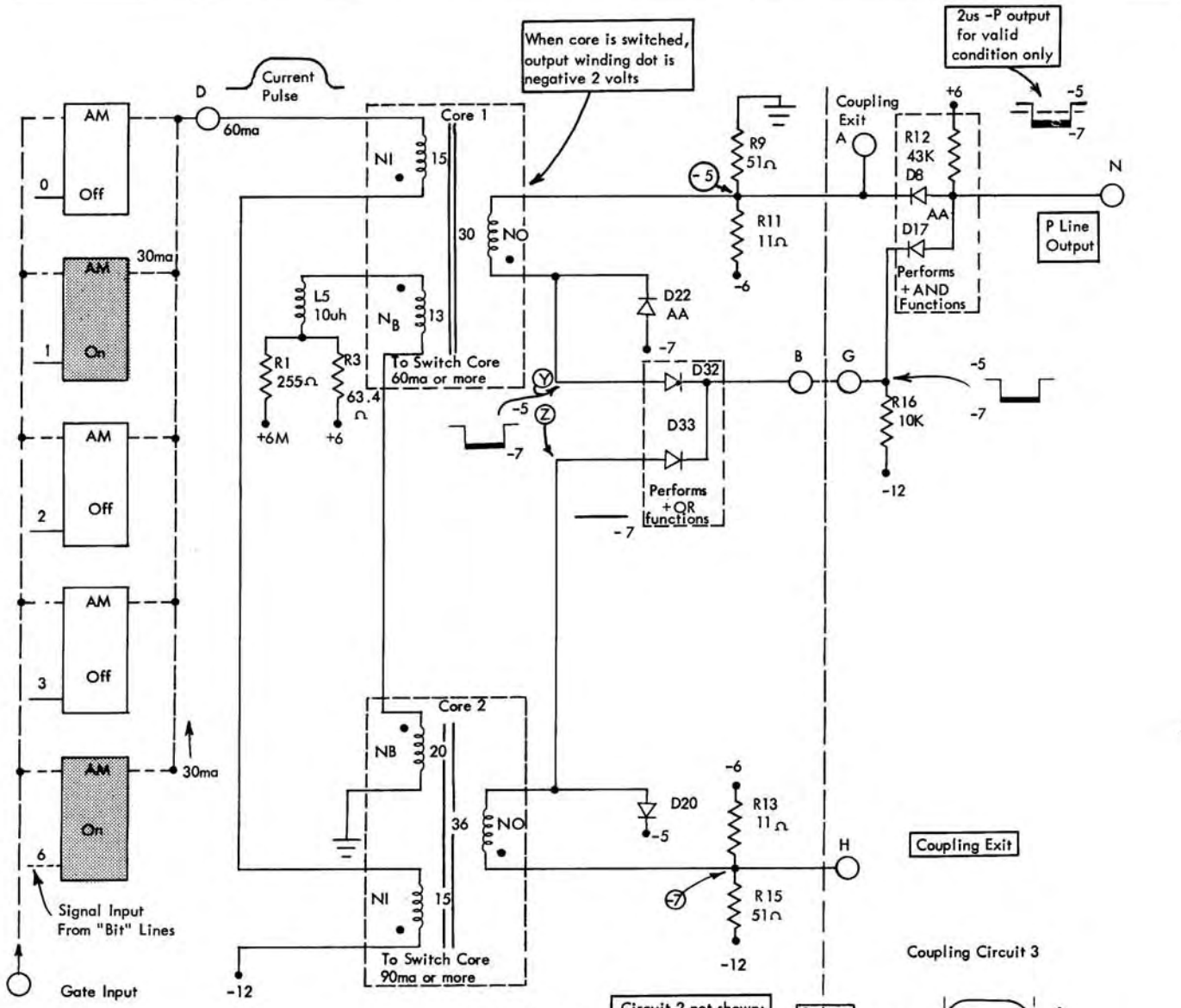
Gate Up-Signal Input Up. When coincidence of the up gate level and the up signal level occurs, conduction through R26 and D21 drops the base level to 0v. T3 becomes forward-biased and conducts. The collector of T3 drops to −6v and forward-biases T4 on. With T4 on, 30ma of current is supplied the output load. The divider network of R33 and R32 acts as a speed-up network and prevents T4 from being reverse-biased too far in the off direction. This divider also limits the amount of reverse voltage across the collector to the base junction of T4 during the reset time of the validity check circuit.

Application

These drivers furnish 30ma of current to a modified core register circuit or to a validity check circuit when the input winding of these circuits is returned to −12v.

A DOT OR function is performed by coupling unloaded capacitor sense amplifier outputs to pin B. A maximum of two capacitor sense amplifier circuits may be coupled to provide a three-way OR function driving into T4 (see HBWW cards).





GH-- 371504

No. of Bits at Sense Amplifiers	VCK Input Current	Core Switched		Voltage at		VCK O'pt
		Core 1	Core 2	Y	Z	
0	0	No	No	-5	-7	+P
1	30	No	No	-5	-7	+P
2	60	Yes	No	-7	-7	-P
3	90	Yes	Yes	-7	-5	+P
4	120	Yes	Yes	-7	-5	+P
5	150	Yes	Yes	-7	-5	+P

T1 (Turn-on delay)= .10 to .38 us
T2 = 1.8 us when T3 = 1.93 us.

Magnetic Core 2-of-5 Bit Validity Check Cards

The GH - - cards are found in validity check circuits. These circuits check for valid information, coded in the 2-of-5 bit code, on either a serial or parallel transfer of information. Three circuits are located on each card, two sensing circuits and one coupling circuit. The two sense circuits are identical, each consisting of two magnetic ribbon cores and a diode "mix." The coupling circuit is composed of a resistor network and a diode switch.

The validity check circuits (VCK) furnish a 2μs −P output for a valid input of two and only two bits, and a +P output for an error condition due to an invalid input of more or less than two bits. For each digit position to be checked, five capacitor sense amplifier drivers (CG - - card) are coupled together to feed the input windings of the VCK card. Each amplifier that senses an information bit provides 30ma to the VCK input. The total to the VCK input sets either an error or no-error condition of the output P line.

Core Bias and Setting. In the static state, about 50ma of current flows through the bias windings of core 1 and core 2. This current biases core 1 such that 60ma or more must flow through its input winding to switch core 1. Core 2 is biased such that 90ma or more is required to flow through its input winding to switch its state. When the cores are switched, 2v is developed across their output windings. The DOT end of the output winding is negative at this time. Since each amplifier supplies 30ma of current when impulsed by an information bit, the status of core 1 and core 2 in relation to the number of bits sensed is given in the chart above. Notice that a −P output is available only when two bits are sensed, a valid input.

Circuit Description

To simplify circuit description, only circuits 1 and 3 of the VCK are shown above. The operation shown is for valid information only.

MISSING BITS

No Bits Sensed. Assume that none of the sense amplifiers are impulsed and that no current flows through the input windings. The voltage divider R11 and R9 connected between −6v and ground sets a −5v reference level at pin A. Voltage divider R13 and R15 connected between −6v and −12v sets pin H at a −7v reference level. D32 and D33 perform an OR function and D8 and D17 perform an AND function.

With no current flowing through the input windings, neither core 1 nor core 2 is switched, and no voltage is developed across the output winding. The voltage at point Y is −5v and at point Z, −7v. The output (pin B) from the OR circuit is −5v. This voltage also appears at pin N through the AND circuit, as both legs of the switch are at −5v. Thus, with no information sensed, the output is a +P line indicating an error condition.

One Bit Sensed. The circuit operation is the same if only one bit is sensed. The sense amplifiers provide only 30ma of current through the input windings, which is insufficient to switch the cores. A +P line output is again obtained.

CORRECT OPERATIONS

Two Bits Sensed. When two information bits are sensed at the sense amplifiers, 60ma of current flows through the input windings and is sufficient to switch core 1 only. The two volts developed across the output windings of core 1 is of such polarity as to drop point Y to −7v. Point Z remains at −7v because core 2 was not switched. The OR circuit output is now −7v and appears at pin N through the AND circuit. This −P output level indicates a no-error condition.

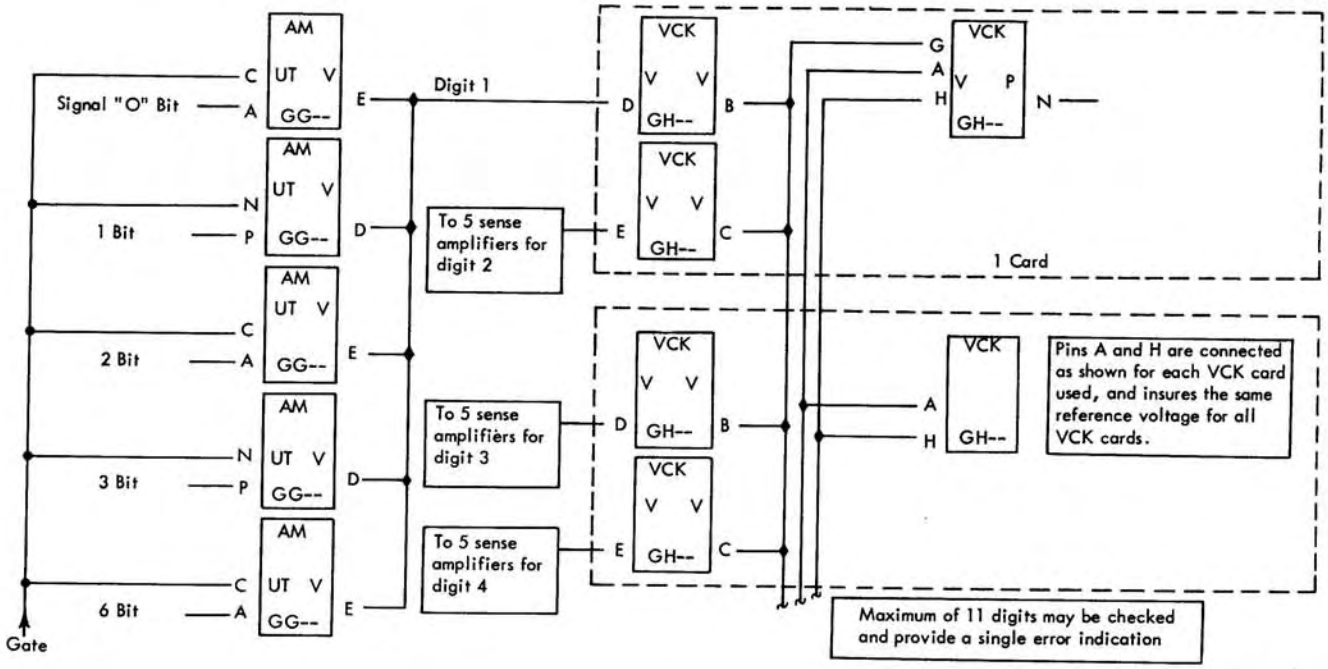
EXTRA BITS

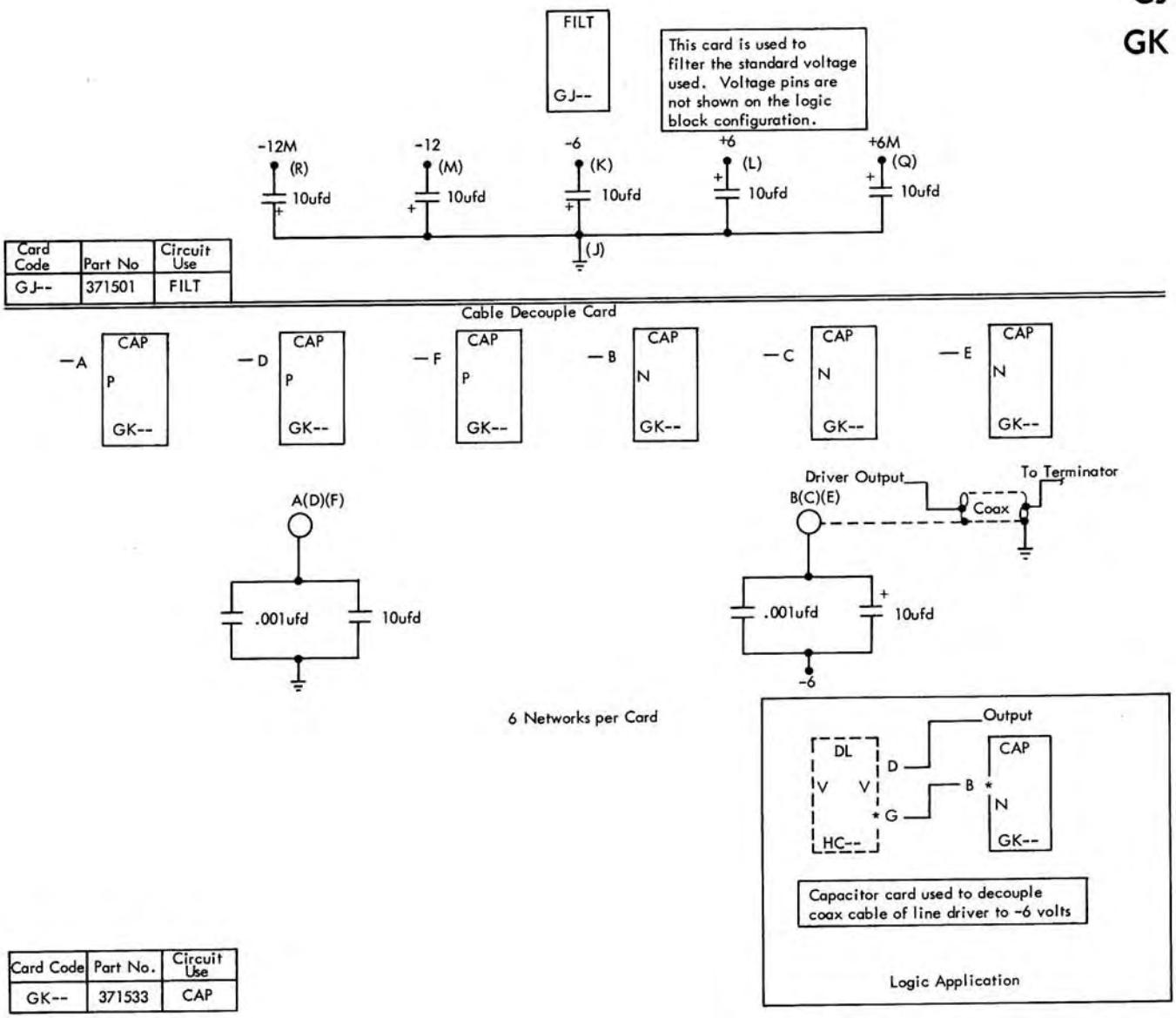
Three, Four, or Five Bits Sensed. When three or more bits are sensed at the sense amplifiers, current flow (90ma to 150ma) through the input windings is sufficient to switch both core 1 and core 2. The polarity of the two volts developed across each output winding sets point Y at −7v and point Z at −5v. The duration of the voltage developed across the output winding of core 2 is longer than that developed across the output winding of core 1. The overlap is required to insure that the voltage at point Z (−5v) inhibits the −7v at point Y which would give a no-error indication. The −5v output from the OR circuit again gives a +P output level at pin N to indicate an error condition. D22 clamps point Y at −7v when core 1 is switched and D20 clamps point Z at −5v when core 2 is switched. L5 is used to damp out transient spikes caused when the cores are switched.

The turn-on delay, measured from the time the input of the sense amplifier crosses the 0v reference level until the VCK output crosses the −6v reference, is about 0.25μs.

Application

VCK cards are used for validity checking on all 2-of-5 bit coded channels such as adder entry, adder output, register, and tape synchronizers. In a parallel validity check application (Figure GH-1), up to 11 validity check circuits are coupled to give a single error indication. The outputs from each validity check sense circuit (pins B and C) are all connected to pin G of one card. Pins A and H of each VCK card used must be coupled to insure that there is no voltage shift in the reference voltages. The error no-error output for all digits checked is at pin N.


AM
UT V
GG--
Signal "O" Bit
1 Bit
2 Bit
3 Bit
6 Bit
Gate
Digit 1
To 5 sense amplifiers for digit 2
To 5 sense amplifiers for digit 3
To 5 sense amplifiers for digit 4
VCK
V V
GH--
VCK
V P
GH--
1 Card
Pins A and H are connected as shown for each VCK card used, and insures the same reference voltage for all VCK cards.
Maximum of 11 digits may be checked and provide a single error indication



Card Code	Part No	Circuit Use
GJ--	371501	FILT

Card Code	Part No.	Circuit Use
GK--	371533	CAP

General Purpose Filter Card

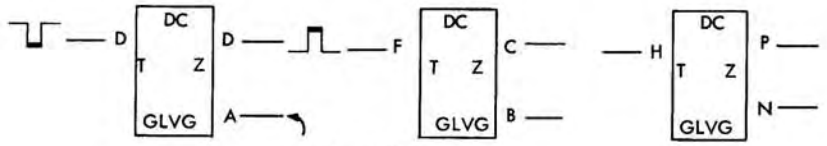
The GJ - - card consists of five 10μfd capacitors used to filter supply voltages to ground potential. The capacitors on the card return directly to the voltage terminals on the SMS card, and eliminate the need for additional back-panel wiring. Signal or voltage pins are not shown on the logic block configuration for this card.

Application

For average filtering conditions, two GJ - - cards are used for each row of cards in the SMS packages. If one filter card is used, optimum filtering is achieved by locating the filter card 75% of the distance along the card row from the voltage entry card.

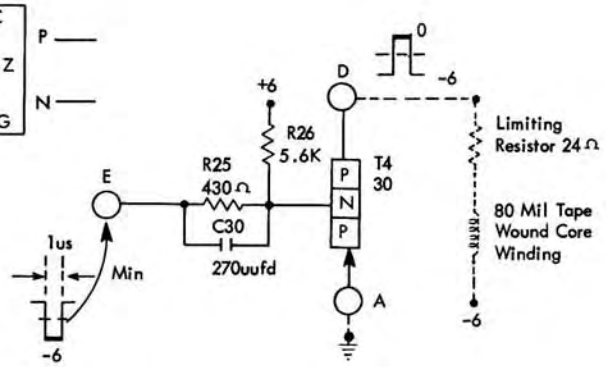
Cable Decouple Card

The GK - - card consists of six capacitor networks used mainly to decouple the neutral wire of a twisted pair or the shield of a coaxial cable. Each capacitor network consists of a 10μfd electrolytic capacitor and a 0.001μfd capacitor bypasses the high frequency portion of the AC signals. Note that three of the networks decouple the AC signal to ground and three networks decouple the AC signal to −6v. A typical logic block application is shown above.



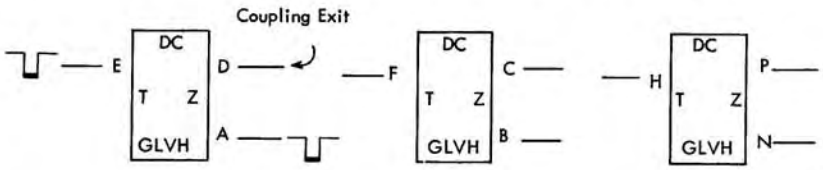
GLVG 371536

Input Levels		Output Levels		Output Current	Delays (usec)		
Min.	Max.	Min.	Max.			Per	Load Shown
Up level depends on I_{co} and I_{cbo}		0.2	-0.6	282 ma Max.	Turn On	Min.	.08
						Max.	.12
-5.5	-6.2	Down level depends on load and I_{co}			Turn Off	Min.	.2
						Max.	.7



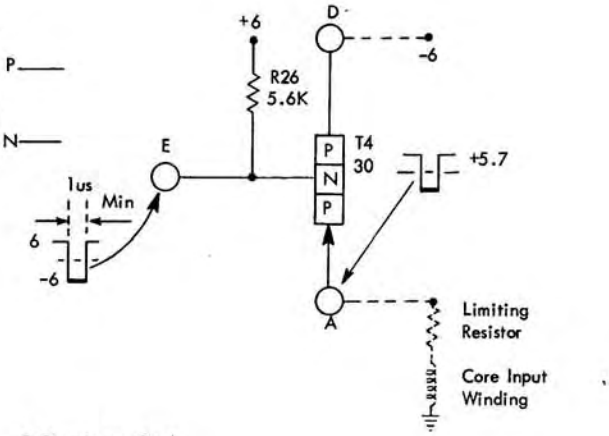
3 Circuits per Card

Emitter Follower Core Driver



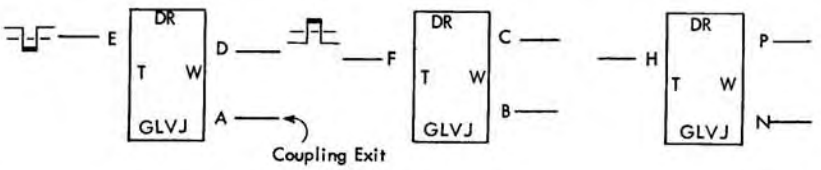
GLVH 371537

Input Levels		Output Levels		Output Current	Delays	(usec)
Min.	Max.	Min.	Max.			
Up level depends on I_{co} and I_{beo}		-4.9	-6.2	465 ma to 600 ma	Turn On	0.1(nom)
					Turn Off	No Appreciable Effect
-5.5	-6.2	Down level depends on load and I_{beo}				



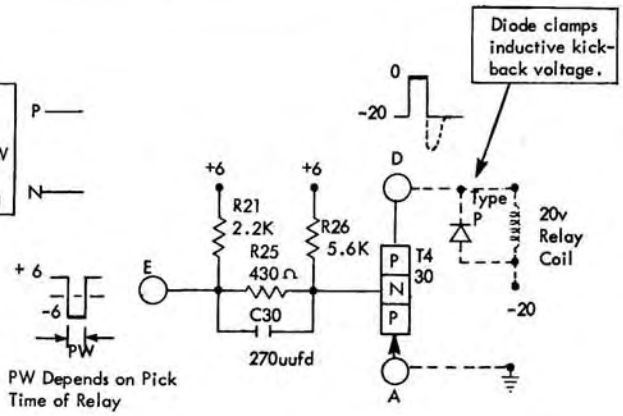
3 Circuit per Card

Relay Driver



GLVJ 371535

Input Levels		Output Levels		Output Current	Delays	(usec)	
Min.	Max.	Min.	Max.			Per	Load Shown
Up level depends on I_{co} and I_{beo}		-0.6	0.2	282 ma	Turn On	Min.	.08
						Max.	.10
-5.5	-6.2	Down level depends on load and I_{co}			Turn Off	Min.	1.0
						Max.	2.7



3 Circuits per Card

Inverter Core Driver

This card consists of three inverter core driver circuits, each capable of supplying 280ma to set magnetic cores. Turn-on of the core driver circuits depends on the voltage to which the transistor emitters are returned. The recommended procedure for coupling is with the emitter tied to ground and the collector load returned to −6v. This arrangement allows a CTDL T line from a loaded collector stage to control the driver.

Circuit Description

In a static condition, Ico flows through the pull-up resistor R26 and sets the base level of T4 to at least +0.54v. If a +T input (+6v) is applied to pin E, T4 remains reverse-biased off and the collector voltage is at −6v. No current flows in the load. When a −T input (−6v) of at least 1 microsecond duration is applied to pin E, T4 is forward-biased on and drops the output voltage to ground potential. Up to 280ma now flows through the core winding and is enough to set the magnetic core. R25 determines the base current supplied by the previous stage and C30 acts as a pulse shaper and improves the rise time of the output signal.

Emitter Follower Core Driver

The GLVH card consists of three emitter follower core driver circuits. Each circuit provides up to 315ma to set magnetic cores. The recommended procedure for coupling is with the collector tied to −6v and an emitter load of 1.3K to 3K returned to ground.

Circuit Description

In the static condition, Ico and Ibeo flows through R26 and sets the base level of T4 to at least 0.54v. With a +T input at pin E, minimum current flows through the emitter follower and the load. When a −T input (−6v) of at least 1 microsecond duration is applied to pin E, up to 315ma flows through the load to set the magnetic core.

Relay Driver

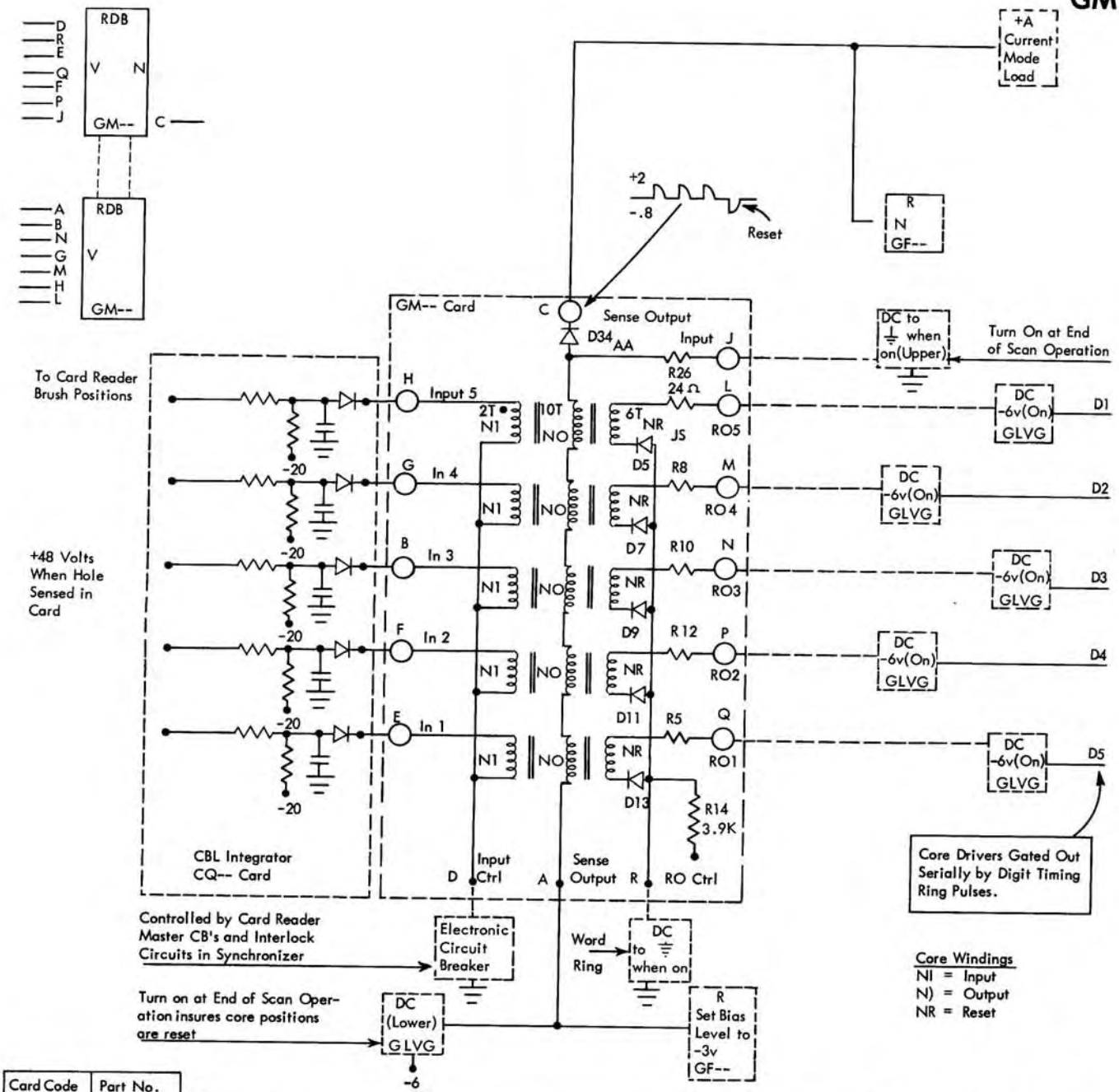
The GLVG card consists of three relay driver circuits that translate a T line input to a W line output. Each circuit is driven from an unloaded CTDL block and provides up to 280ma to a 20v relay or functional coil. This circuit also drives into tape wound cores. Recommended operation is with the emitter connected to ground and the collector load returned to −20v.

Circuit Description (Relay Load)

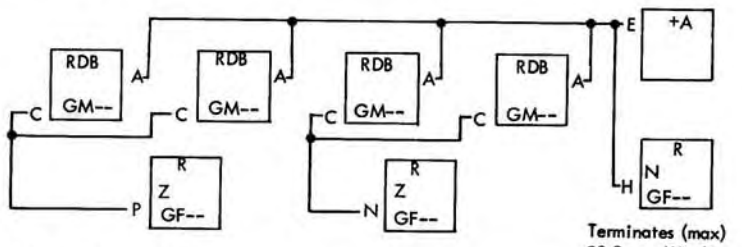
In the quiescent status, Ico current flow through the pull-up resistors R26, R25, and R21 to +6v keeps T3 reverse-biased off. The collector is at −20v and no current flows to the relay. When the input decreases to −6v, T4 is forward-biased on and the output at pin D increases to ground potential. Up to 280ma flows in the output circuit and picks the relay. A +T input turns off the transistor and current flow to the relay ceases. D1 clamps the collector voltage to −20v and prevents the inductive kick-back voltage from damaging the transistor. R21 serves as the collector load for the previous stage. C30 improves the waveshape of the output current pulse.

Pulse Duration

Input pulse duration is a function of the pick time of the relay used. The relay driver is normally fed by a CTDL latch circuit that provides an input pulse of at least 4 milliseconds for picking the relay. Drop out occurs when the latch is reset.

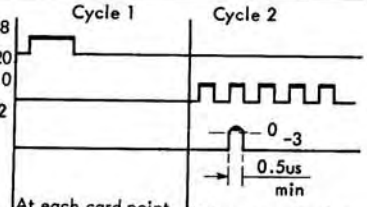


Card Code	Part No.
GM--	371532



Logic application showing associated bias and load card connections to sense windings for card scanning buffer operation.

Terminates (max) 20 Sense Windings



At each card point time, brushes sensing holes in card set cores in parallel.

Between card point times, cores are read out serially by digit timing ring. Cores which were set provide output pulses to current mode block.

Input-Output Core Card 1

The GM - - card consists of five magnetic-tape-wound core positions designed especially for use in the input-output area of a system. Groups of these cards properly connected provide an input scanning core buffer normally used with a card reader. As the card is read, cores wired to brushes sensing holes in the card are set at each card point of the input device. Between these card points, the core positions are read out serially and provide the drive to current mode transistor N blocks. External bias and integrator are required in this application.

Circuit Description

The operation of this card in a typical card scanning core buffer application is shown above. Assume that a card is being read and that all cores have been previously reset.

Set Cores, Cycle 1. All brushes sensing holes in the card at a particular card point time permit sufficient current flow from the gated electronic circuit breaker, through the core input windings and the integrator networks to +48v, to set the core positions. The input integrator networks connected to each input winding prevent back circuits and transient noise signals from affecting the core operation, by isolating the brush and core positions.

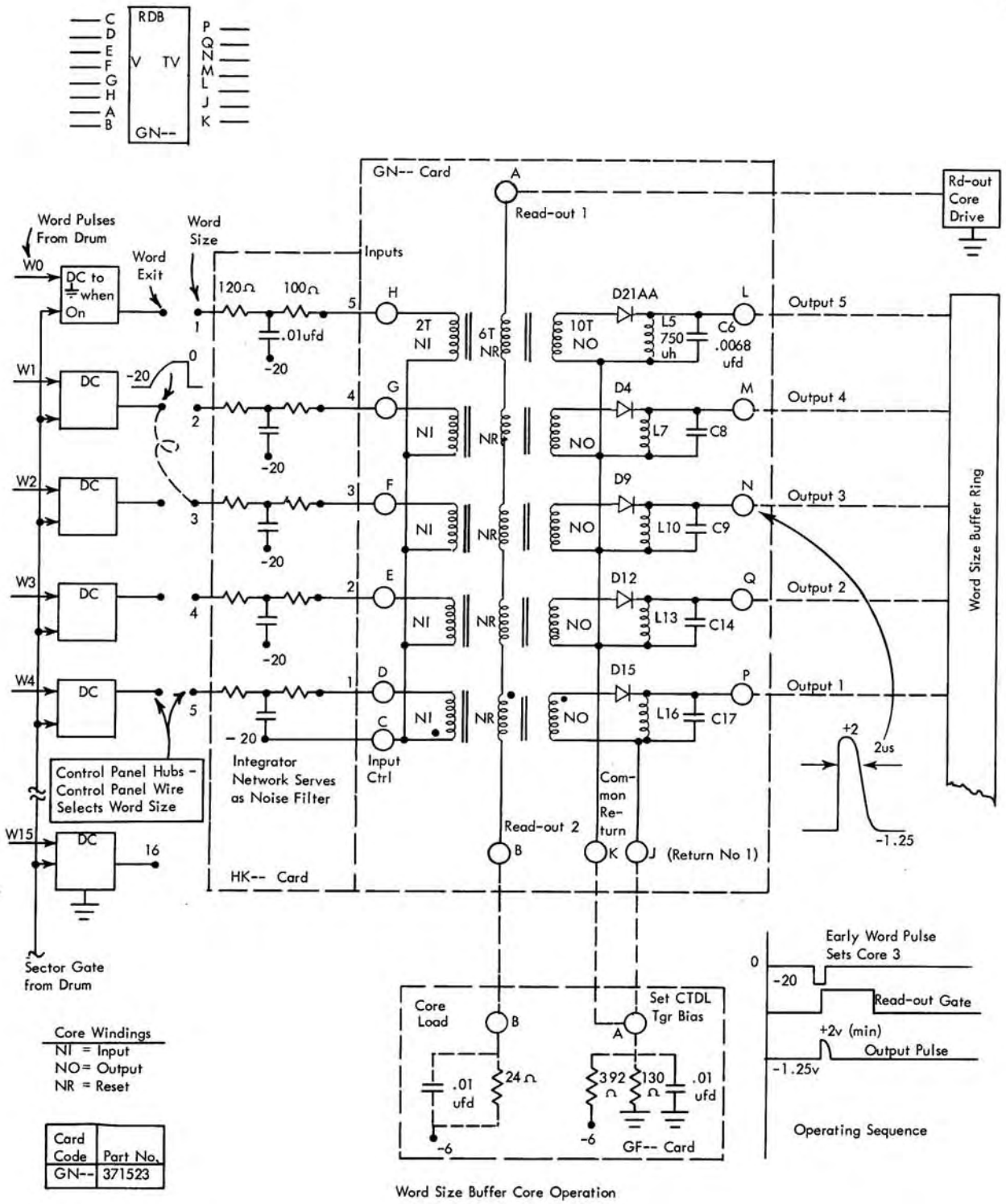
Reset Cores, Cycle 2. Between card reader digit times, core positions are serially reset under control of the core drivers gated on by word and digit rings as shown. When a set core position is read out, a 2v to 5v signal is induced across the output windings which, in conjunction with the load card, provides a +N output to the current mode block.

The sense windings are biased near −3.0v by the external bias card connected to pin A. An LC network returned to the other end of the sense windings (pin C) effectively widens the output pulse seen at the current-mode base and insures that the +N line is up for at least 0.5μs. After all positions are serially read out, the upper and lower read-out core drivers are gated on and place pin J at ground potential and pin A at −6v. The resulting current flow through the sense windings insures that all positions have been reset off and permits safer operation of the validity check circuits.

This sequence of setting cores at each card point time, followed by a serial read-out, continues for the entire card.

Application

Card scanning core buffer configurations of various sizes may be produced from the basic GM - - card and associated bias cards.



Word Size Buffer Core Operation

Word-Size Buffer Core

Five magnetic-tape-wound cores and associated circuitry are packaged on the GN - - card for specific use in the input-output area of a system. Groups of these cards are combined to form word-size buffer core rows that control the ring drive used in the read-in or read-out scan matrixes. Control panel wiring permits the scan matrixes to advance in such a way as to scan in or out only the number of digits desired.

Operation of the magnetic cores is similar to that of the card scanning core buffer card. However, selective read-in to a particular core position is dependant on the control panel wiring. In the punch-out application shown above, a control panel wire from word 2 exit to the word size 3 hub indicates that only three digits are to be punched into the card for word 2. As the drum revolves, each of the word exit hubs is sampled and, if wired, a one-word early impulse sets the corresponding core position. In the example given, core 3 would be set during word 1 time.

At read-out time, all core positions are reset off; however, core 3 is the only position switched. When core 3 is switched, a suitable CTDL output is developed and sets a trigger in the CTDL word-size trigger ring. This word-size trigger ring, in turn, controls the ring drive of the output scan matrix so that only three digits are punched in the card for word 2.

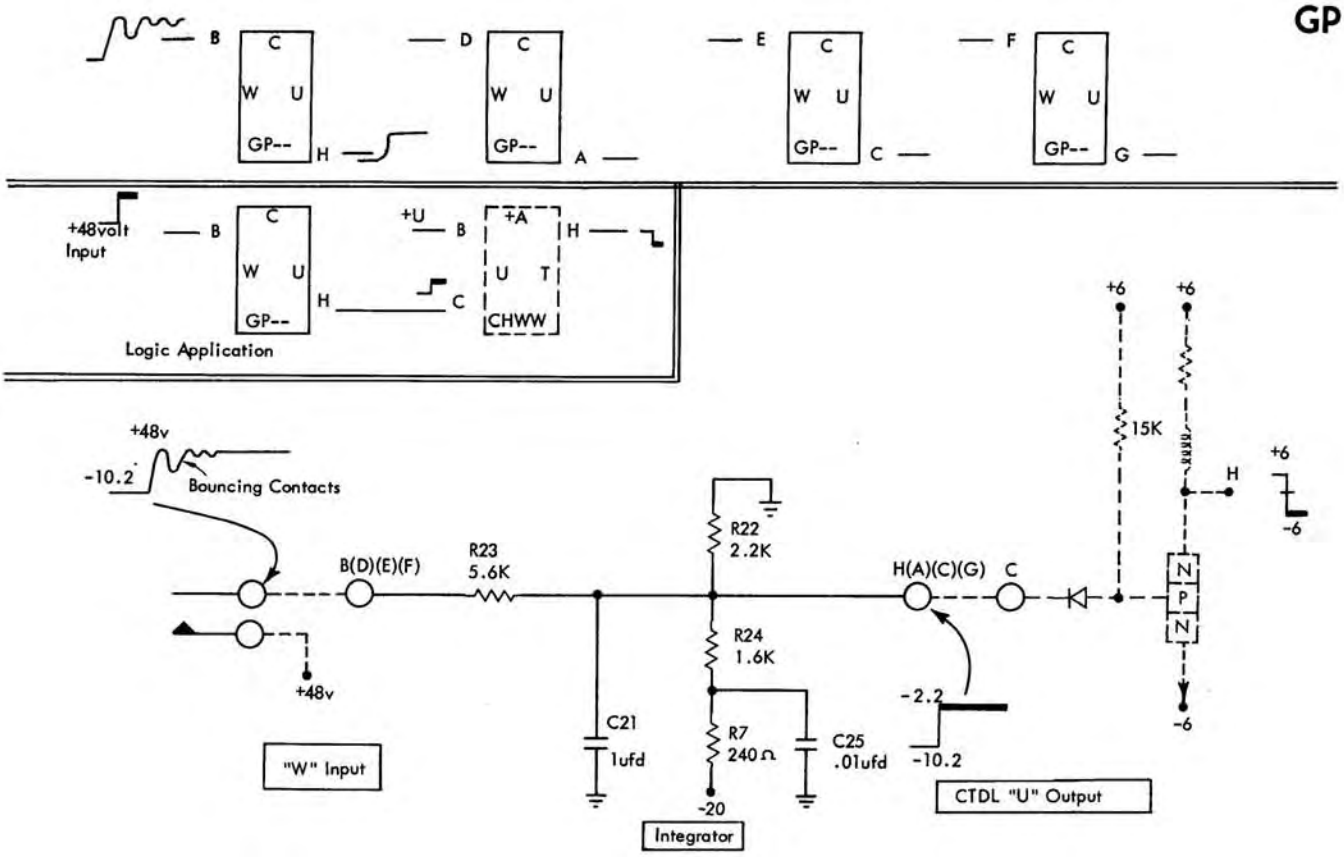
Circuit Description

Assume that the circuit is wired as shown and a punch-out operation is being performed. All core positions are reset off.

At early word 1 time, word 2 exit hub is sampled. Sufficient current (100ma) from −20v through the input windings (N1) of core 3 to the word size hub, control panel wire to ground, sets core 3 on. When the read-out core driver is turned on, current flows from −6v through the six turn reset windings to ground. All cores are reset off. Current that flows through the reset windings and the 24 ohm limiting resistor causes core position 3 to switch off and develop an output of approximately 3 to 5 volts across the output winding (No) of that position. External bias networks connected to pin K and J set the bias level of the output winding to near −1.5v, which permits a suitable CTDL output from the WSB card when a core is switched. The LC network in the output windings effectively increases the pulse width of the signal output coupled to the word size buffer ring and insures the triggering action of the ring.

Application

Similar WSB core rows are used for controlling the ring drive of the input scan matrix. Word-size buffer core configurations of various sizes can be produced from the basic GN - - card.



Four Circuits Per Card

GP-- 371502

Input		Output		Delays (ms)		
Min.	Max.	Min.	Max.		Per	Circuit
43.0	53.0	-5.1	0.7	Turn On	Min.	0.4
0		-7.9	-12.6		Max.	1.5
				Turn Off	Min.	0.5
					Max.	1.8

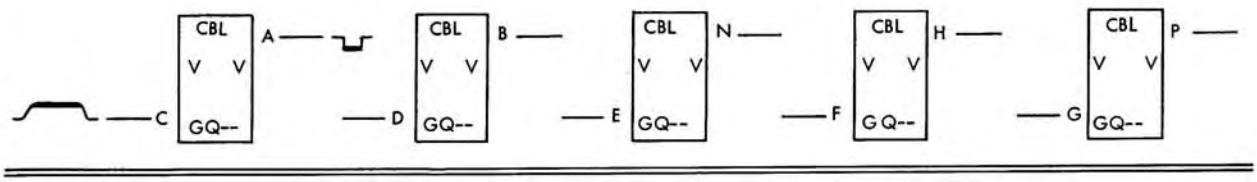
Converter W to U Line

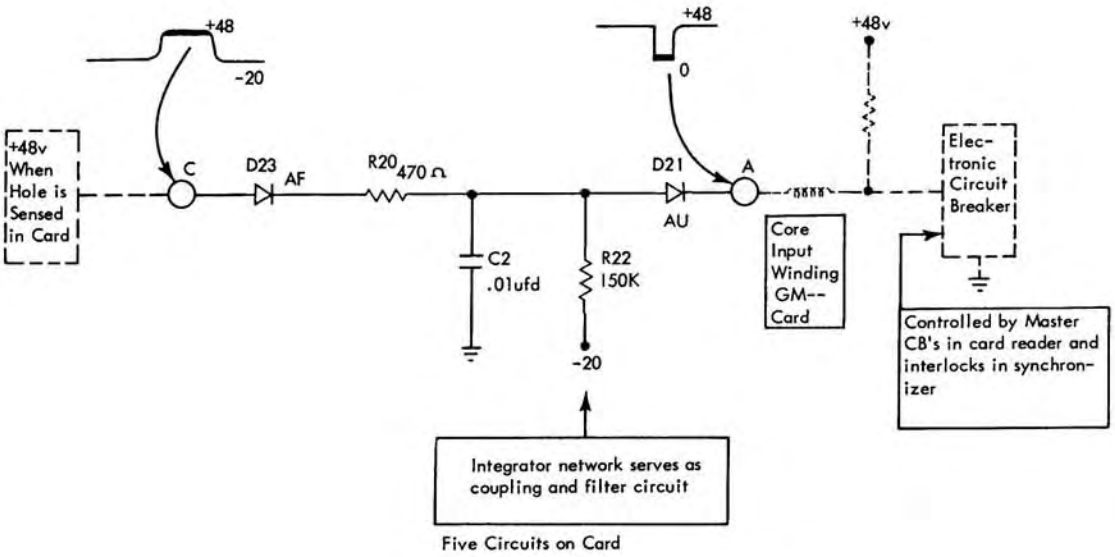
The GP - - card consists of four identical relay to CTDL integrator circuits. Each circuit converts a W line (+48v) input from the normally open contacts of a relay to a CTDL U line output. The U line output normally drives into CTDL P type logic blocks.

Circuit Description

Assume that the integrator circuit is connected as shown above. When the relay is down and the N/O contacts are open, current flow from the −20v supply to ground and to the load (+6v) provides a −U output (−10.2v) from the integrator network. When the relay is energized and the N/O contacts close, +48v is applied to pin B. Current flow through the integrator network increases and gives a +U output at pin H of the integrator. C21 filters the oscillating input caused by the "bouncing" of the contact points when they are first made. C25 filters the noise component injected in the circuit. External loading conditions affect the down output voltage seen at pin H.

The integrator turn-on delays were measured from the time the relay was picked until the output of the integrator crossed the −6v reference. The turn-off delays were measured from the time the relay points opened until the output of the integrator crossed the −6v reference level.





Five Circuits on Card

Card Code	Part No.	Circuit Use
GQ--	371515	CBL

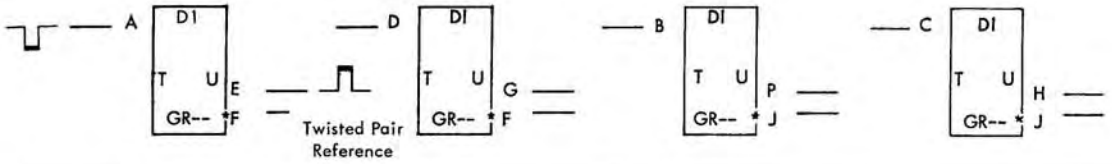
Core Buffer Integrator

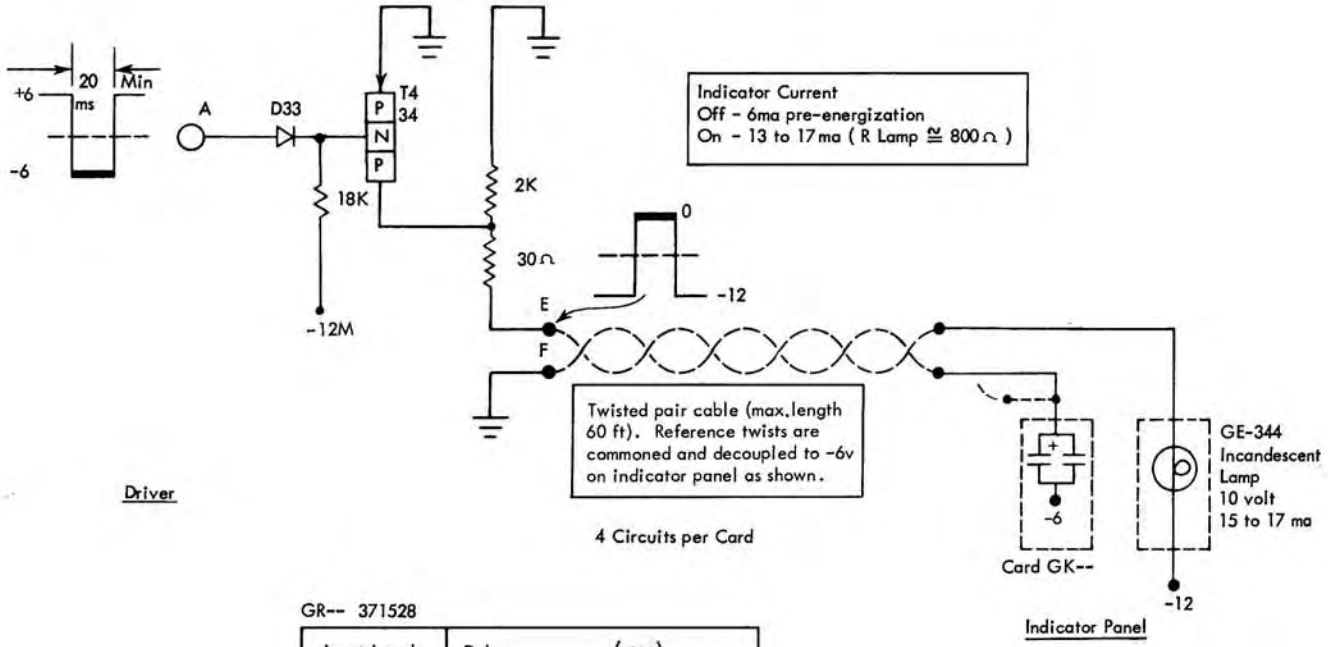
The GQ - - card consists of five special integrator networks designed for use with the card scanning core buffer card (GM - -). Each integrator network serves as a coupling circuit between the card reader brush position and the input winding of a core buffer position.

Circuit Description

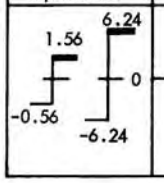
When a hole is sensed in the card and the electronic CB is gated on, sufficient current (100ma) flows through the input winding to set the core position. D23 and D21 act as isolation diodes between the core buffer and the input circuits, and prevent transient noise signals from affecting the core buffer operation. These integrator networks also prevent back circuits between brush positions.

C2 charges to +48v when the brush senses a hole in the card and compensates for possible brush bounce during the time the electronic circuit breaker is made. It also serves as a high-frequency filter for noise transients. R22 and R20, returned to −20v, allow C2 to charge quickly to +48v when the brush first senses a hole in the card.





GR-- 371528



Input Level	Delay (usec)		
		Min.	Max.
	Turn On	.10	.10
	Turn Off	.29	1.30

Low Current Indicator Driver

The low current indicator driver card (GR - -) supplies 15 to 17ma to a 10v incandescent lamp (GE344). A −T input level of 20 milliseconds is required to give a visual indication within the lamp. Four indicator drivers are located on each GR - - card.

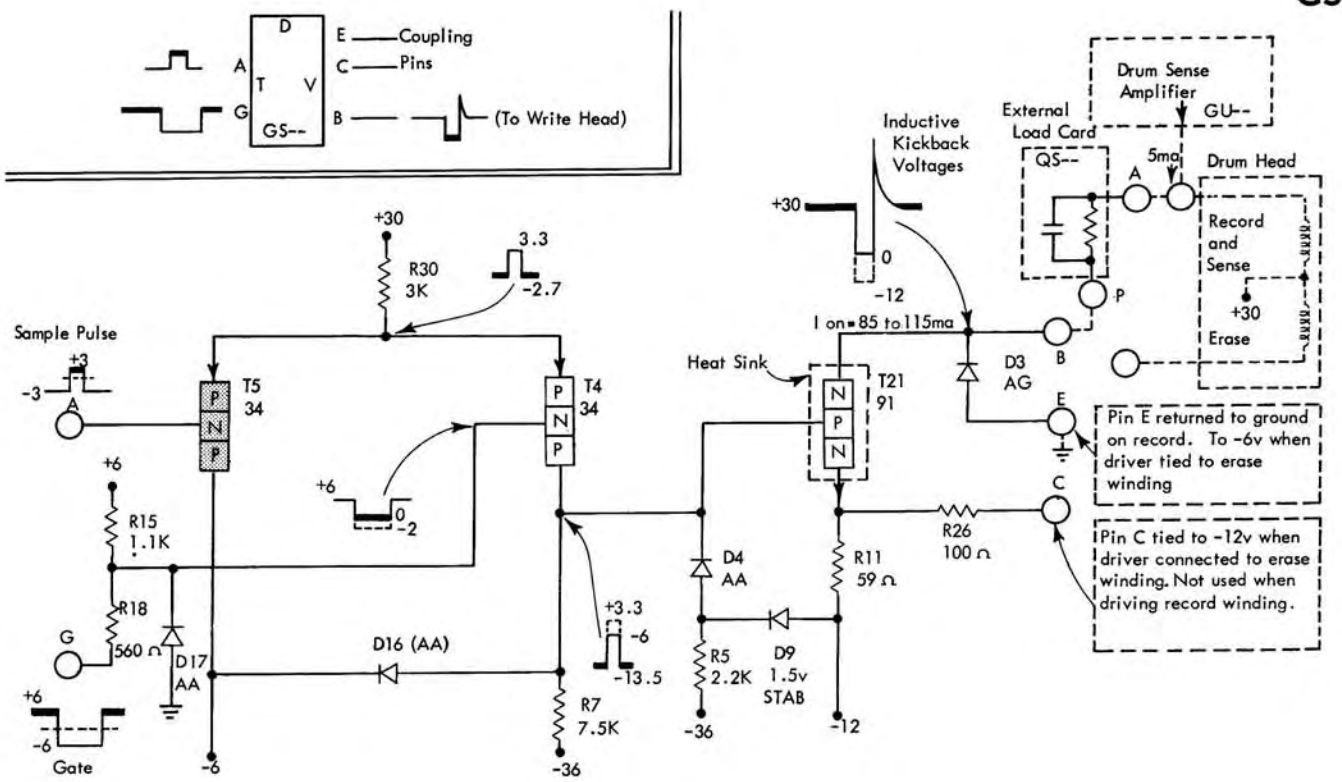
Circuit Description

With a +T input at pin A, T4 is reverse-biased off. A pre-energization current of 6ma flows through the lamp, the 30 ohm and the 2K resistors to ground. This current, however, is not sufficient to give a visual indication in the lamp. The voltage output seen at pin A at this time would be near −12v.

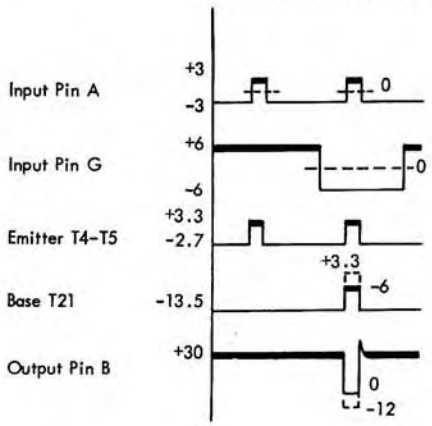
When the input drops to −6v, T4 becomes forward-biased on and appears as a low resistance in parallel with the 2K resistor. The output at pin E increases to 0v and 13 to 17ma flow through the transistor to give a visual indication within the lamp.

Application

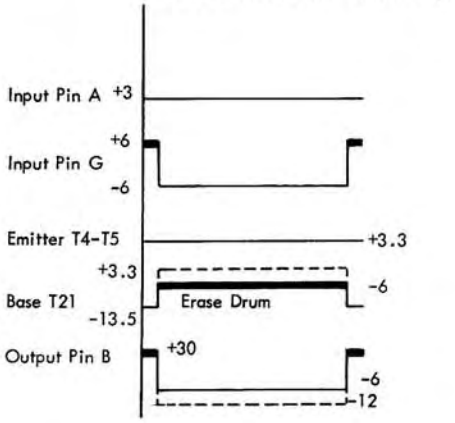
Twisted pair cables are used to connect the driver to the indicator panels. The voltage reference twists are grounded at the driver end and are commoned and decoupled to −6v at the indicator panel as shown above. This circuit is capable of driving an indicator located a maximum of 60 feet from the driver. Five indicator drivers may be driven from one CTDL block.



Driver Connected to Record Winding



Drive Connected to Erase Winding



GS-- 371524

Input Pin A		Input Pin G	
Min.	Max.	Min.	Max.
2.6 to -2.6	+3.9 to -3.9	4.0 to -0.2	6.2 to -6.2

Drum Write Driver

The drum write driver provides the necessary currents to the drum head windings to record or erase information bits on the surface of a magnetic drum. The driver circuit operates at 250kc and consists of an emitter follower, inverter, and a power-diffused transistor capable of supplying 85 to 115ma to the magnetic head windings. There is one driver circuit on each card. A heat sink is provided for the power transistor to help dissipate the heat developed in the device.

Driver Connected to the Record Winding

When the driver is used to record a bit on the drum, a restricted T level input (±3v) is applied to pin A (sample pulse), and a CTDL T level input (±6v) is applied to pin G (gate). Pin E is connected to ground to prevent T3 from operating in saturation and pin C is left floating. A bit is recorded when the sample pulse is up and the gate input is down.

Circuit Description

To Record a Bit. Assume a starting condition when the sample pulse and gate are both down. Emitter follower action of T5 clamps the emitter voltage of T4 to −2.7v. The base voltage of T4, limited by the input divider network and the diode clamp (D17) to ground, is near 0v. T4 is biased off and the base of T21 remains at −13.5v. This base voltage for T21 is established by the divider current through R7, D4 and R5 to D9 and the −12v supply. Stabistor D9 insures at least a −1.5v bias on the power transistor at this time. With T21 off, only the constant 5ma from the sense amplifier flows through the record-sensing winding.

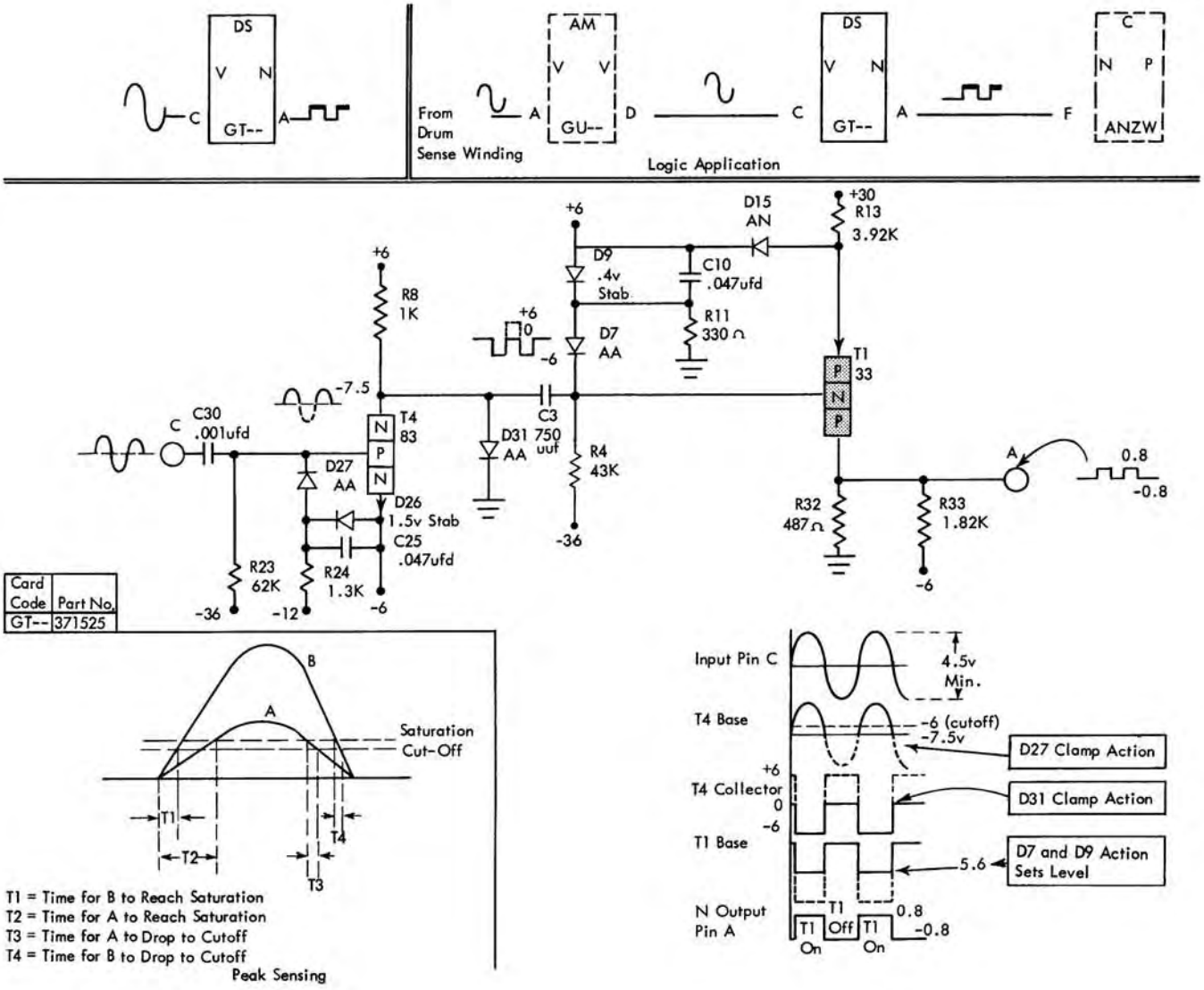
When the sample pulse increases to +3v, less current flows through the emitter follower T5 and sets the common emitter voltage of T4 and T5 to +3.3v. With the gate still down, the base of T4 (0v) is now forward-biased and T4 conducts. The collector of T4 increases toward +3.3v but is clamped by D16 to −6v, which limits the drive to the base of T21.

Increasing the base voltage of T21 to −6v forward-biases the power transistor into heavy conduction (85ma to 115ma). This heavy surge of current through the record winding produces a high density magnetic field that records a spot on the drum. The collector of T21 tries to drop from +30v to −12v but is clamped to ground by D1. D1 prevents T3 from operating in saturation and results in a faster cut-off of the transistor. When the sample pulse drops to −3v, T4 is reverse-biased off, and the base of T21 returns to −13.5v and cuts off the power transistor.

Driver Connected to Erase Winding

Two factors are considered when the driver is used to erase the drum information. First, the erase time is usually much greater than the record time. Second, increased current flow is needed through the erase winding to compensate for the constant 5ma of current flowing in the record-sense winding. This 5ma of current sets up a magnetic field which opposes that set up by the erase winding. Both factors cause an increase in the power dissipation required in T21. To prevent T21 from exceeding its power dissipation limits, pin C is connected to −12v (decreases the value of the emitter limiting resistor) and pin E is connected to −6v. When T3 is turned on, it is driven into saturation and the power dissipation limit is not exceeded.

Circuit operation for this function is similar to that described above for recording a bit. However, instead of a sample pulse feeding pin A, normally a constant +3v source is connected to pin A. The erase time is then controlled by the pulse width of the −T gate input.



Drum Sense Shaper

The drum sense shaper (DS) consists of a two-stage capacity-coupled amplifier operated at 250kc. The sinusoidal signal from a drum sense amplifier is converted to an N line square wave which drives current mode logic blocks.

To insure a reliable square wave output, the sinusoidal input must have a peak-to-peak swing of at least 4.5v.

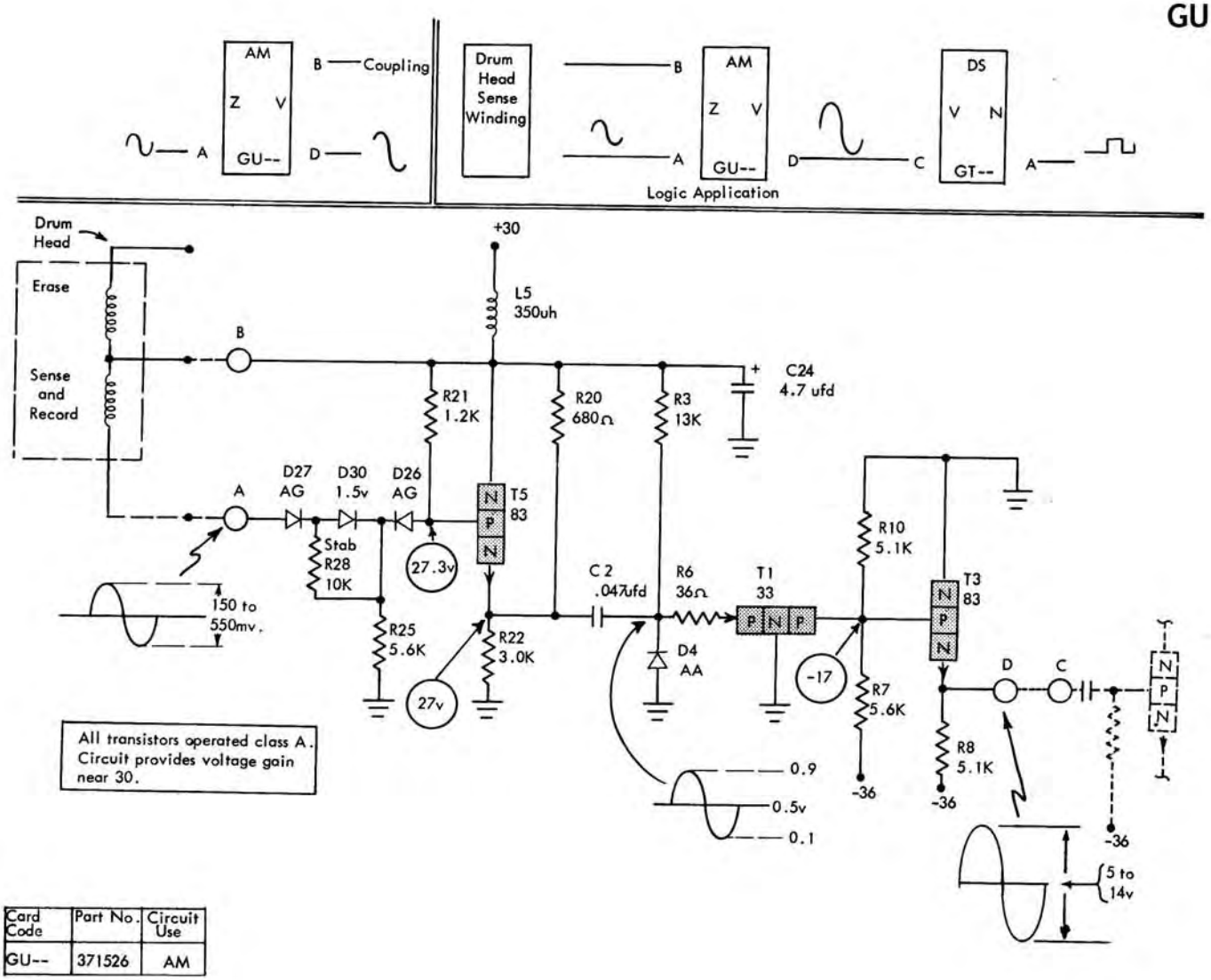
Circuit Description

In the quiescent state, the base level of T4 is set at −7.5v by the input divider networks. T1 is on and has its base level near +5.6v. The output at pin A is +0.8v.

When the input signal is applied to pin C, the negative voltage swing coupled through C30 is clamped to −7.5v by D27 and D26. The use of D26 (1.5v stabistor) keeps the base of T1 1.5v more negative than the emitter, and makes the circuit less sensitive to noise variations. As the signal level increases above −6v, T4 turns on and its collector voltage drops to −6v. This negative swing is coupled through C3 and is clamped at the +5.6v level by D7 and D9 (.4v stabistor). This clamping action prevents T1 from operating in saturation and results in a quicker turn-off time. The output from T1 stays at +0.8v.

When T4 is cut off, its collector voltage increases toward +6v but is clamped at 0v by D31, resulting in a fast rise time of the signal. This sharp positive swing is coupled to the base of T1 and is sufficient to reverse-bias and cut off the 033 transistor. With T1 off, the output drops to −0.8v.

Because of slight variations in the amplitude of the input signals to T4, "peak sensing" is used and the turn-off (instead of turn-on) of T4 is used to control T1 and give more accurate timings of the output. The figure above shows that the time for T4 to reach saturation is dependent on the input signal amplitude, whereas once T4 is driven into saturation, the time required for the transistor to drop from saturation to cut-off is relatively the same regardless of the input signal amplitude.



Card Code	Part No.	Circuit Use
GU--	371526	AM

Drum Sense Amplifier

The drum sense amplifier is used to amplify the sinusoidal signal from the sense winding of a drum head. The GU - - card consists of two emitter followers and a grounded base voltage amplifier, all operated class A. A voltage gain of near 30 from the amplifier provides a sine wave output capable of driving a drum shaper amplifier. Frequency of operation for this circuit is 250kc.

A sine wave input signal having a peak-to-peak swing of 150 to 550 millivolts from the sense winding is coupled to pin A.

Circuit Description

Assume that no signal is read at the sense winding and all transistors are forward-biased on for class A operation. Circled voltage values indicate emitter and base potentials at this time.

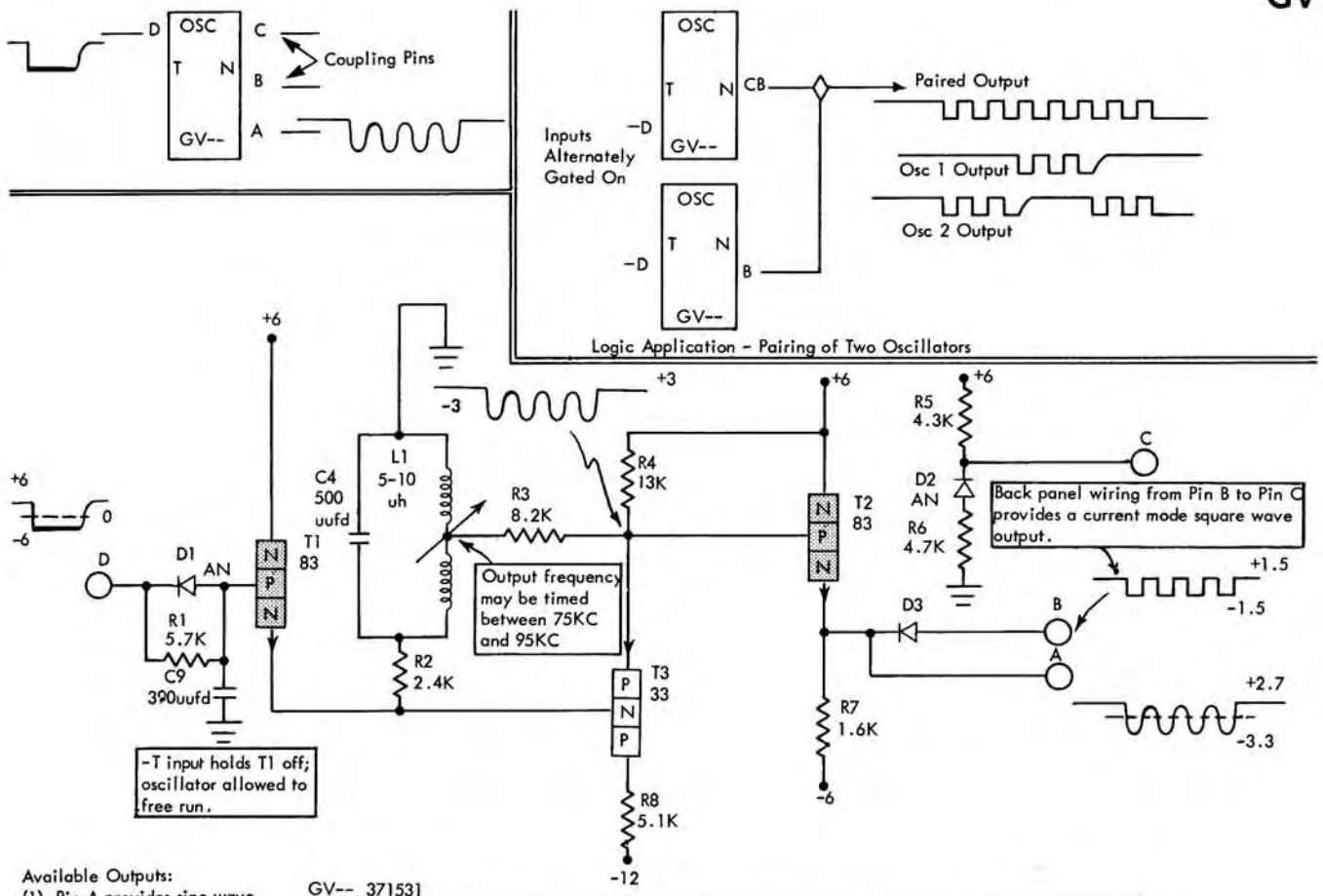
When the sense winding passes a recorded spot on the drum, a sinusoidal voltage is induced in the winding. This voltage varies the bias level of T5, causing the conduction through R22 and T5 to vary accordingly. The emitter of T5 follows the input signal and couples the small changes in voltage through C2 to the emitter of T1. Conduction through the grounded base amplifier and high impedance load provides a voltage gain of near 30 to the base of T3.

The output from the emitter follower T3 is an in-phase sine wave output of 5v to 14v peak-to-peak, which is coupled to the drum shaper amplifier.

Because the sense winding is also used as the record winding, a high inductive kick-back voltage is seen at pin A when writing on the drum. D27 prevents this high voltage from damaging T5. It is also necessary to place R28 in parallel with the 1.5v stabistor (D30), as its back resistance can be as high as 210 megohms. If R28 were not in the circuit the back voltage developed across the stabistor could exceed its specified 12.5v limit and damage the stabistor. L5 and C24 are used as filter networks to ground.

Application

Pin B of the drum sense amplifier is connected to the center tap of the erase and record windings. Pin A is connected to the other end of the record winding as shown.



Available Outputs:
(1) Pin A provides sine wave CTDL output.
(2) Connection of Pin B to Pin C provides a current mode square wave output.
(3) Oscillators may be paired as shown in logic application. More stable operation results in output.

GV-- 371531

Input Levels		Output Levels				Delays		(Usec)
		Current Mode		CTDL			Per	Circuit
Min.	Max.	Min.	Max.	Min.	Max.			
5.8 / -5.8	6.2 / -6.2	1.63 / -1.0	1.9 / -2.0	2.3 / -3.0		Turn On	Min.	.10
							Max.	.20
						Turn Off	Min.	1.9*
							Max.	

* See Circuit Description

Variable Gated Oscillator

The GV - - card contains a variable gated oscillator which provides repetitive output pulses at a frequency of 75kc to 95kc. The circuit consists of a controlled input circuit, a Hartley type oscillator, and a buffer circuit. A special clamping network is provided on the card to permit paired coupling of two oscillator card outputs or to obtain either a CTDL T line or CM N line output. A down T level at pin D allows the oscillator to be free running and gives a sine wave output at pin A. This circuit is used as a read-write control for RAMAC® and operates at 83-1/3kc for this function.

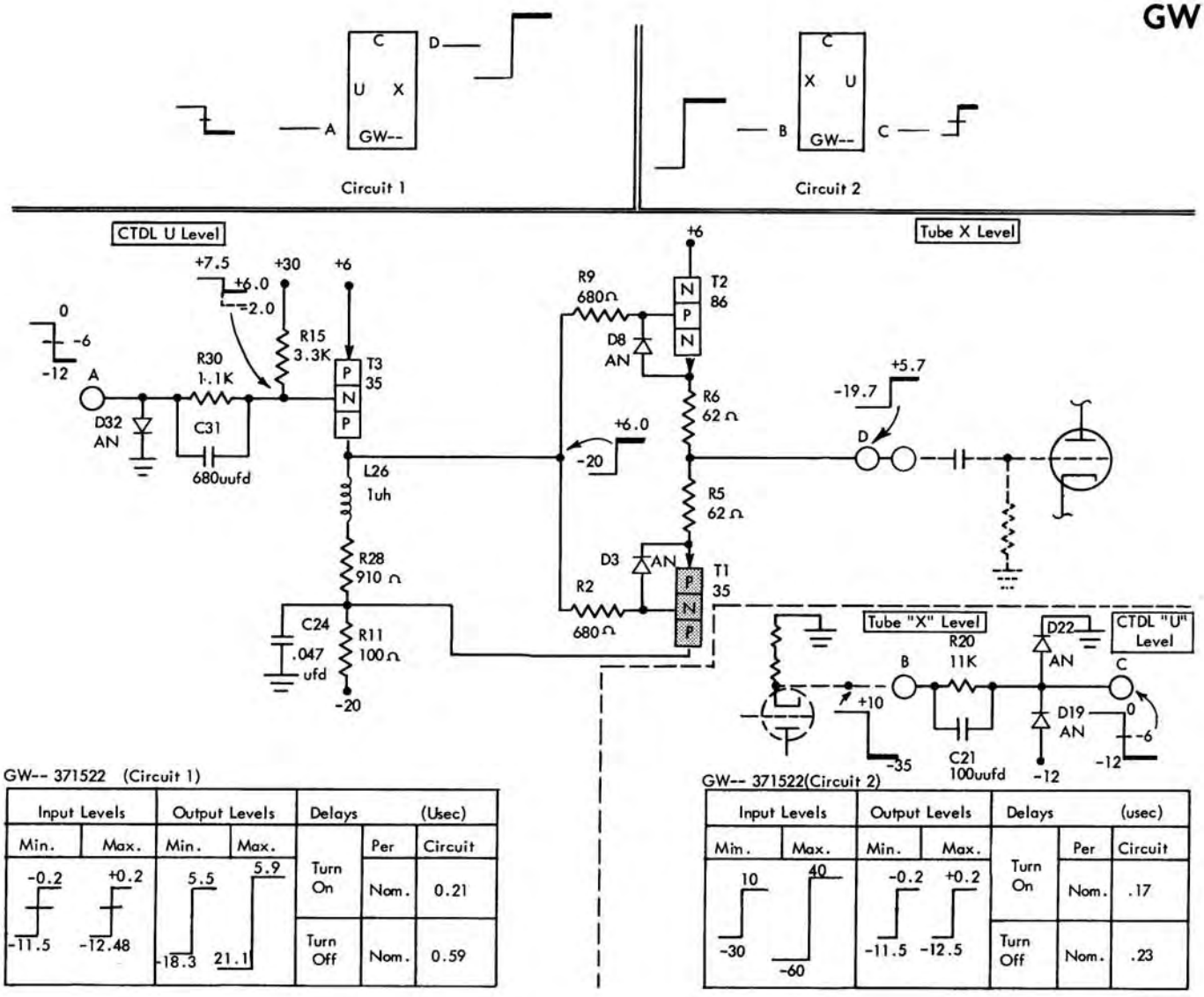
Circuit Description

Input Up. Assume that the input T line is up at pin D. T1 is forward-biased and current flows through L1, R2 and T1. This sets the base level of T3 to +5.7v. The emitter of T3 is set near 3.0v by the divider network of L1, R3 and R4 to +6v. T3 is reverse-biased and the oscillator is off. Pin A output now is about 2.7v.

Input Down. When the input drops to −6v, T1 is reverse-biased and off. The negative swing to −6v causes T3 to be forward-biased on. Electron flow through R8, T3, R3, and the upper part of L1 to ground starts the oscillator action of the tank circuit. Magnetic feedback between the two sections of L1 is sufficient to keep the tank circuit oscillating, which provides regenerative feedback to the base of T3. The sine wave output from the tank circuit is coupled to emitter follower T2 and provides a sine wave output at pin A. Oscillations continue until T3 is cut off by a +T level input at pin D.

The frequency of oscillation is determined by the value of C4 and L1. The input diode D1 provides a quick turn-off of T1 while C9 is used to increase the turn-on time of T1. This increase in turn-on time (1.9μs) is desirable in order to insure overlap between the outputs of a pair of oscillators being alternated and mixed. D3, D2, R5 and R6 provide a special divider network that limits the CTDL output to a current mode N line.

The turn-on delay is measured from the time the input signal crosses the 0v reference until the first negative swing of the output crosses the 0v reference level.



Input Levels		Output Levels		Delays		(Usec)
Min.	Max.	Min.	Max.		Per	Circuit
-0.2	+0.2	5.5	5.9	Turn On	Nom.	0.21
-11.5	-12.48	-18.3	21.1	Turn Off	Nom.	0.59

Input Levels		Output Levels		Delays		(usec)
Min.	Max.	Min.	Max.		Per	Circuit
10	40	-0.2	+0.2	Turn On	Nom.	.17
-30	-60	-11.5	-12.5	Turn Off	Nom.	.23

Converters: (1) U to X Levels; (2) X to U Levels

The GW - - card consists of two separate circuits used for converting between tube and transistor levels. Circuit 1 accepts a U level from a CTDL logic block and provides an out-of-phase X level that is used to drive a vacuum tube circuit. Circuit 2 accepts a vacuum tube X level from a cathode follower and provides a CTDL U in-phase output capable of driving one CTDL logic block.

Circuit Description

CIRCUIT 1.

When the U line is up (0v), the base level of T3 is set near +7.5v by the divider network of D32, R30, and R15 to +30v. T3 is reverse-biased and off. The collector of T3 is near −20v and forward-biases T1 on and reverse-biases T2 off. The output from the complementary emitter followers is near −19.7v at this time. When the input signal drops to −12v, T3 becomes forward-biased and conducts. The collector of T3 goes to +6v and causes T2 to be forward-biased and T1 to become reverse-biased. Conduction through T2 causes the output at pin D to increase to +5.7v.

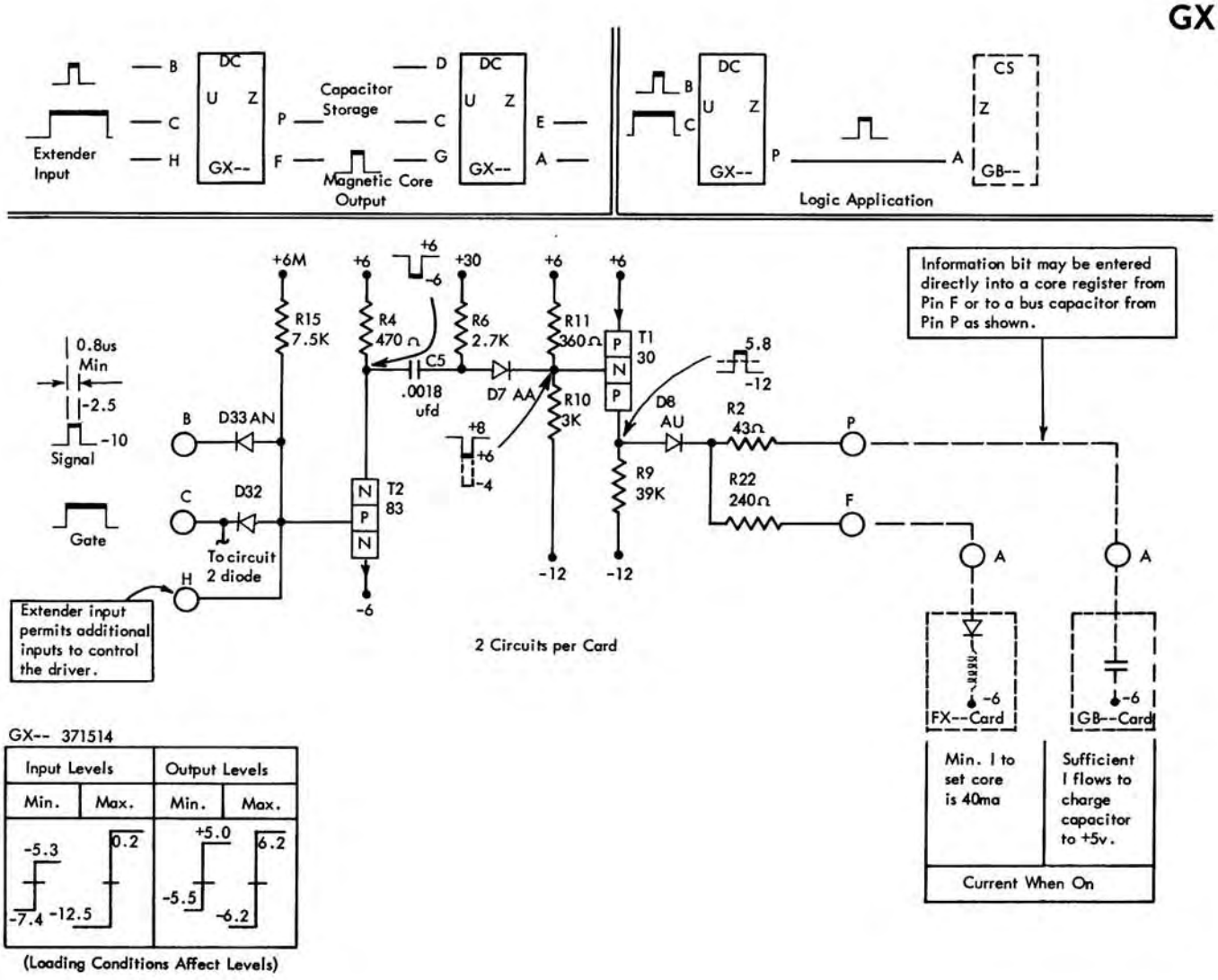
D32 is a protective measure for T3, and provides a path to the +30 volt base supply voltage in case the input driving circuit is removed from pin A. Because of the high switching voltages at the base-emitter junctions of T2 and T1, D8 and D3 are used to protect the transistors by limiting the reverse-bias voltage at the base of these transistors. R2, R9, R5, and R6 limit the current flow through the transistors. The use of the complementary emitter followers gives a sharp rise and fall of the output signal waveform.

CIRCUIT 2.

When the cathode follower output is up, conduction through D22 and R20 clamp the positive output seen at pin C to approximately 0v. Similarly, when the cathode follower output drops to −35v, D19 becomes forward-biased and limits the negative output at pin C to near −12v.

Application

These circuits are found in systems using both CTDL logic and vacuum tube data processing equipment.



GX-- 371514

Input Levels		Output Levels	
Min.	Max.	Min.	Max.
-5.3 to -7.4	0.2 to -12.5	+5.0 to -5.5	6.2 to -6.2

(Loading Conditions Affect Levels)

Magnetic Core Bit Insert Driver

The GX - - card consists of two capacitor or core bit insert drivers. Each circuit provides the necessary current to set a magnetic core shift register directly or charge a bus capacitor storage circuit to the one state. Input arrangement to the circuit is similar to a CTDL logic block, consisting of two diode inputs and an extender pin. A +U signal of at least 0.8μs duration is required at both pins B and C to have the circuit turn on and provide a +Z output pulse of 1.45μs duration at pins P and F. Pin P is used when driving into a capacitor storage load; pin F is used when driving into a magnetic core input winding.

Circuit Description

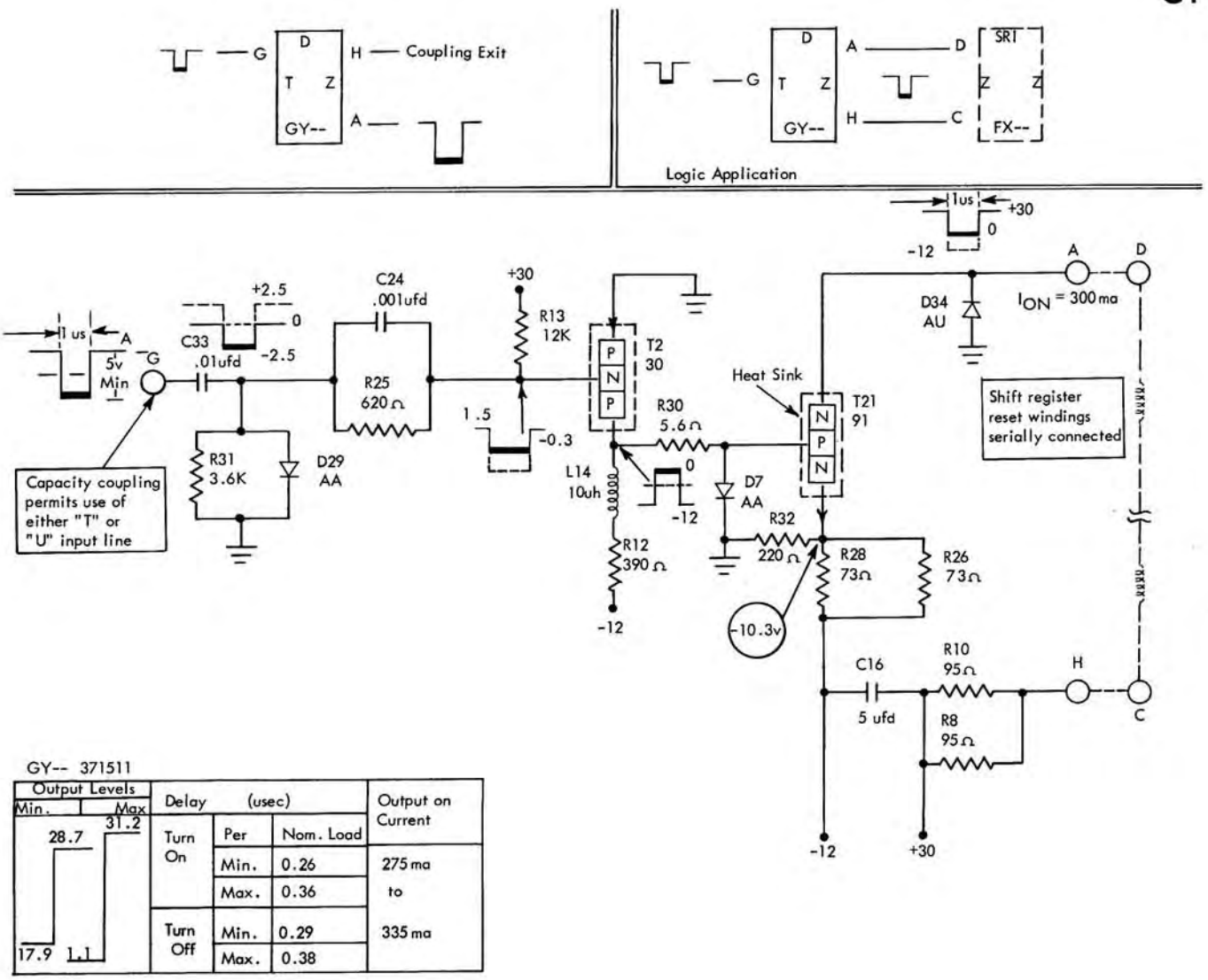
A −U input at pin C (gate) or at pin B (signal) reverse-biases T2 off, and causes the collector voltage of T2 to be at +6v. Divider action of R11, R10, D7 and R6 sets the base of T1 to approximately +8v. T1 is biased off and its collector voltage is near −12v. No output current flows because the isolation diode D8 is reverse-biased.

Coincidence of +U inputs at pins B and C drives T2 into saturation and drops its collector voltage to −6v. The negative pulse (−12v) is coupled through C5 and turns T1 on. The current flow from the load through the forward-biased D8 and T1 to +6v is sufficient to charge a maximum capacitor storage load of 3500$\mu\mu$fd to +5v. If the output at pin F is used, a minimum current flow of approximately 40ma is required through the input winding to set a magnetic core position.

The coupling capacitor C5 also serves as a protective measure for T1 and the register core windings. If the input is "locked on," the negative shift coupled to the base of T1 lasts only for the RC time duration of the input network to T1. After a given period of time, T1 would return to its reverse-biased state and the power dissipation limits would not be exceeded in T1 or the core windings.

Application

In the 7070 system, the bit insert driver is used to enter information bits to a register core at C pulse time or to a bus capacitor at A pulse time.



GY-- 371511

Output Levels		Delay (usec)		Output on Current
Min.	Max			
28.7	31.2	Turn On	Per Nom. Load	
		Min.	0.26	275 ma
		Max.	0.36	to
		Turn Off		
		Min.	0.29	335 ma
		Max.	0.38	
17.9	1.1			

Read-Out Driver

The read-out driver (ROD) is designed to reset or shift out data bits from magnetic core shift registers. A basic inverter circuit drives a power diffused transistor and provides a constant current pulse to the serially connected shift windings of the shift register cards. The voltage level of the core mode output is a variable dependent on the number of cores switched.

Read-out drivers can be driven from either T or U levels because the input signal is AC coupled and does not require a specific voltage reference. The input pulse timing determines the read-out timing of the shift register.

Circuit Description

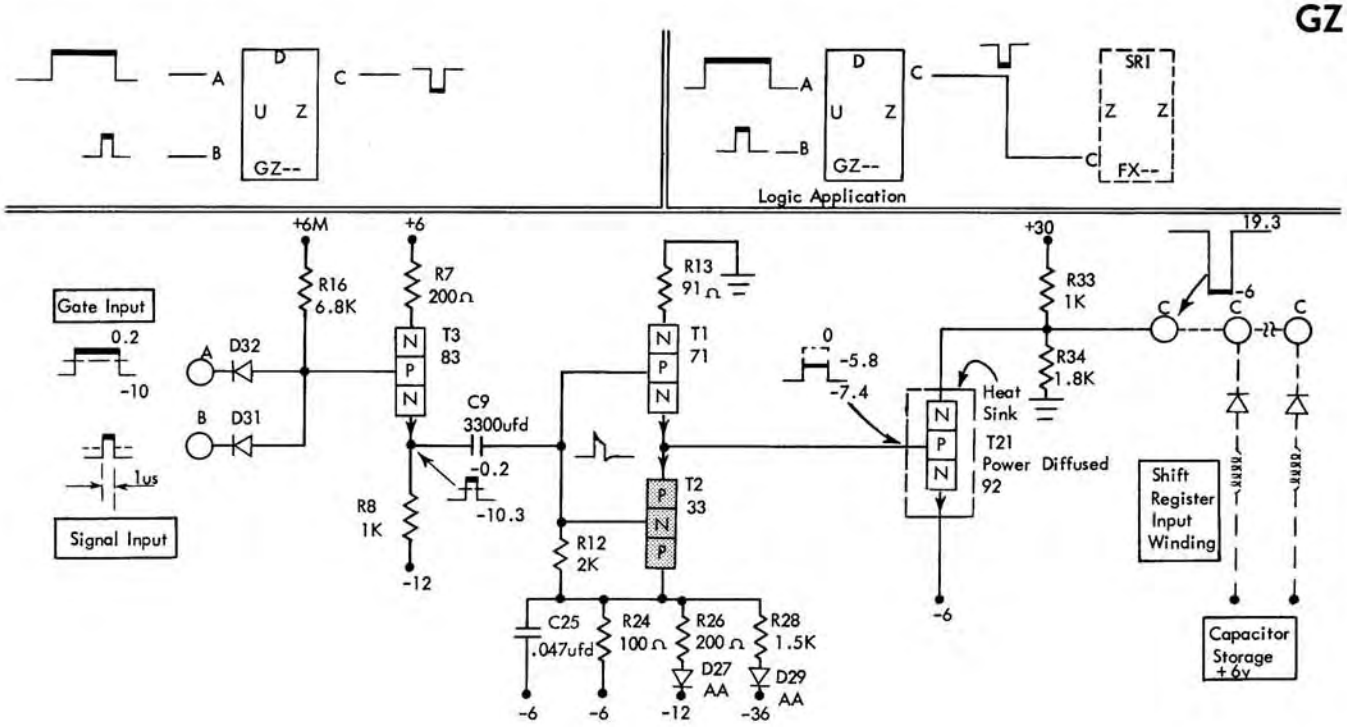
In the quiescent state, the base level of T2 is set at 1.5v by conduction through the input divider network to the +30v supply. T2 is off. With T2 off, T21 is reverse-biased off because its base is near −12v and its emitter is at −10.3v.

A negative input swing of at least 5v is sufficient to forward-bias the base of T2 and drive it into conduction. The collector voltage of T2 increases to ground potential and now forward-biases T21. The power transistor turns on and provides up to 300ma of current to the output circuit, and is capable of resetting up to 15 magnetic cores.

The 95 ohm resistors act as a fuse to protect the read-out windings of the cores if T21 is "locked" on. Because of the high current flow through the power-diffused transistor, T21 is set in a block type heat sink to help dissipate the heat developed. D7 clamps the base level of the power transistor to ground and protects the base-emitter junction of T21 if the −12v supply fails. D34 to ground provides protection for T21. It prevents the collector circuit from floating if the load card is removed, by providing a parallel collector path to ground.

Application

This read-out driver can drive a maximum of 30 shift register core windings, with 15 of the cores being in the ON status.



GZ-- 371510

Input Levels		Output Levels		Delays			Output Current
Min.	Max.	Min.	Max.		Per	Nom. Load	On
-1.0 / -8	0.2 / -12.5	12.2 / -5.2	20.9 / -6.2	Turn On	Min.	.35	715ma to 1250 ma
					Max.	.37	
				Turn Off	Min.	1.27	
					Max.	1.30	

Read-In Driver

The read-in driver supplies the necessary voltage and current outputs to set the magnetic cores of shift registers. Both the gate and signal U line inputs must be up to obtain a special core mode output.

The signal input at pin B is usually fed from a timing ring and has a pulse duration of 1μs. The gate input at pin A is normally on for a full digit time.

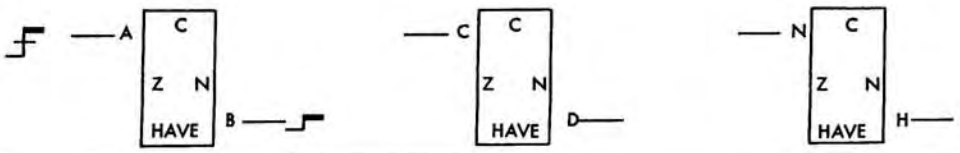
Circuit Description

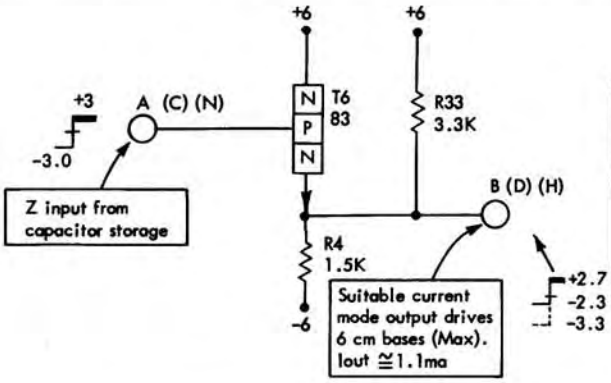
A −U level at either the gate or signal input causes minimum current flow in T3. Emitter follower action of T3 and C9 couple the negative input to the base of the complementary emitter followers. T2 becomes forward-biased on and T1 becomes reverse-biased off. The complementary emitter follower output at this time is near −7.3v and holds T21 off. With the power diffused transistor off, the output at pin C is 19.3v. This positive output prevents read-in to the magnetic core shift register winding, as the load diode is reverse-biased and prevents the flow of current through the windings.

When coincidence of +U levels occurs at pins A and B, T3 becomes more forward-biased and conducts much harder. The positive shift appearing at the emitter of T3 is coupled through C9 to the common base of T1 and T2. T2 is now reverse-biased off and T1 becomes forward-biased on. Complementary emitter follower action quickly increases the base voltage of T21 toward 0v. However, when the positive swing increases to near −5.7v, T21 becomes forward-biased and goes into heavy conduction. The output at pin C decreases to −6v. Read-in to the magnetic core windings can now occur because the load diodes are forward-biased and permit current to flow through the windings to discharge the capacitor storage units.

Application

This read-in driver can supply up to 1250ma to set a maximum of 25 magnetic cores. It can also serve as a "dump-line" to discharge 25 charged bus capacitors.

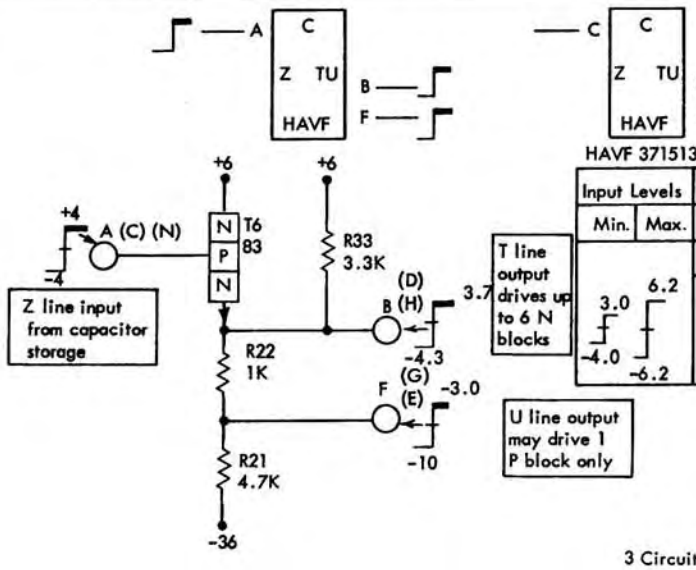




HAVE 371516

Input Levels		Output Level		Delays		(usec)		
Min.	Max.	Min.	Max.		Load	0uufd	33uufd	100uufd
3.0 / -4.0	6.2 / -6.2	0.6 / -0.6	6.2 / -3.0	Turn On	Min.	.04	.08	.14
					Max.	.08	.12	.20
				Turn Off	Min.	.00	.03	.10
					Max.	.03	.06	.12

3 Circuits Per Card



HAVF 371513

Input Levels		Output Levels				Delays		(usec)		
Min.	Max.	Pin B		Pin F			Per	0uufd	33uufd	100uufd
		Min.	Max.	Min.	Max.					
3.0 / -4.0	6.2 / -6.2	2.4 / -4	6.2 / 6.5	-5.2 / -7.4	0.3 / -16	Turn On	Min.	.04	.08	.14
							Max.	.08	.12	.20
						Turn Off	Min.	.00	.03	.10
							Max.	.03	.06	.12

3 Circuits Per Card

Core Mode to Z-to-N Converter

The HAVE card senses the core mode Z level of a capacitor storage circuit and converts it to an in-phase current mode N line output. Three identical circuits are located on each HAVE card.

In the circuit shown above, conduction through the divider network of R4 and R33 sets the emitter voltage of T6 to −2.3v. When the Z input line drops to −3v, T6 is reverse-biased off. The output at pin B remains at −2.3v. A +Z input level forward-biases T6 on. Additional current flow through R4 and T6 clamps the output at pin B to +2.7v. The output at pin B is a usable current mode N level that can drive directly into current mode bases. Loading conditions affect the down level seen at pin B.

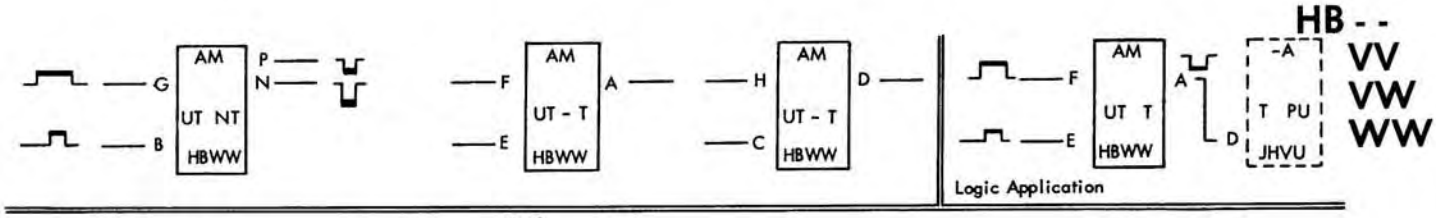
Core Mode to CTDL Converter

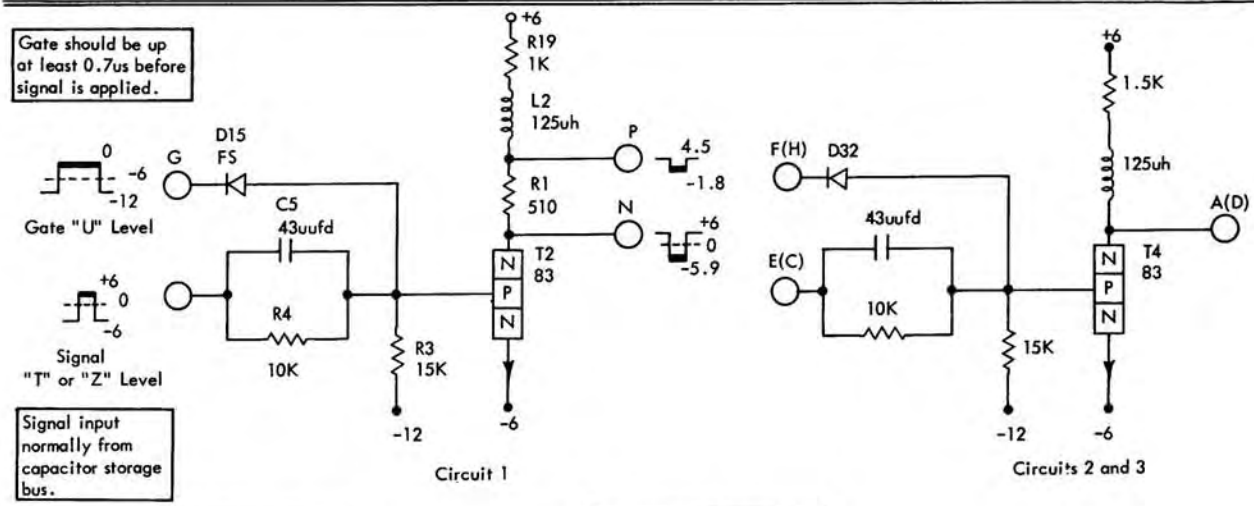
The HAVF card accepts a Z line input from a capacitor storage circuit and translates it to an in-phase T or U line. Three identical circuits are on each card. Output loading conditions affect the output voltage level at pins B and F.

Circuit Description

When a −Z line (−4v) is applied to pin A, emitter follower action sets the voltage at pin B to −4.3v (no load). Increasing the Z line input to +4v causes the emitter follower to conduct more and the output at pin B is +3.7v. The T output is used to drive CTDL N type blocks. The circuit may also be used to drive into CTDL P type blocks by using the U output indicated at pin F.

The circuit delays are the result of transistor turn-on time and the output circuit RC constants.





Input Levels			
Gate In		Signal In	
Min.	Max.	Min.	Max.
2.7 to -4.0	6.2 to -6.2	-5.5 to -7.4	0.2 to -12.5

Output Levels			
Current Mode		CTDL Out	
Min.	Max.	Min.	Max.
2.8 to -1.1	6.2 to -2.5	1.4 to -5.6	+6.2 to -6.2

Card Code	Part No 37----	CM Output Circuit	Collector Loading Circuit 1	2	3	Delays		(usec)
							Per	Block
HBWW	1500	1	Yes	Yes	Yes	Turn On	Min.	0.0
HBVW	1559	1	Yes	Yes	No		Max.	0.07
HBVV	1560	1	Yes	No	No	Turn Off	Min.	0.2
HB--	1561	No	No	No	No		Max.	0.55

Capacitor Sense Amplifier

The capacitor sense amplifier circuits are used to sense the capacitor levels of magnetic core registers or to invert a CTDL T line. Three capacitor sense amplifier circuits are located on each HBWW card. Both the gate input and signal input must be up for the transistor turn-on. The U line gate input is driven by CTDL logic blocks or emitter followers and must be up approximately 0.7μs before the signal input. The gate input controls the base bias level. An out-of-phase T level is obtained from these circuits.

Circuit Operation (Circuit 1)

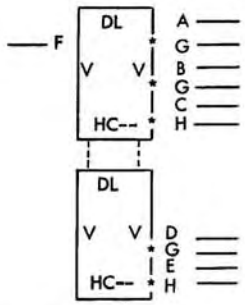
Gate Down, Signal Up or Down. With a −U level at the gate input pin G, the base of T2 is held reverse-biased off regardless of the status of the input signal at pin B. The CTDL output at pin N is at +6v (no load).

Gate Up, Signal Up. When the gate input at pin G increases to 0v, and the signal input at pin B is up (+6v), conduction through D15 and R4, and R3 and R4 forward-biases T2 on. The output voltage at pin N is approximately −6v (minus the small drop across the forward-biased transistor). C5 couples the input signal to the base of T2 and improves the output waveform. The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current mode output.

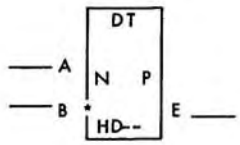
Application

These circuits are normally used to sample the status of the capacitor levels of magnetic core registers.

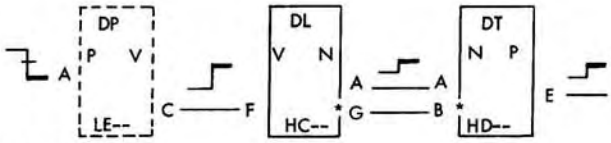
The circuit loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL and current mode outputs are available from these circuits as noted on the schematic.



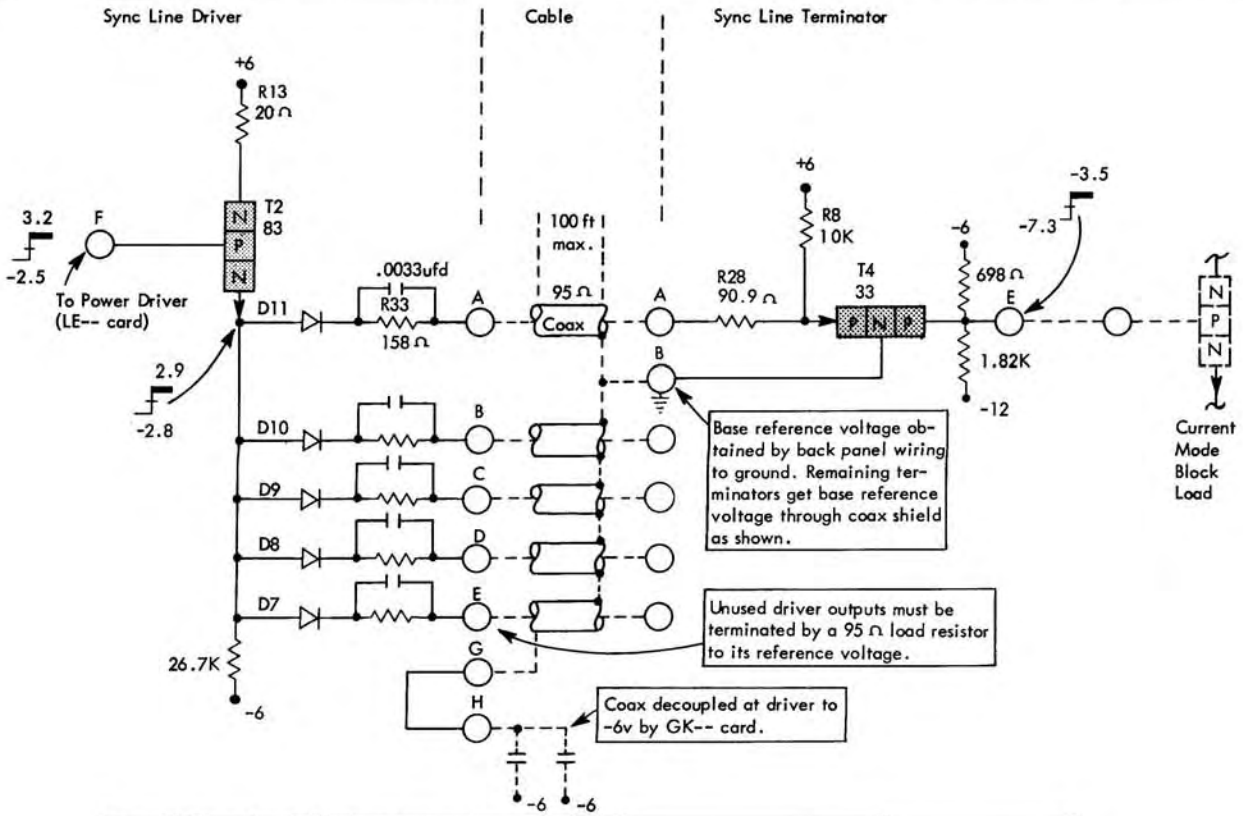
Sync Line Driver Configuration



Sync Line Terminator Configuration



Logic Application



Card Code	Part No.	Circuit Use	Sync Line Driver Input Pin F		Sync Line Terminator Output Pin E		Delays (usec)			
			Min.	Max.	Min.	Max.		Per	Driver, Cable, Terminator	Foot of Coax Cable
HC--	371527	DL	2.7 to 0	+3.5 to 0	-5.0 to -7.0	-1.7 to -7.7	Turn On	Min.	.12	1.73 musec
								Max.	.15	
HD--	371540	DT	-0.5	-3.5			Turn Off	Min.	.03	
								Max.	.04	

Sync Line Driver

This card consists of one sync line driver that can supply current drive and isolation to five sync line terminators. These terminators are remotely located in various modules and are connected to the sync line drivers by coaxial cable. The sync line driver accepts a 500kc special mode signal from a power inverter and provides the proper current and impedance match to the five coaxial cables for efficient transmission of the input signal. Shields of the five coaxial cables are commoned and AC by-passed to −6v by an external 10μfd electrolytic capacitor at the driven end of the coaxial cable. There is no phase inversion between the input signal at the driver and the output signal of the terminator.

Circuit Description

Because the sync line driver always feeds coaxial cables terminated by sync line terminator circuits, both the driver and the terminator circuits are described at this time. Assume a starting condition of T2 on, T4 on and the emitter of T4 at 0.2v. When the special mode input at pin F of the sync line driver is down, emitter follower action clamps the emitter of T2 to −2.8v. D11 is reverse-biased and prevents current flow into the cable from the driver. At this time, approximately 0.58ma flows from the coupling network of the terminator, through T4 and R8 to +6v. The output at pin E of the line terminator is a −P level.

When the special mode input at pin F of the sync line driver increases to +3.2v, emitter follower action clamps the emitter of T2 to near +2.9v. D11 is now forward-biased and additional current flows from the terminator coupling networks, through T4, R28, into the cable, R33, D11, T2 and R13 to +6v. The additional current flow through T4 provides a +P output at pin E of the line terminator.

Application

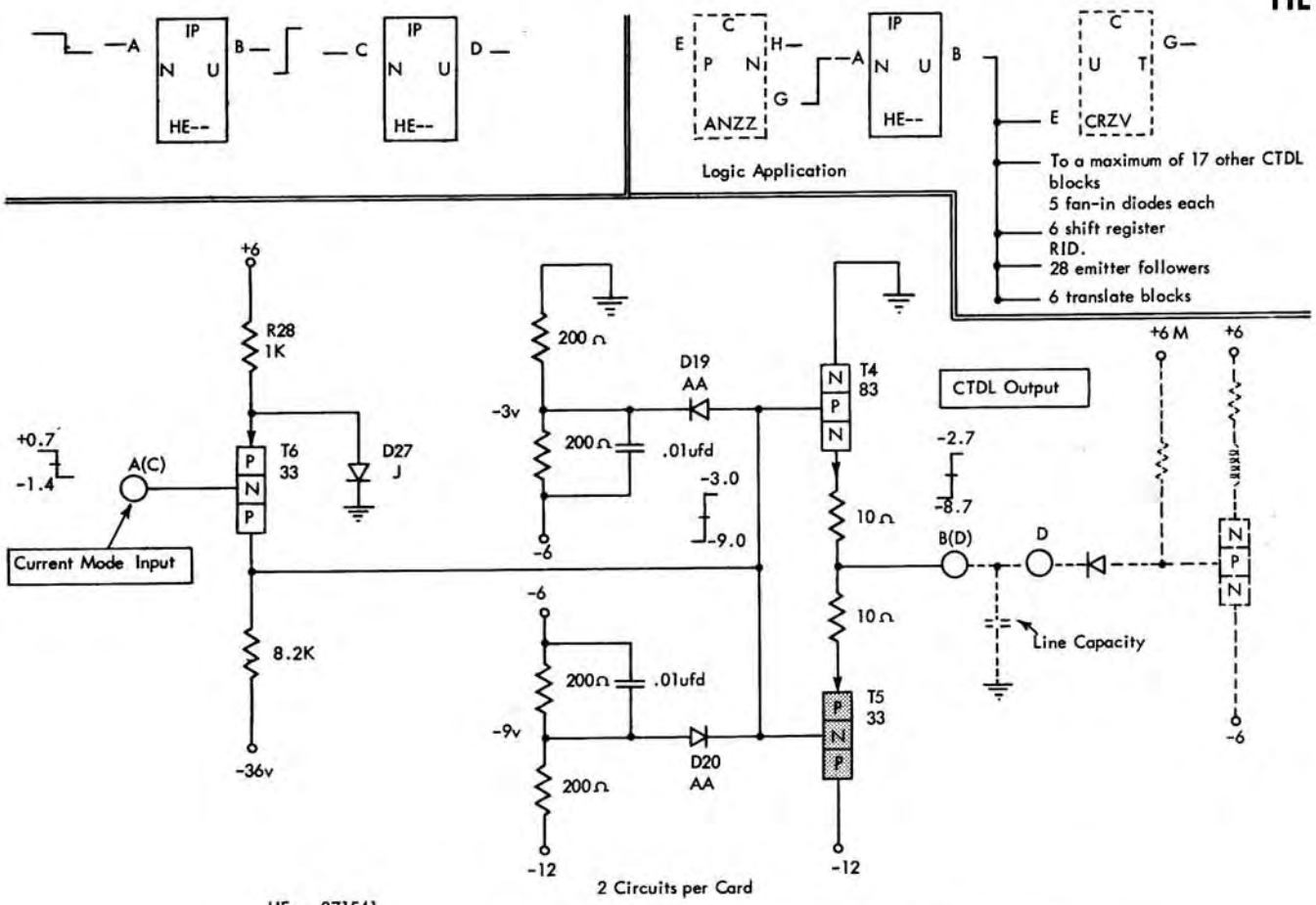
The sync line driver can drive five 100-foot lengths of coaxial cable when properly terminated. If only one coaxial cable and terminator are used, the unused driver outputs must be terminated by a 95 ohm resistance to ground. (Resistors are located on LE - - card.)

Sync Line Terminator

The sync line terminator properly terminates the coaxial cable driven by a sync line driver and translates an N input to an in-phase P output.

The output from the terminator drives current mode P blocks. This circuit function as a class A grounded base amplifier with at least 0.5ma of emitter current flowing at all times. The 90.9 ohm resistor in the input circuit matches the terminator impedance to the characteristic impedance of the cable (95 ohms). Because the base of the transistor is brought out to a signal pin, it is necessary to back-panel wire this point to its proper reference voltage (ground). However, when more than one terminator is driven by the same sync line driver, one and only one terminator base is connected to ground. The remaining four terminators receive their base reference through the coaxial shield.

Circuit operation is described in the sync line driver card description (HC - -). This circuit functions as part of a line-driver, line-terminator pair.



HE-- 371541

Input Level		Output Level		Delays (usec)			
Min.	Max.	Min.	Max.		Load	2 RID	10 CTDL Blocks
+0.4 to -0.4	+1.1 to -2.5	-5.3 to -7.4	-3.6 to -9.6	Turn On	Min.	.13	.18
					Max.	.15	.28
				Turn Off	Min.	.15	.14
					Max.	.26	.23

CM-to-CTDL Power Inverter

The HE- - card consists of two power inverter circuits used for converting a current mode N line input to an out-of-phase CTDL U line output. Each circuit on the card has a basic inverter driving into complementary emitter followers. The input circuit is normally driven by the current mode timing rings, or logic circuits. The power inverter output drives into CTDL U type blocks or into shift register read-in drivers.

Circuit Description

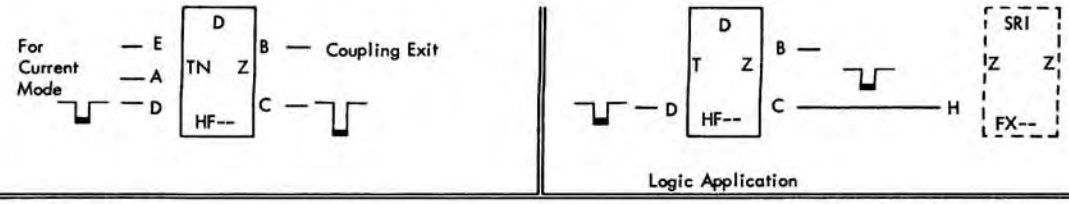
Assume that the power inverter is driving into the CTDL block as shown above. T5 is on; T4 and T6 are off. The emitter of T6 is at 0v. With a +N input at pin A, T6 is held reverse-biased off. Its collector output is set by electron flow from the −36v collector supply to the complementary emitter follower bases, where it is clamped to near −9.0v by D20 to the divider network. T5 continues to conduct, giving an output at pin B of −8.7v.

When a −N input appears at pin A, T6 is forward-biased on. The collector voltage of T6 attempts to go to 0v but is clamped to −3v by D19. T4 becomes forward-biased on and T5 is reverse-biased off. Conduction through T4 quickly charges the line capacity and increases the output at pin B to −2.7v.

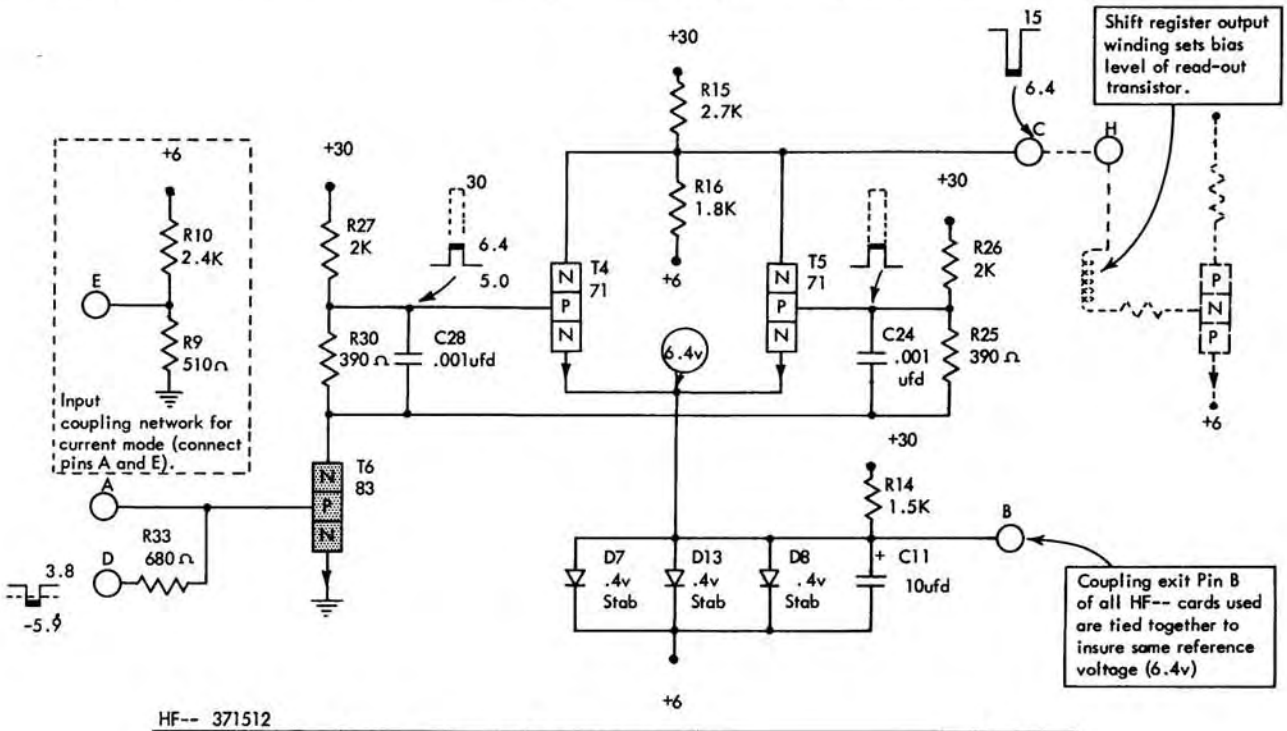
The complementary emitter follower action permits the circuit to charge and discharge large capacitive loads, which results in an output signal with sharp rise and fall characteristics.

Application

Maximum DC loading for this power inverter circuit is noted in the logic application shown above.



Logic Application



HF-- 371512

CM Input Level		CTDL Input Levels		Output Levels		Delays		(usec)	Current Output On
Min.	Max.	Min.	Max.	Min.	Max.		Per	Circuit	
+0.4	6.2	1.4	+6.2	11.7	17.0	Turn On	Min.	0.3	500ma (max)
-0.6	-6.2	-0.5	-6.2	6.1	7.2		Max.	0.7	
						Turn Off	Min.	0.3	
							Max.	0.76	

Read-Out Control Driver

The read-out control driver is used to set the bias level on the read-out transistors of a shift register. When the driver is off, the transistor is reverse-biased to the extent that a core output cannot cause turn-on. When the driver is on, the transistor is only slightly reverse-biased and a core output pulse causes transistor turn-on. Each HF - - card contains one driver circuit and a coupling network. Back-panel wiring of the coupling network allows this driver to be driven by either a CTDL T line or a CM N line. A down input level causes a maximum current flow of 500ma in the output circuit and gives a constant 6.4v output. This drive is sufficient to control an 11 digit, 2-of-5 bit register with sign.

Circuit Description (CTDL T Line Input to Pin D)

With a +T input to pin D, the base of T6 becomes more positive than the emitter and T6 is turned on. Conduction through R30 and R27 to 30v, and through R25 and R26 to +30v sets the base voltage of T4 and T5 to near 5v. The emitters of T4 and T5 are held at +6.4v by R14 and the stabistors between +6v and +30v. There is a constant 0.4v drop across the stabistors. At this time T4 and T5 are reverse-biased and off. There is no current in the output circuit and the output voltage at pin C is near +15v set by divider network of R16 and R15.

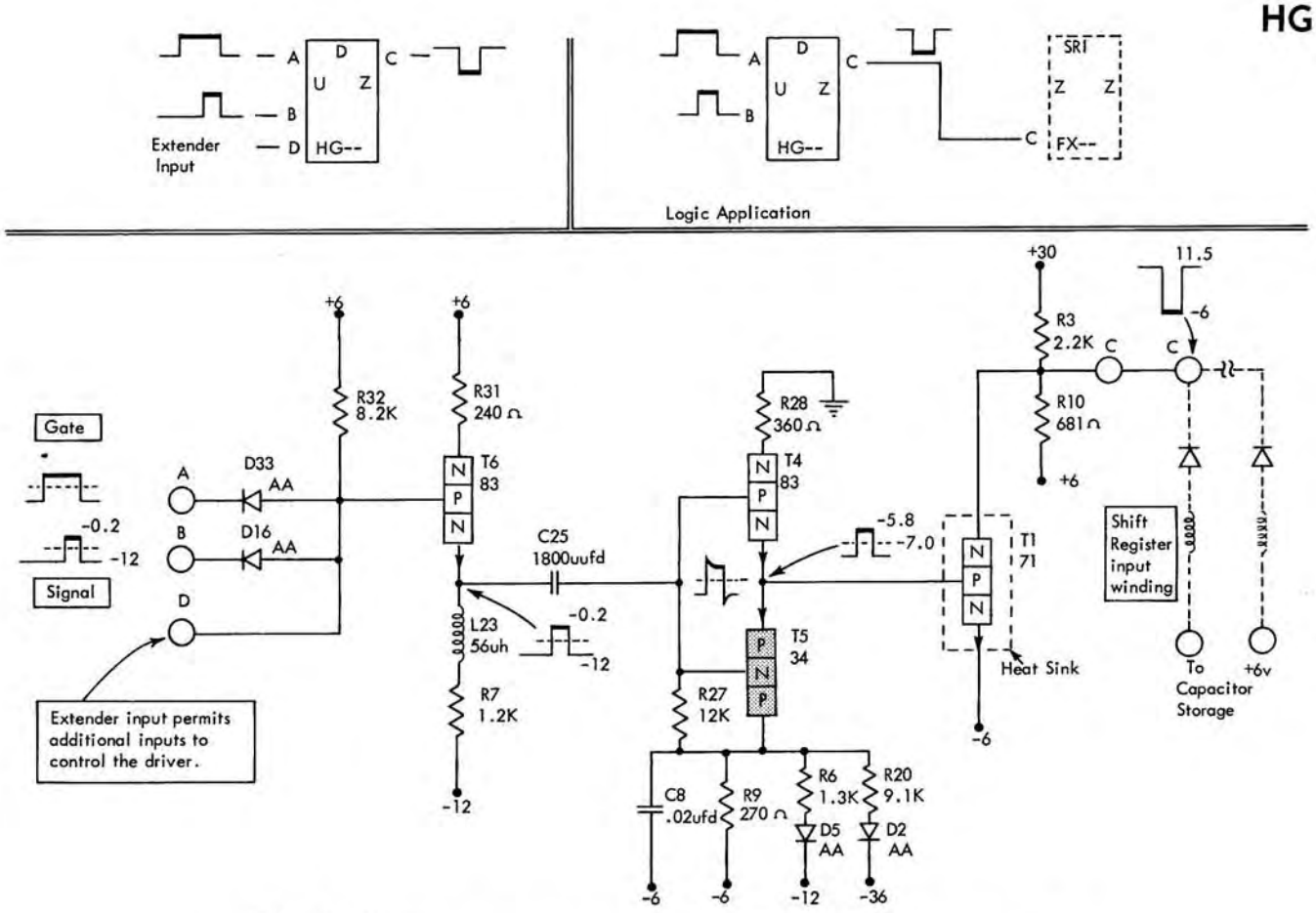
When the signal input is down, T6 is reverse-biased and off. The base voltages of T4 and T5 increase above the 6.4 emitter voltage and drives both transistors into heavy conduction. Each 071 transistor is capable of supplying 250ma to the output load.

The output voltage at pin C is at 6.4v and sets the bias level of the shift register read-out transistor so a core output can cause turn-on.

The 0.001μfd capacitors, and the 390 ohm, 2K resistor network equalize the loading of T4 and T5 to compensate for differences in characteristics of the 071 transistors.

Application

The read-out control driver is used for all types of shift registers. In normal operation, this driver should feed the register near its mid-point. If a current mode N signal is to drive into this circuit, extender pin A is back-panel wired to pin E and provides correct coupling. Pin B of all read-out control drivers used in a register operation are coupled together and insure the same reference voltage (6.4v) for all drivers.



HG-- 371517

Input Levels		Output Levels		Delays			Output on Current
Min.	Max.	Min.	Max.		Per	Circuit	
-1.0	0.2	10.8	11.9	Turn On	Min.	.158	72ma
-8.0	-12.5	-5.7	-5.9		Max.	.200	to
				Turn Off	Min.	.478	438ma
					Max.	.538	

(usec)

Digit Read-In Driver

The digit read-in driver is used to set the magnetic cores of a single digit register. Both the signal and gate U line inputs must be up to give a special core mode output capable of supplying 430ma. This current can set up to 5 magnetic cores of a single digit register.

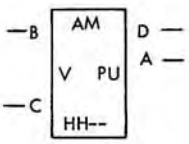
The signal input is normally fed from a timing ring and has a pulse duration of 1 microsecond. The gate input is on for a full digit time. Extender pin D provides for additional inputs to control the circuit.

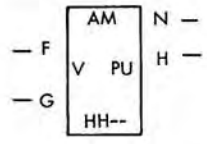
Circuit Description

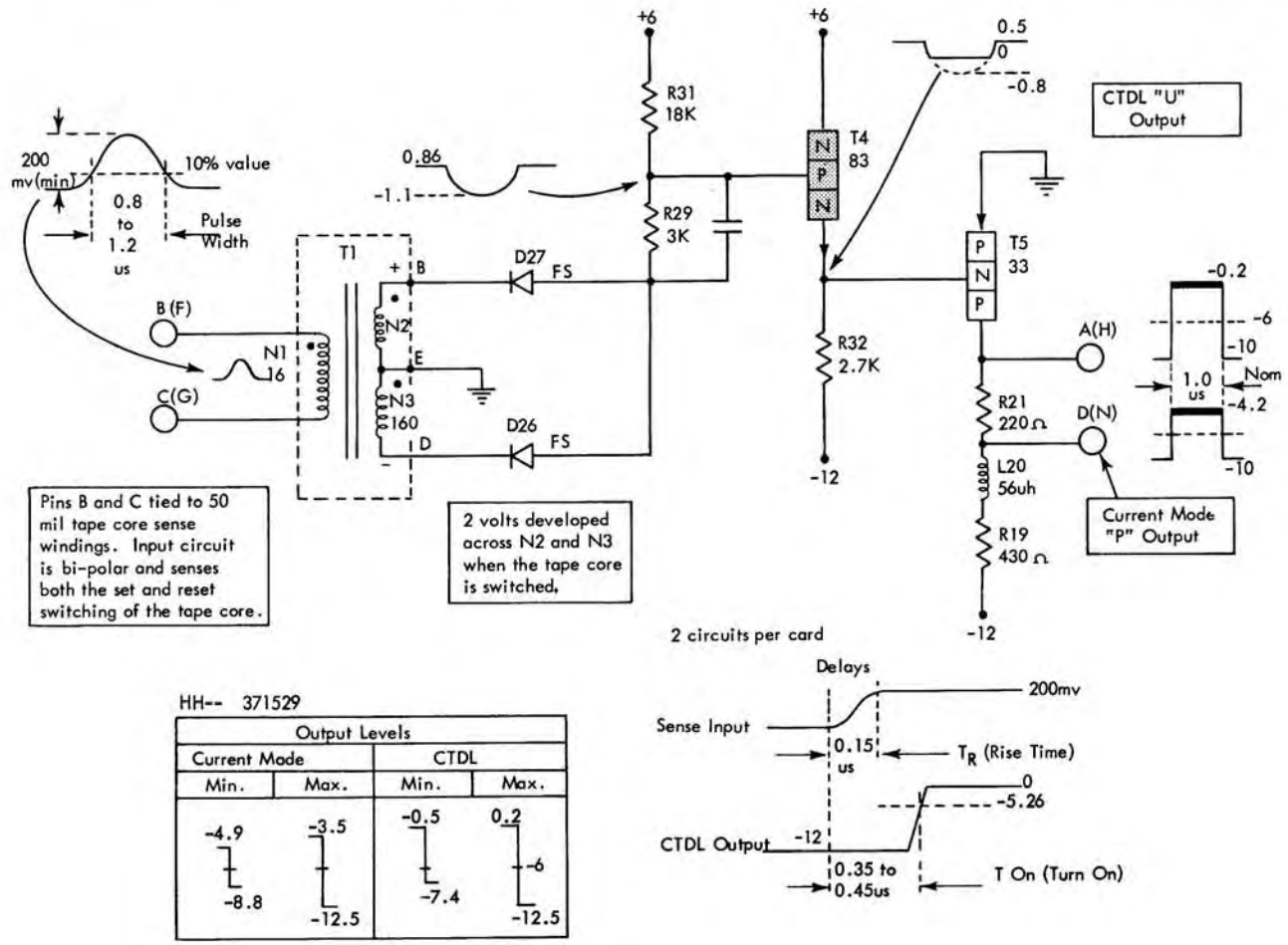
If either the U line gate or signal input are down, the base voltage of T6 is near −12v. Conduction is at a minimum through T6 and a −12v swing is coupled by C25 to the base of T4 and T5. This negative shift forward-biases T5 on and reverse-biases T4 off. The output from the complementary emitter followers reverse-biases T1 off. The collector voltage of T1 is set by the divider network of R10 and R3 and the output seen at pin C is +11.5v. The diodes in the shift register input windings are reverse-biased and prevent current flow through the core input windings, even if the capacitors are charged.

When both the gate and signal are up, T6 becomes more forward-biased. Conduction through T6 increases and the positive voltage shift at the emitter is coupled through C25 to forward bias T4 on and T5 off. The output of the complementary emitter follower attempts to go to 0v but is clamped near −5.8v when T1 is forward-biased on. The collector voltage of T1 decreases to −6v and, if the capacitor storage networks are charged to +6v, conduction through the forward-biased diodes and core input windings quickly discharges the capacitors and sets the core positions on.

The complementary emitter followers provide sharp control of the turn on and turn off of T1.







HH-- 371529

Output Levels			
Current Mode		CTDL	
Min.	Max.	Min.	Max.
-4.9 to -8.8	-3.5 to -12.5	-0.5 to -7.4	0.2 to -6 to -12.5

Tape-Core Sense Amplifier

The HH - - card consists of two tape-core sense amplifier circuits. Each circuit senses and amplifies the special mode switching output pulse of a 50 mil tape core and provides both a CTDL and a current mode output. The input circuit is tied to a core output winding and senses both the set and reset switching of the core. The output of each amplifier circuit is identical to a CTDL logic block and may drive simultaneously into both a CTDL U line and a current mode P line. A plus output is obtained on both the set and reset switching of the core.

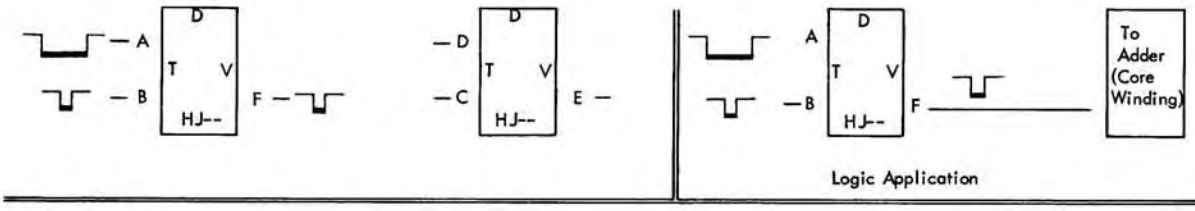
Circuit Description

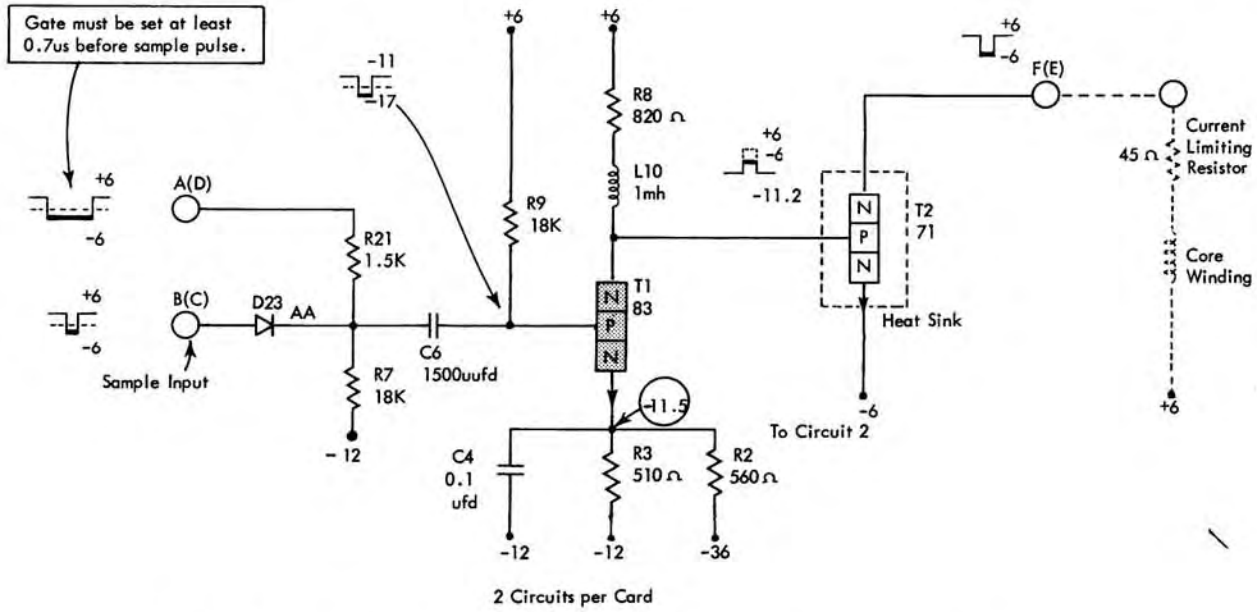
With no signal at the input pins B and C, conduction from ground through N2, D27 and from N3 and D26 to R29, R31 to +6v sets the base of the emitter follower of T4 to 0.86v. The emitter follower output reverse-biases T5 off, giving a CTDL output at pin A of 12v.

Assume the tape core is switched on (set), and the 200 millivolt input signal appears between pins B and C. About 2v is induced across windings N2 and N3 with polarities as shown. Increased current flow through the forward-biased D26 to +6v now sets the base of T4 to −1.1v. The emitter follower output decreases toward −0.8v and forward-biases T5 on. With T5 on, a +U output appears at pin A. R21 limits the voltage swing seen at pin D to a usable current mode P line output.

Circuit operation is the same when the core is switched off (reset). However, the voltages developed across N2 and N3 are now of opposite polarity to those assumed when the core was set. Greater current now flows through D27 and lowers the base voltage of T4 to −1.1v.

The turn-on delay is measured from the time the input signal starts to rise until the CTDL output signal reaches the −5.26v point. Turn-off delay data are not given as the delays cannot be referenced to the driving pulse.





HJ-- 371530

Input Levels		Output Levels		Delays		(usec)	On Output Current
Min.	Max.	Min	Max.		Per	Circuit	
+3 / -3	+6 / -6	5.76 / -5.76	6.24 / -6.24	Turn On	Min.	0.17	250 ma
					Max.	0.30	
				Turn Off	Min.	0.12	
					Max.	0.23	

Core Adder Driver

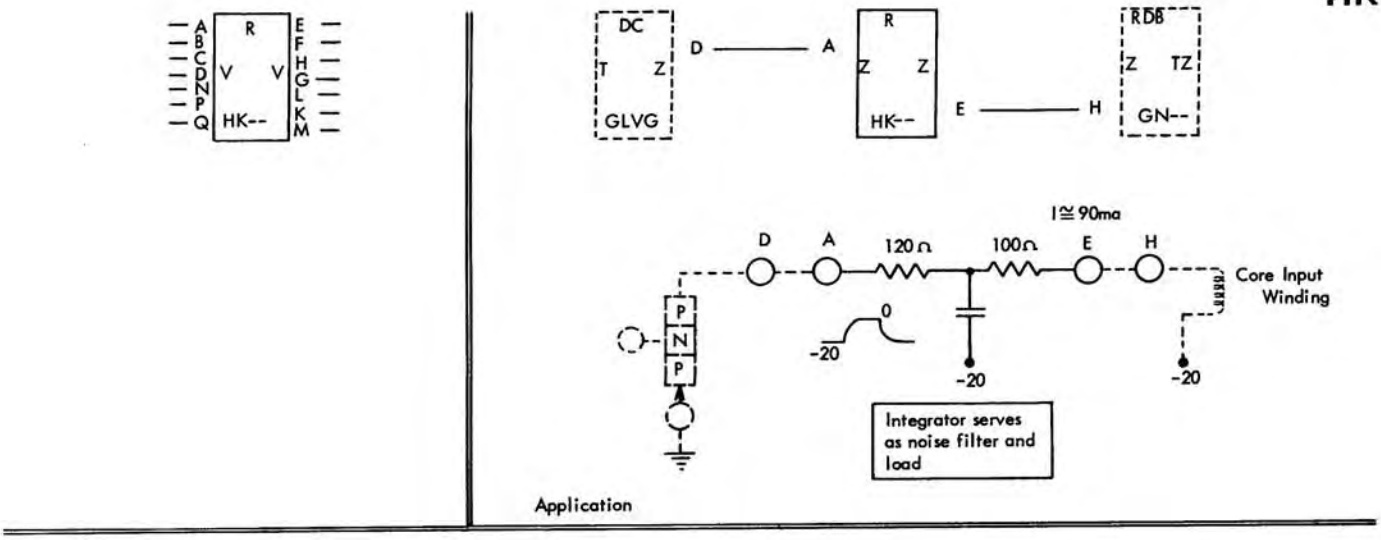
The HJ - - card consists of two core adder driver circuits that provide the necessary current to the core adder and core translator input windings. Each circuit is controlled by a T line signal and T line gate inputs. Both the gate and signal inputs must be down to have output current flow.

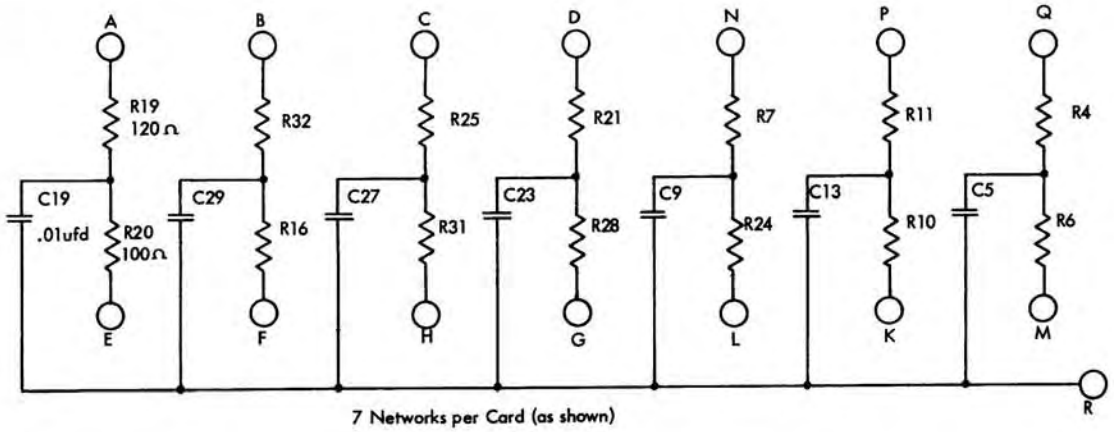
Circuit Description

In a quiescent state, T1 is forward-biased on and its collector voltage is near −11.2v. T2 is reverse-biased off and no current flows in the core windings. When the gate is up, conduction through R7 and R21 to the +6v level prevents the −T input signal from turning off T1. T1 continues to conduct and keeps its collector voltage near −11.2v. T2 is reverse-biased off and no output current flows through the core winding.

Coincidence of a −T gate and a −T signal level permits the base of T1 to be reverse-biased off. The voltage at the collector of T1 increases toward +6v, but clamps at −5.7v when T2 becomes forward-biased and conducts. T2 provides up to 300ma to the core adder or translator input winding.

The RC time of C6 and R9 is such that the signal coupled to the base of T1 is of essentially the same duration as the signal input pulse. The divider network of R2 and R3 sets the emitter voltage of the input transistors on circuits 1 and 2 to −11.5v. For reliable operation, the gate input must be set at least 0.7 microseconds before the sample pulse is applied.





Card Code	Part No	Circuit Use
HK--	371543	R

Integrator Load Card

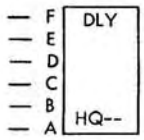
The HK - - card consists of seven integrator networks used in the input-output area. These integrator networks serve as load and filter networks between the core drivers and the core input windings. Special mode input and output signals are associated with the integrator networks.

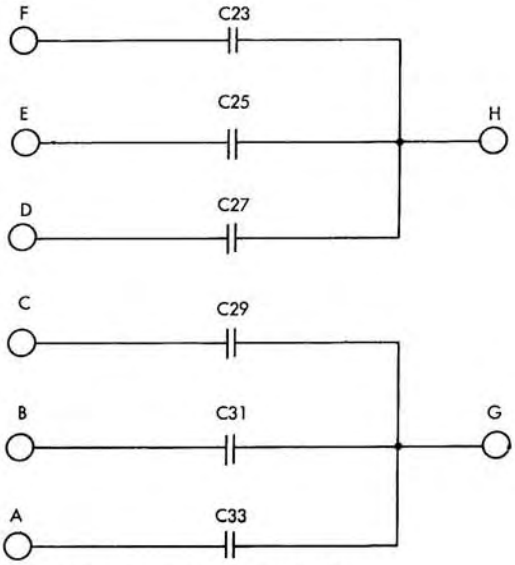
Circuit Description

When the core driver is off (as shown above), no current flows to the core input windings. The capacitor is discharged and the voltage at pin E is −20v. A negative input to the core driver transistor causes the transistor to turn on, which increases the input voltage level of the integrator to 0v. A surge current from the capacitor through the 120 ohm resistor and the transistor quickly charges the capacitor and sets the integrator output to 0v. Conduction from the −20v supply through the core input winding to the integrator and core driver is enough to set the core on.

Application

These integrator networks are normally used with the word size buffer core cards (GN - -).





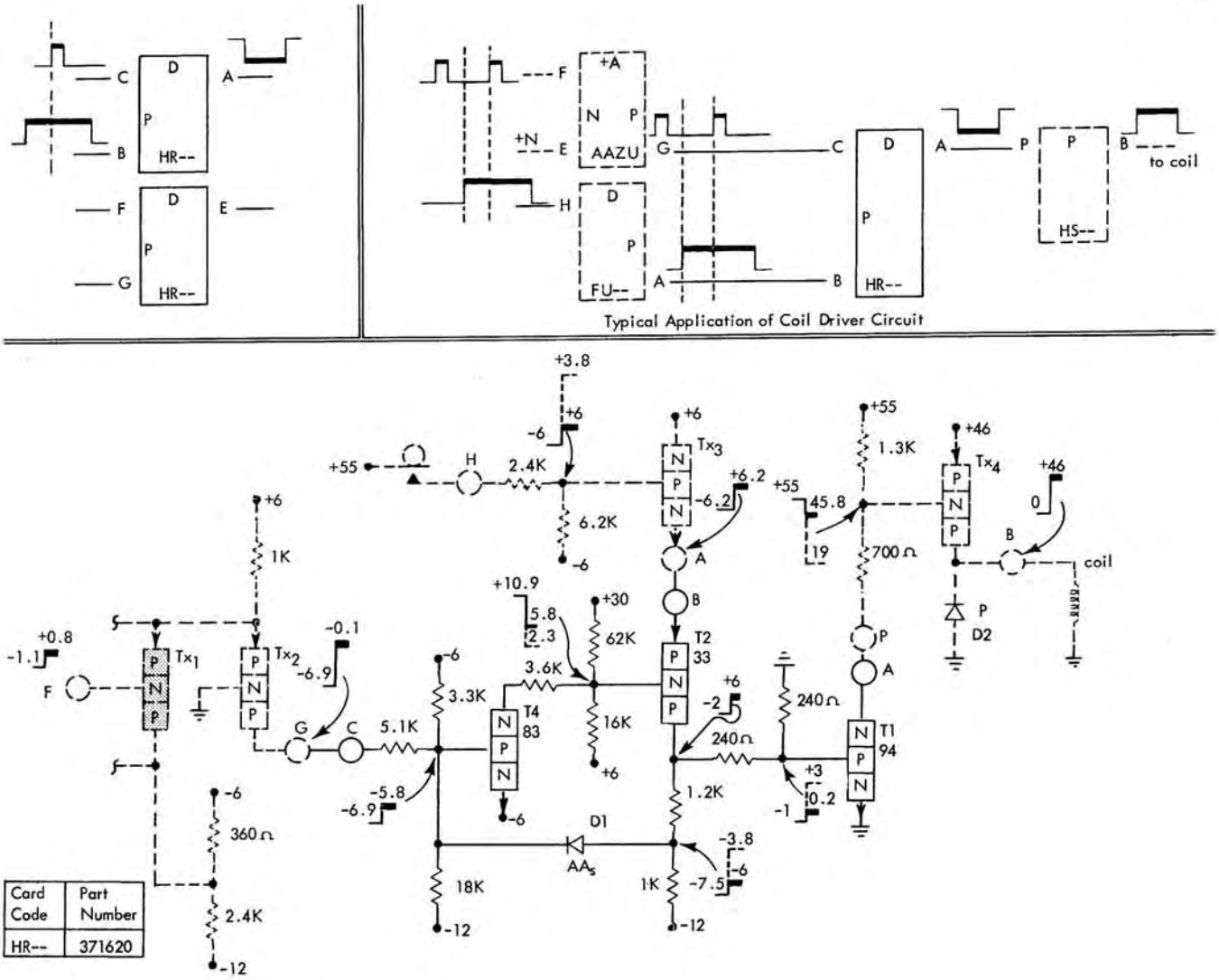
All Capacitors Values are 0.0010ufd

These capacitors are normally used to compensate for skew between logic blocks. They may also serve as coupling capacitors if required.

Card Code	Part No	Circuit Use
HQ--	371544	Dly CAP

Ring Delay Network

The HQ - - card consists of six 0.0010 μfd capacitors. Grouping the capacitors as shown and returning the capacitors to terminal pins permits their use in several circuits in a system.These capacitors are used in current mode trigger ring circuits and are tied to the outputs of the cross-coupled logic blocks making up the triggers. The capacitors provide a slight delay of the feed back signal and compensate for line skew at the inputs. The slight delay insures positive switching action of the trigger. These capacitors also serve as coupling or filter capacitors by proper back panel wiring.



Typical Application of Coil Driver Circuit

Card Code	Part Number
HR--	371620

Current Mode, Coil Driver Latch

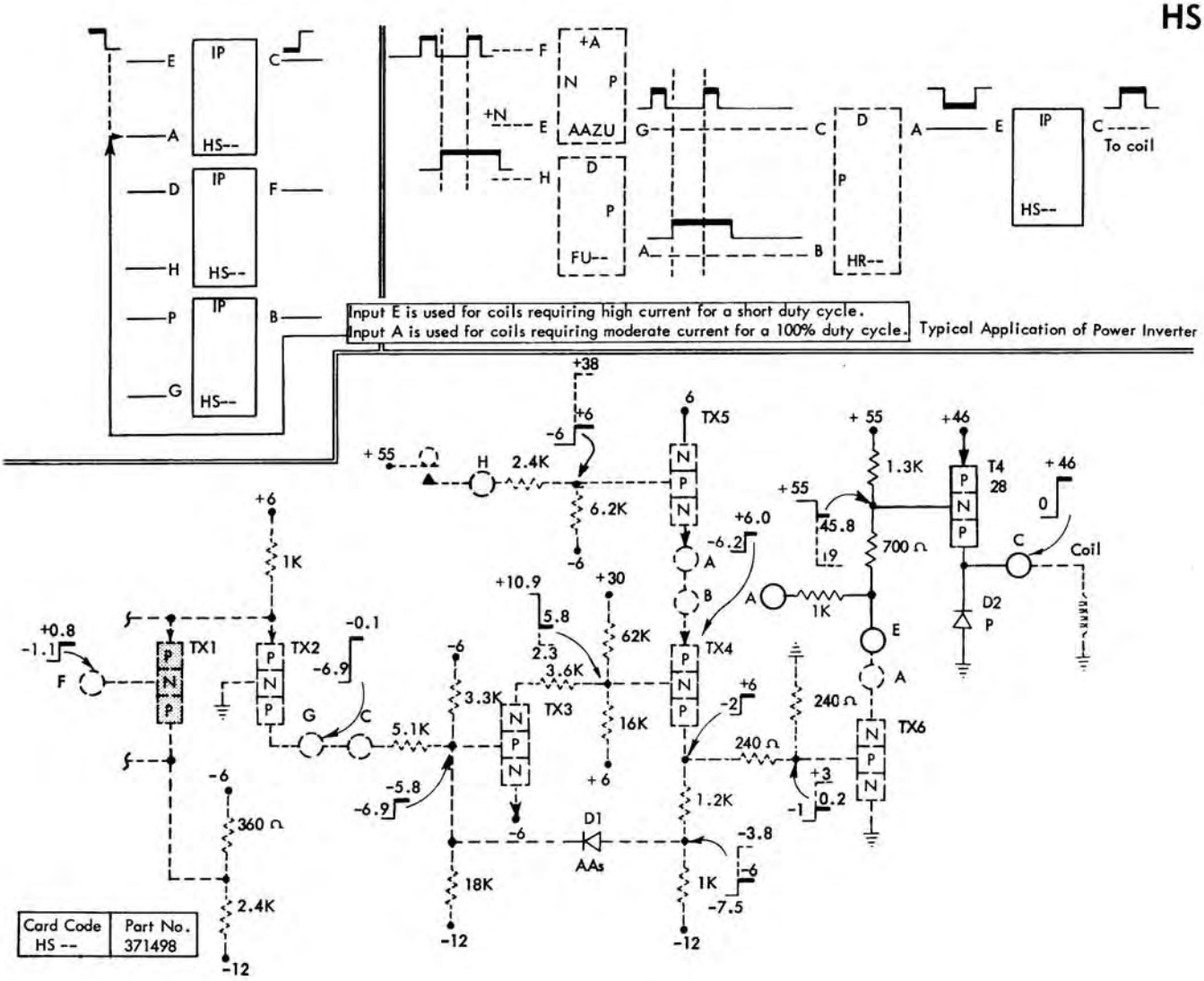
The HR - - coil driver latch is designed to work with the FU - - gate and reset card and the HS - - coil driver card. The HR - - driver develops a negative output when it recognizes a coincidence of plus inputs. Once picked, it latches for the duration of the gate signal supplied to it by the FU - - gate and reset driver (see logic application above). The FU - - driver accepts a +55v CB input and provides a +6v output to gate HR - -. The HS - - card is a power inverter which, when impulsed by HR - -, develops a +46v output and provides enough current to pick a coil. The HR - - card is described here as part of a multi-card coil driver circuit so over-all circuit function and purpose are better visualized.

Circuit Description

As shown, TX1 is forward-biased and TX2 is reverse-biased. T4, T2, and T1 are reverse-biased because divider currents have established their base levels as shown. Tx3 and TX4 are reverse-biased by their base return potentials. The output of TX4 is 0v and the coil is not picked.

When the CB closes, the base divider of TX3 attempts to rise to +38v but its collector-to-base is forward-biased and the base clamps to +6v. The emitter of TX3 follows its base upward so the emitter of T2 is now gated to receive an input to its base. When the input to TX1 rises, TX2 is forward-biased and TX1 is cut off. Current flow from −12v through 18K, 5.1K, and TX2 to +6v raises the base potential of T4 and it conducts. Current flow from −6v through T4, 3.6K, and 62K to +30v attempts to lower the base of T2 to +2.3v which forward-biases T2. Current flow from −12v through 1K, 1.2K, T2, and TX3 to +6v raises the base level of T1 and it conducts. The drop across the 1K resistor attempts to raise the anode of D1 to −3.8v which forward-biases D1. Current flows from −12v through 18K, D1, 1.2K, T2, and TX3 to +6v. Thus, the base of T4 remains forward-biased after TX2 is cut off because T4 is now latched by D1. This latch is maintained until the +55v CB source is removed. Current flow through T1 to +55v lowers the base level of TX4 and it conducts. Current flows through the coil and TX4 to +46v and the coil picks. D2 absorbs the coil voltage on dropout.

The circuit is dropped out by opening the CB which lowers the base and emitter potential of TX3 to −6v which drops out T2 and TX3. With T2 cut off, D1, T4, T1, and TX4 cut off.



Current Mode, Coil Driver Power Inverter

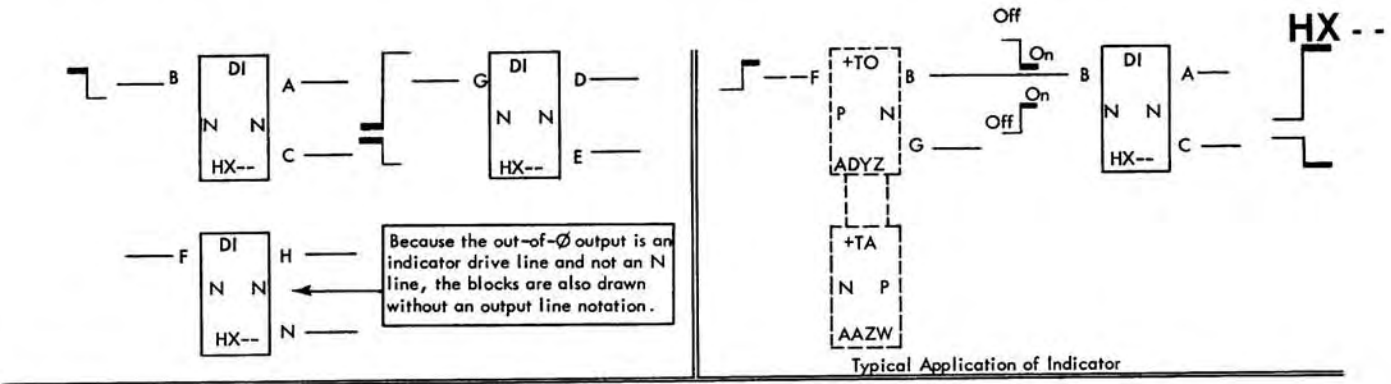
The HS - - coil driver is designed to work with the HR - - coil driver latch circuit. When the HS - - driver receives a negative input from HR - -, it develops a +46v output and provides enough current to pick a coil (see logic application above). The HS - - card is presented here as a part of a multicard coil driver circuit so overall circuit function and purpose are better visualized. The HR - - driver develops a negative output when it recognizes a coincidence of plus inputs. Once picked, it latches for the duration of the gate signal supplied to it by the FU - - gate and reset driver. The FU - - driver accepts a +55v CB input and provides a +6v output to gate HR - -.

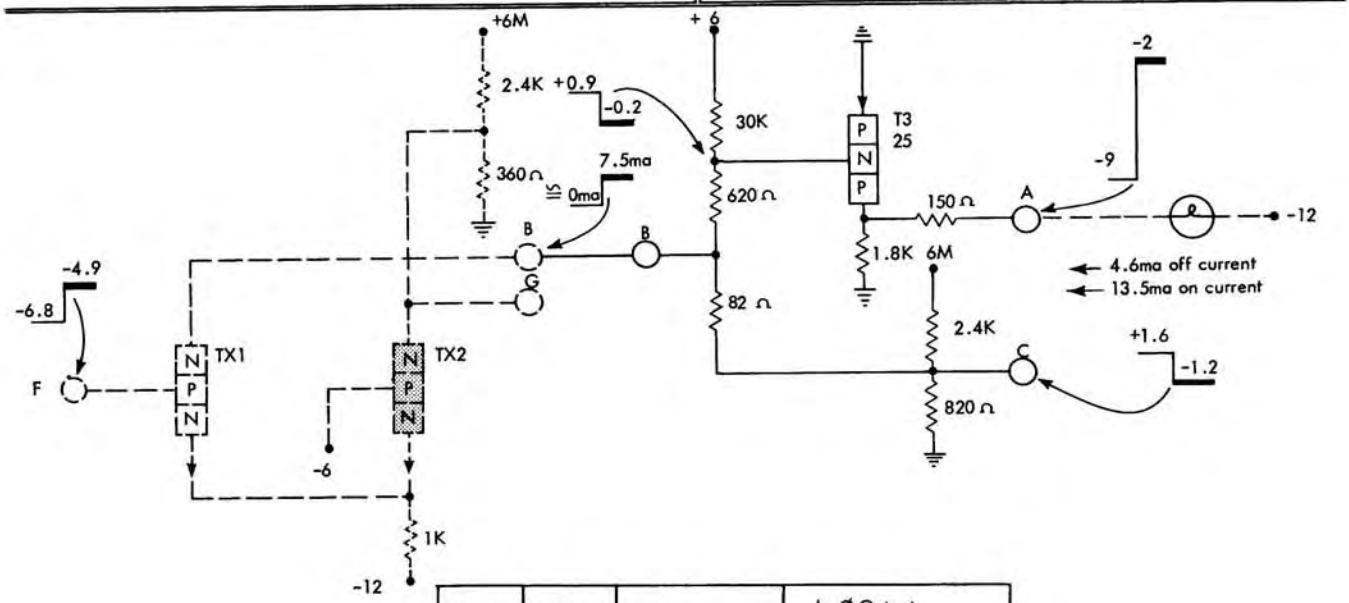
Circuit Description

As shown, TX1 is forward-biased and TX2 is reverse-biased. Tx3, TX4, and TX6 are reverse-biased because divider currents have established their base levels as shown. T4 and TX5 are reverse-biased by their base return potential. The output of T4 is 0v and the coil is not picked.

When the CB closes, the base divider of TX5 attempts to rise to +38v, but its collector-to-base is forward-biased and the base clamps to +6v. The emitter of TX5 follows its base upward so the emitter of TX4 is now gated to receive an input to its base. When the input to TX1 rises, TX2 is forward-biased and TX1 is cut off. Current flow from −12v through 18K, 5.1K, and TX2 to +6v raises the base potential of TX3 and it conducts. Current flow from −6v through TX3, 3.6K, and 62K to +30v attempts to lower the base of TX4 to +2.3v which forward-biases TX4. Current flow from −12v through 1K, 1.2K, TX4, and TX5 to +6v raises the base level of TX6 and it conducts. The drop across the 1K resistor attempts to raise the anode of D1 to −3.8v which forward-biases D1. Current flows from −12v through 18K, D1, 1.2K, TX4, and TX5 to +6v. Thus, the base of TX3 remains forward-biased after TX2 is cut off because TX3 is now latched by D1. This latch is maintained until the +55v CB source is removed. Current flow through TX6 to +55v lowers the base level of T4 and it conducts. Current flows through the coil and T4 to +46v and the coil picks. Input A increases the input resistance to T4 by 1K which reduces the forward bias of T4 and thereby limits current through T4. D2 absorbs the coil voltage on drop-out.

The circuit is dropped out by opening the CB which lowers the base and emitter potential of TX5 to −6v which drops out TX4 and TX5. With TX4 cut off, D1, TX3, TX6, and T4 cut off.





Card Code	Part No 37----	Input Current		In Ø Output Min.	In Ø Output Max.
HX--	1049	Min.	4.82	-0.4	1.7
		Nom.	7.5	+0.4	
		Max.	10.38	-2.4	

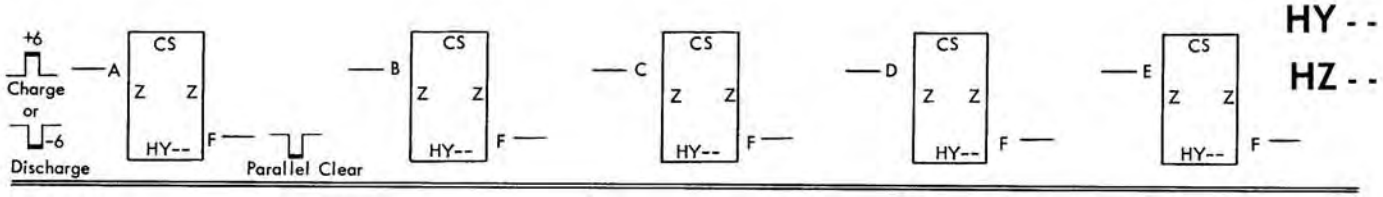
Current Mode, —N Line Indicator

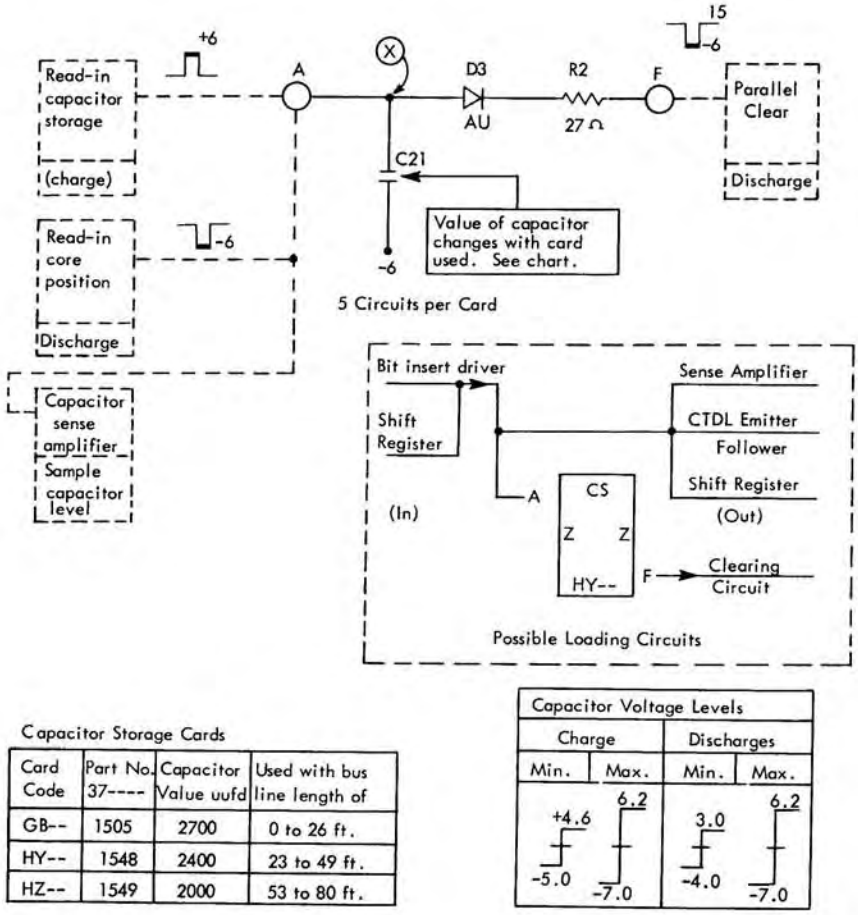
The HX - - card consists of three indicator circuits. Each circuit requires a —N line input to turn on the indicator lamp connected to the out-of-phase output. Each circuit also provides an in-phase N line output capable of driving two N type logic blocks. The signal levels associated with the indicator output are special purpose levels of —2v to —9v.

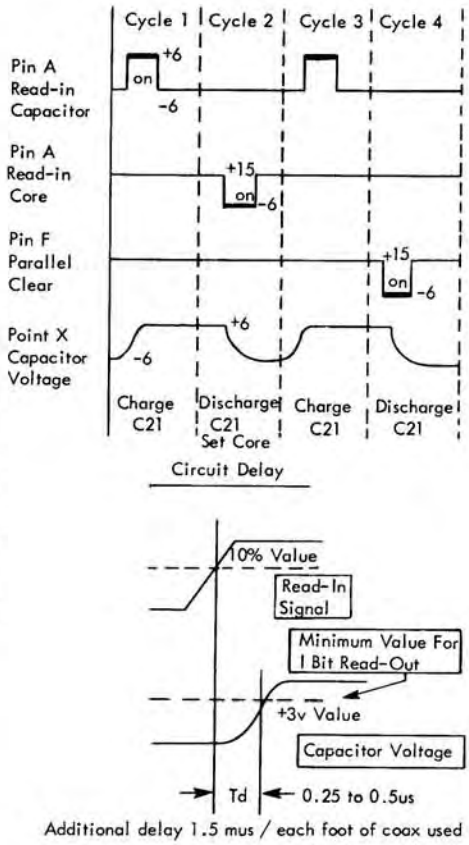
Circuit Description

In the state shown, TX1 is reverse-biased and input current to the indicator is zero. Divider current through the 820 ohm, 2.4K coupling network establishes output C at a +N level of +1.6v. Current flow out of this network through the 30K resistor to +6v sets the base level of T3 at +0.9v and T3 is reverse-biased. The 5ma current flow from —12v through the lamp and the 1.8K resistor to ground is not enough to light the lamp. This current flow sets output A at a —9v level.

When the input to TX1 rises, TX1 is forward-biased and 7.5ma flows from —12v, through TX1 into the indicator where it divides into two components of current. One component flows into the coupling network which establishes output C at a —N level of —1.2v; the other flows through the 620 ohm and 30K resistor to +6v which drives the base of T3 below ground. T3 is forward-biased and the 13.5ma which flows from —12v through the lamp, 150 ohm resistor, and T3 to ground is enough to light the lamp. The voltage drop across the 150 ohm resistor and T3 is 2v so output A is at a —2v level.







Capacitor Storage Cards

Card Code	Part No. 37----	Capacitor Value uufd	Used with bus line length of
GB--	1505	2700	0 to 26 ft.
HY--	1548	2400	23 to 49 ft.
HZ--	1549	2000	53 to 80 ft.

Capacitor Voltage Levels

Charge		Discharges	
Min.	Max.	Min.	Max.
+4.6 to -5.0	6.2 to -7.0	3.0 to -4.0	6.2 to -7.0

Capacitor Storage

The HY - - card consists of five capacitor storage circuits, each capable of storing one binary bit by virtue of its two possible states, charged and discharged. The input to the capacitor storage card is from the parallel output of a core register position or from a bit insert driver. Capacitor storage status is detected by sensing the voltage level on the capacitor. Capacitor storage outputs drive core register bit positions, sense amplifiers or CTDL emitter followers. The capacitor charge is removed by a special clearing circuit tied to pin F.

Circuit Description

Assume the capacitor storage circuit is connected as shown and that the capacitor is discharged (−6v).

Cycle 1, Charge Capacitor. When the read-in capacitor circuit at pin A is at +6v, conduction from point X to the read-in capacitor storage circuits charges the capacitor to +6v.

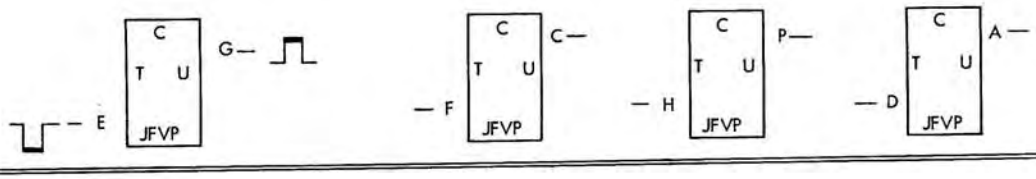
Cycle 2, Discharge Capacitor. The capacitor charge remains at +6v and may be sampled for system use until the read-in core driver circuit drops the voltage at pin A to −6v. The capacitor discharges to this value and the resulting discharge current is enough to set a magnetic core of a shift register position to the 1 state.

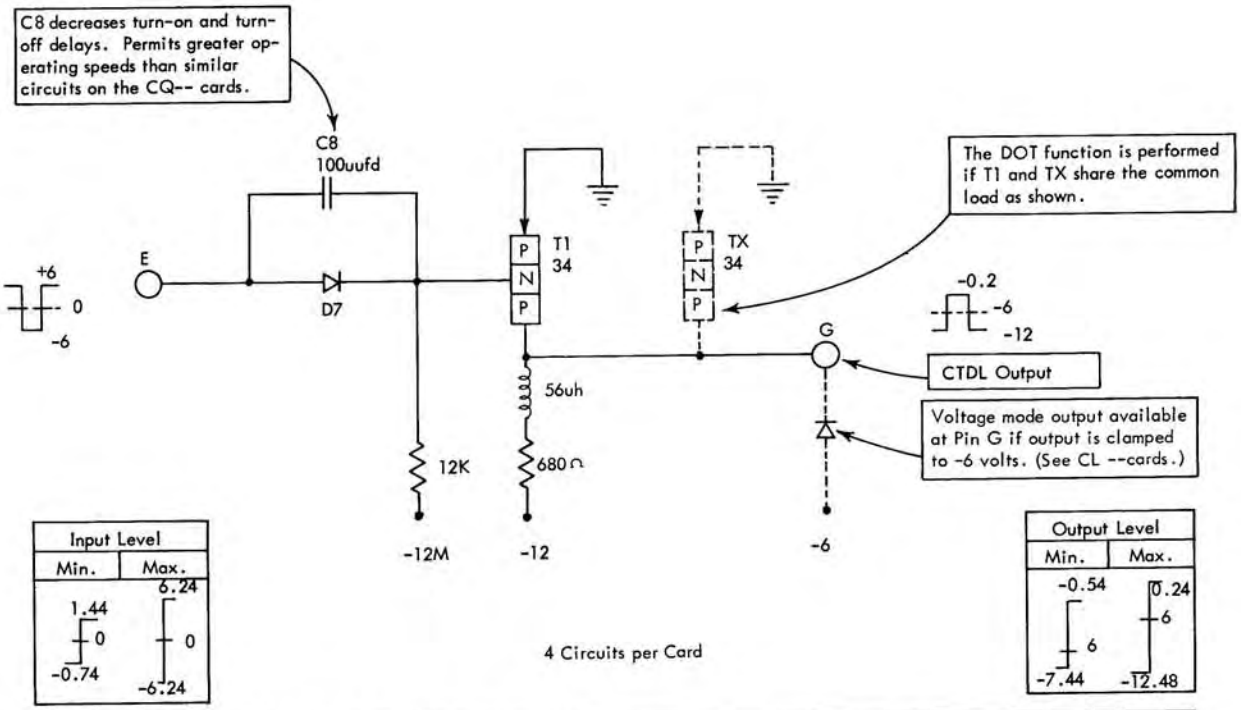
Cycle 3, Charge Capacitor. Again the read-in capacitor storage circuit causes the voltage at pin A to increase to +6v, and charges the capacitor to this value.

Cycle 4, Discharge Capacitor. To prevent the capacitor from being charged by the Ico of the shift register transistors, the parallel clear line is gated on at the end of each read-out cycle to discharge the capacitor. Discharge current from pin F, R2, and the forward-biased D3 reduces the voltage at point X to −6v. D3 provides isolation to the parallel clear circuit when it is off (+15v).

Application

In the 7070 system these cards serve as bus capacitors for transferring information bits to and from memory or core registers. The pulse duration of the capacitor charge varies from 2 to 4 microseconds depending on circuit use. The storage cards are used in both 4 and 6 microsecond transfer cycles. To compensate for line capacitance, three capacitor cards are available for driving different length bus lines.





Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Circuit 1	2	3	4	Delays	Per	Basic Block (usec)	Par'lel C'lector	CM Base	Diode Input	100 uufd	Circuit Use
JFVP	1576	No	No	Yes	Yes	Yes	Yes	Turn On	Min.	.075	.00	.00	.00	.02	+C
JFVN	1577	No	No	Yes	Yes	No	No		Max.	.22	.007	.015	.02	.05	+CO
JFVA	1578	No	No	Yes	No	No	No	Turn Off	Min.	.100	.004	.005	.00	.03	
JF--	1579	No	No	No	No	No	No		Max.	.150	.01	.02	.005	.06	

CTDL High Speed T-to-U Converter

The JFVP card consists of four one-way PNP logic circuits. Each circuit on the card converts a T input to an out-of-phase U output. This card is similar to the standard CTDL one-way block except that the input circuit is changed to permit a higher speed of operation. In this group of cards the base resistor is reduced in value and a capacitor is placed across the input diode. These changes reduce the turn-on and turn-off times of the transistor and result in faster switching action in the output circuit.

Circuit Description

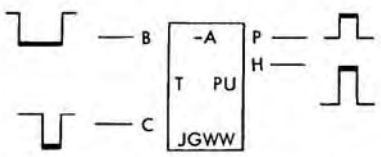
Assume a starting condition of T1 off as shown above. When the input signal decreases suddenly to −6v, a surge of current flows through the 12K resistor and C8. This current flow quickly drops the base voltage of T1 below ground and drives T1 into saturation. The output at pin G nears 0v minus the slight drop across T1. After the initial surge of current charges C8 and forward-biases T1 on, normal diode action insures that T1 remains in saturation for the remainder of the −T input signal.

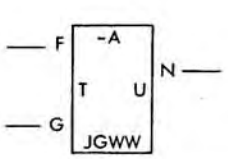
Similarly, when the input returns to +6v, current flow through the 12K resistor and C8 quickly raises the base level above ground potential and removes the minority carriers from the base region. T1 is biased-off and provides a −U output level at pin G. Conduction through D7 holds T1 off for the remainder of the +T input signal.

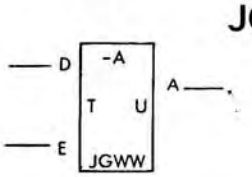
Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

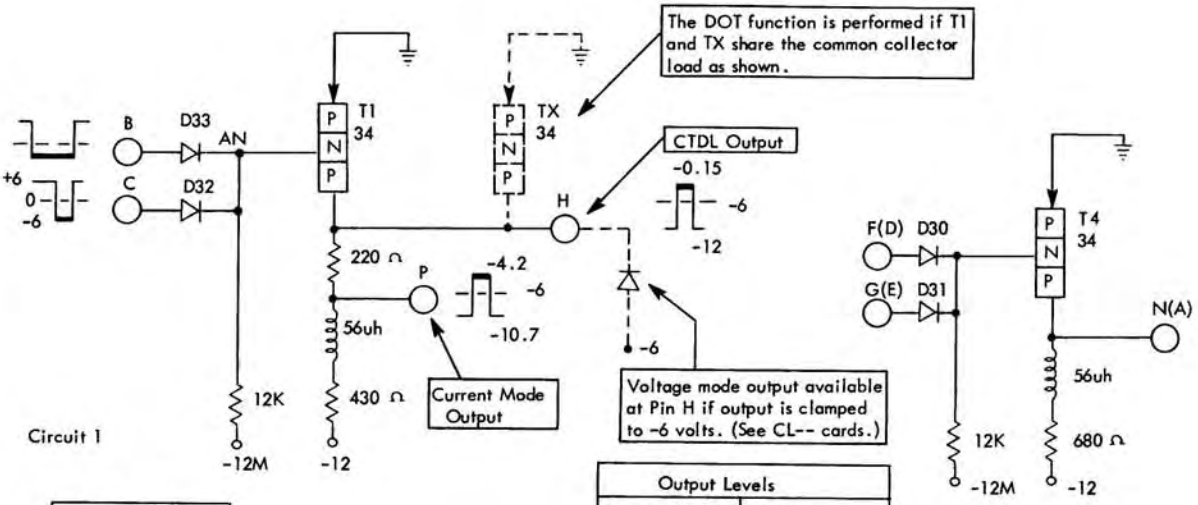
Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT function is accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.









Input Level	
Min	Max.
1.44 / -0.74	6.24 / -6.24

Output Levels			
Current Mode		CTDL	
Min.	Max.	Min.	Max.
-4.9 / -8.8	-3.5 / -6 / -12.48	-0.54 / -7.44	0.24 / -6 / -12.48

Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Circuit 1	2	3	Delays	Per	Basic Block (usec)	Par'lel C'lector (usec)	CM Base (usec)	Diode Input (usec)	100 uufd (usec)	Circuit Use
JGWW	1580	No	1	Yes	Yes	Yes	Turn On	Min.	.155	.000	.000	.000	.02	-A +O
JGVW	1581	No	1	Yes	Yes	No		Max.	.48	.007	.015	.020	.05	-AO
JGVV	1582	No	1	Yes	No	No	Turn Off	Min.	.07	.004	.005	.000	.03	+OA
JG--	1583	No	No	No	No	No		Max.	.15	.010	.020	.005	.06	C

CTDL High-Speed Two-Way —AND

The JGWW card consists of three two-way PNP logic circuits. Each circuit on the card normally performs a —AND and INVERT logical function which translates a T input to an out-of-phase U output. By decreasing the value of the input base resistor used in this circuit, faster switching of the output pulse results, in comparison to the identical circuit in the CGWW group.

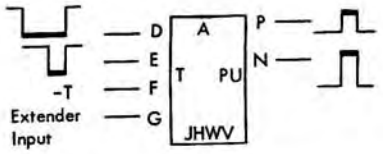
Circuit Description (Circuit 1)

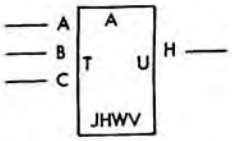
The —AND function is performed by the diode mix D33 and D32 returned to —12v, and the INVERT function is accomplished by the transistor circuit. Coincidence of —T levels is required at input pins B and C to forward-bias T1 into saturation. With T1 on, the output at pin H nears 0v (minus the small voltage drop across the transistor). When either of the input signals increases to +6v, T1 is turned off. The low forward impedance of the conducting logic diode rapidly removes the excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a fast response at the trailing edge of the output waveform. At this time the transistor acts as a high impedance and the output at pin H decreases to —12v. The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

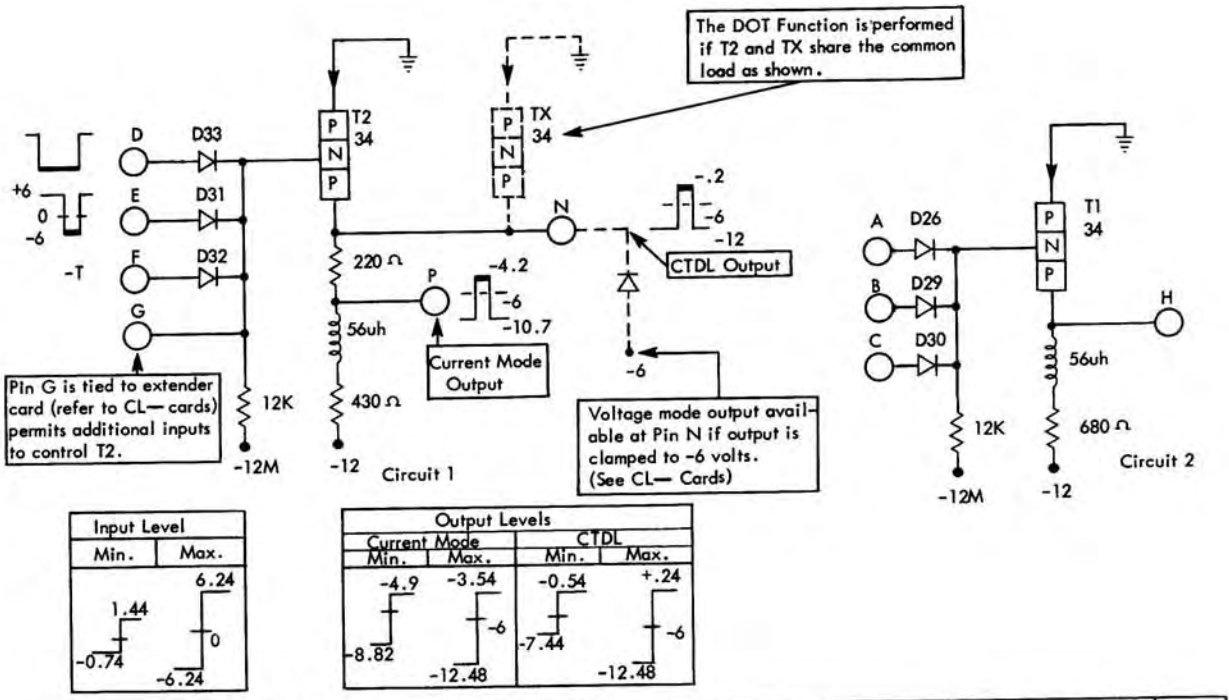
Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.







Card Code	Part No. 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Circuit 1	Collector Loading Circuit 2
JHWV	1584	1	1	Yes	Yes
JHVU	1585	1	1	Yes	No
JH--	1586	1	No	No	No

Delays (usec)		Per	Basic Block	Par'lel C'lector	CM Base	Diode Input	100 uufd	Circuit Use
Turn Off	Min.	.145	.00	.00	.00	.02	+O +OA C -A -AO
	Max.	.49	.007	.02	.02	.05	
Turn On	Min.	.075	.004	.005	.000	.03	
	Max.	.15	.01	.02	.005	.06	

CTDL High-Speed Three-way —AND

The JHWV card consists of two three-way PNP logic circuits. Each circuit on the card normally performs a —AND and INVERT logical function which translates a T input to an out-of-phase U output. By decreasing the value of the input base resistor used in this circuit, faster switching of the output pulse results, in comparison to the identical circuit in the CJWV group. Extender pin G permits additional inputs to control circuit 1.

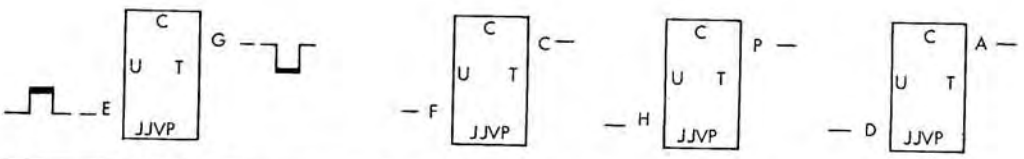
Circuit Description (Circuit 1)

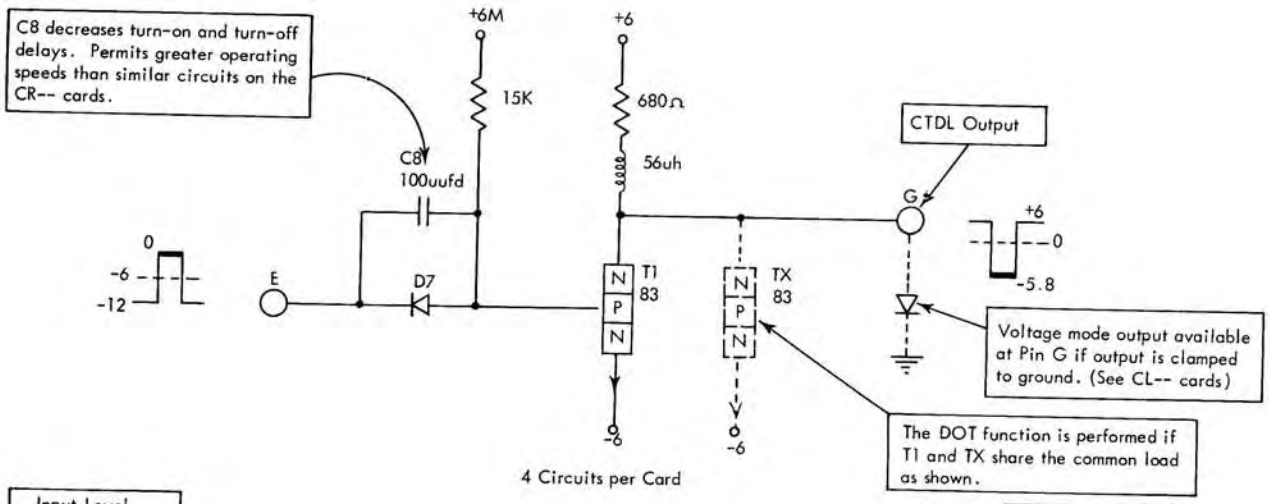
The —AND function is performed by the diode mix D33, D32, and D31 returned to −12v; the INVERT function is accomplished by the transistor circuit. Coincidence of −T levels is required at input pins D, E, and F to forward-bias T2 into saturation. With T2 on, the output at pin N nears 0v (minus the small voltage drop across the transistor). When any of the input signals increase to +6v, T2 is forced off. The low forward impedance of the conducting logic diode rapidly removes the excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin H decreases toward −12v. The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.





4 Circuits per Card

Input Level	
Min.	Max.
-5.3	0.24
-7.4	-6
	-12.48

Output Levels	
Min.	Max.
1.44	6.3
-5.5	-6.3

Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Ckt 1	Ckt 2	Ckt 3	Ckt 4	Delays	Per	(usec) Basic Block	Par'lel C'lector	CM Base	Diode Input	100 uufd	Circuit Use
JJVP	1587	No	No	Yes	Yes	Yes	Yes	Turn On	Min.	.09	.00	.00	.00	.02	+C
JJVN	1588	No	No.	Yes	Yes	No	No		Max.	.19	.007	.02	.02	.03	+CO
JJVA	1589	No	No	Yes	No	No	No	Turn Off	Min.	.015	.004	.005	.000	.03	
JJ--	1590	No	No	No	No	No	No		Max.	.09	.01	.02	.005	.06	

CTDL High Speed U-to-T Converter

The JJVP card consists of four one-way NPN logic circuits. Each circuit on the card converts a U input to an out-of-phase T output. This card is similar to the standard CTDL one-way block except that the input circuit is changed to permit higher speeds of operation. A capacitor is placed across the input diode to reduce the turn-on and turn-off times of the transistor, which results in faster switching action in the output circuit.

Circuit Description

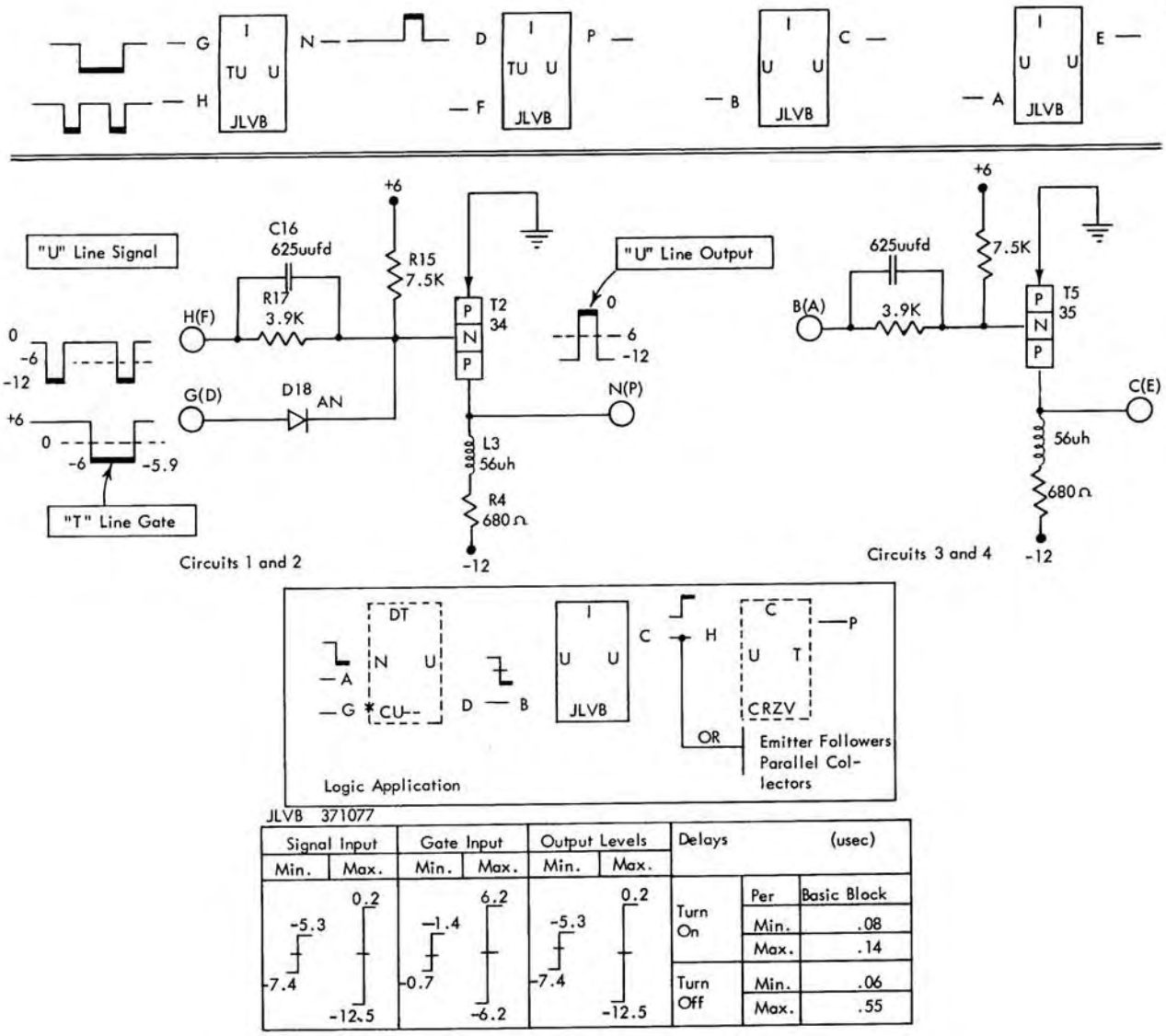
Assume a starting condition of T1 off as shown above. When the input signal increases suddenly to 0v, a surge of current flows through C8 and quickly forward-biases the base of T1. T1 is driven into saturation and provides a −T output at pin G. After the initial surge of current charges C8 and forward-biases T1 on, normal diode action insures that T1 remains in saturation for the remainder of the +U input signal.

Similarly, when the input signal returns to −12v, current flow through C8 quickly drops the base level below −6v and rapidly removes the minority carriers from the base region. T1 is biased off and provides a +T output level at pin G. Conduction through D7 holds T1 off for the remainder of the −U input signal.

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading for the different cap connections in this group of cards is noted on the circuit diagram. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT function is accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.



JLVB 371077

Signal Input		Gate Input		Output Levels		Delays		(usec)
Min.	Max.	Min.	Max.	Min.	Max.			
-5.3 / -7.4	0.2 / -12.5	-1.4 / -0.7	6.2 / -6.2	-5.3 / -7.4	0.2 / -12.5			
						Turn On	Per	Basic Block
							Min.	.08
							Max.	.14
						Turn Off	Min.	.06
							Max.	.55

CTDL PNP Logic Inverter

This card consists of four PNP non-translating inverter circuits used for current amplification. All circuits function as CTDL U line inverters and provide the drive to P type logic blocks. Circuits 1 and 2 have an additional T line gate input that controls the transistor bias level for these circuits. When both inputs are used, the gate and signal inputs must be down for transistor turn-on. All circuits have internal collector loads.

Circuit Description (Circuits 1 and 2)

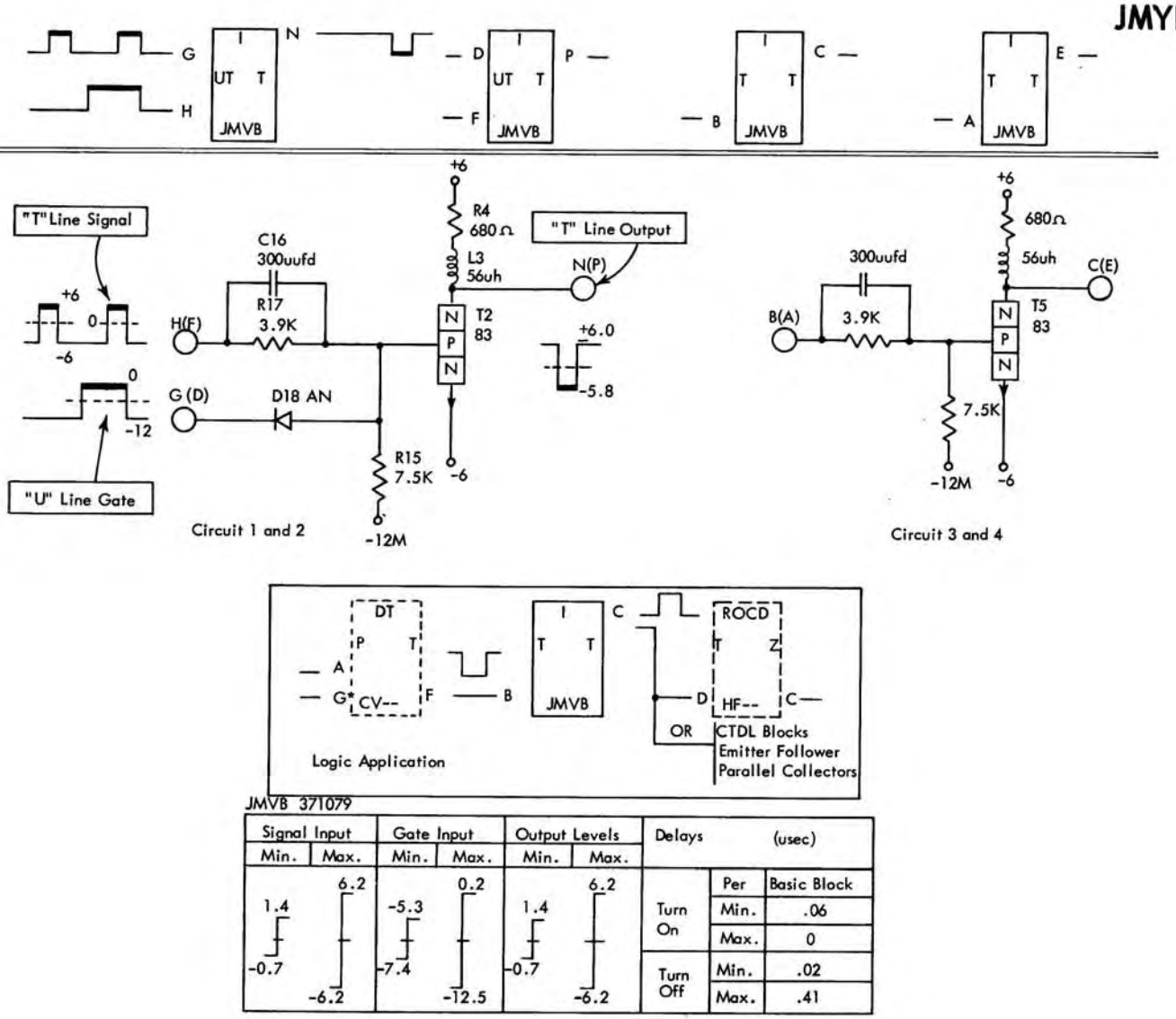
Gate Up — Signal Up. When the gate is up at pin G and the signal input is up at pin H, conduction through R17 to D18 and R15 sets the base of T2 to approximately +6v. T2 is reverse-biased off and the output at pin N is at −12v.

Gate Down — Signal Up. With a −T gate input at pin G and a +U signal input at pin H, conduction through R17 and R15 sets the base of T2 near +2.1v. T2 remains reverse-biased off and the output at pin N stays at −12v.

Gate Down — Signal Down. When a −T gate input is applied to pin G and a −U input is applied to pin H, conduction through R17 and R15 to D18 forward-biases T2 on. The output at pin N increases rapidly to ground potential, and current flows in an external load. C16 improves the shape of the output signal.

Application

These circuits provide inversion of a U line input signal, and drive into CTDL logic blocks or emitter followers.



JMVB 371079

Signal Input		Gate Input		Output Levels		Delays		(usec)
Min.	Max.	Min.	Max.	Min.	Max.			
1.4 to -0.7	6.2 to -6.2	-5.3 to -7.4	0.2 to -12.5	1.4 to -0.7	6.2 to -6.2		Per	Basic Block
						Turn On	Min.	.06
							Max.	0
						Turn Off	Min.	.02
							Max.	.41

CTDL NPN Logic Inverter

This card consists of four NPN non-translating inverter circuits used for current amplification. All circuits function as CTDL T line inverters and provide the drive to N type logic blocks. Circuits 1 and 2 also have an additional U line gate input which controls the transistor bias level for these circuits. When both inputs are used, both the gate and signal inputs must be up for transistor turn-on.

Circuit Description (Circuits 1 and 2)

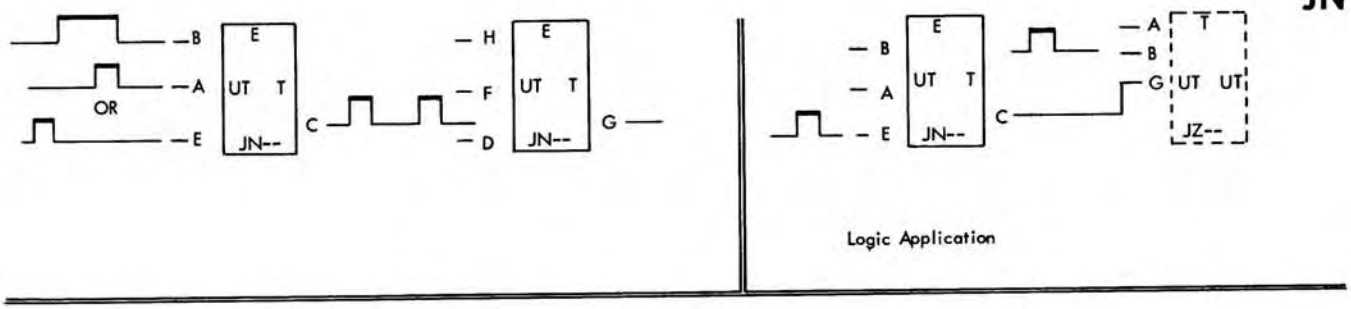
Gate Down — Signal Up. When the gate is down at pin G and the signal input is up at pin H, conduction through D18 and R15 to R17 and the +6v signal sets the base of T2 near −12v. T2 is reverse-biased off and the output at pin N is +6v.

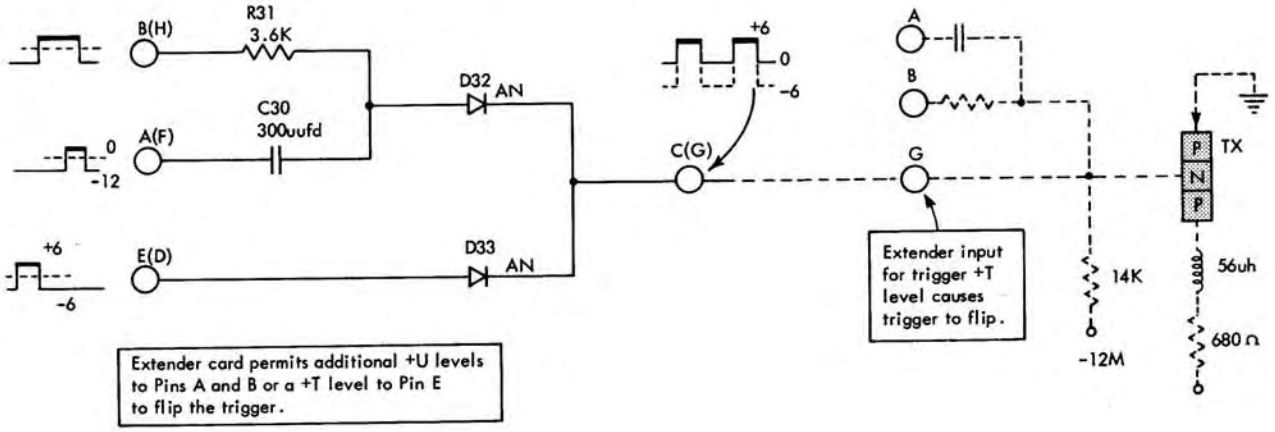
Gate Up — Signal Down. If the gate is up at pin G and the signal input is down at pin B, conduction from −12v through R15 and R17 to pin H sets the base of T2 near −8.5v. The transistor remains reverse-biased and the CTDL output at pin N stays at +6v.

Gate Up — Signal Up. When the gate input at pin G is up, and the signal input at pin H is up, conduction through D18 and R17 and R15 and R17 to the +6v signal input increases the base voltage above −6v and drives T2 into saturation. The output voltage at pin N is approximately −6v (minus the small drop across the forward-biased transistor). C16 improves the shape of the output signal. The peaking coil L3 provides a high impedance when T2 is first turned on, and improves the leading edge of the output wave.

Application

These circuits provide inversion of a T line input signal and drive CTDL logic blocks or emitter followers.





JN-- 371081

"U" Line Inputs		"T" Line Inputs	
Min:	Max.	Min.	Max.
-5.3	0.2	1.44	6.2
-7.4	-6	-0.74	0
	-12.5		-6.2

CTDL Trigger Extender Card

The JN - - card consists of two circuits used for expanding the inputs to the CTDL trigger 2 circuit (JZ - - card). Each extender on this card permits an additional DC set or a gated AC set to control the trigger.

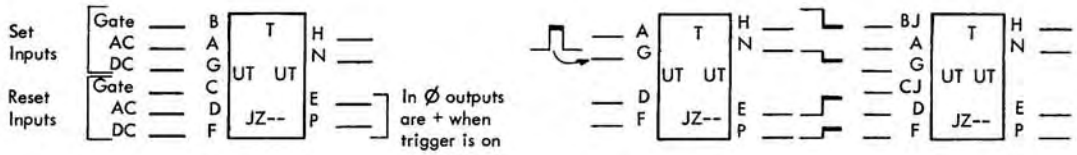
Circuit Description

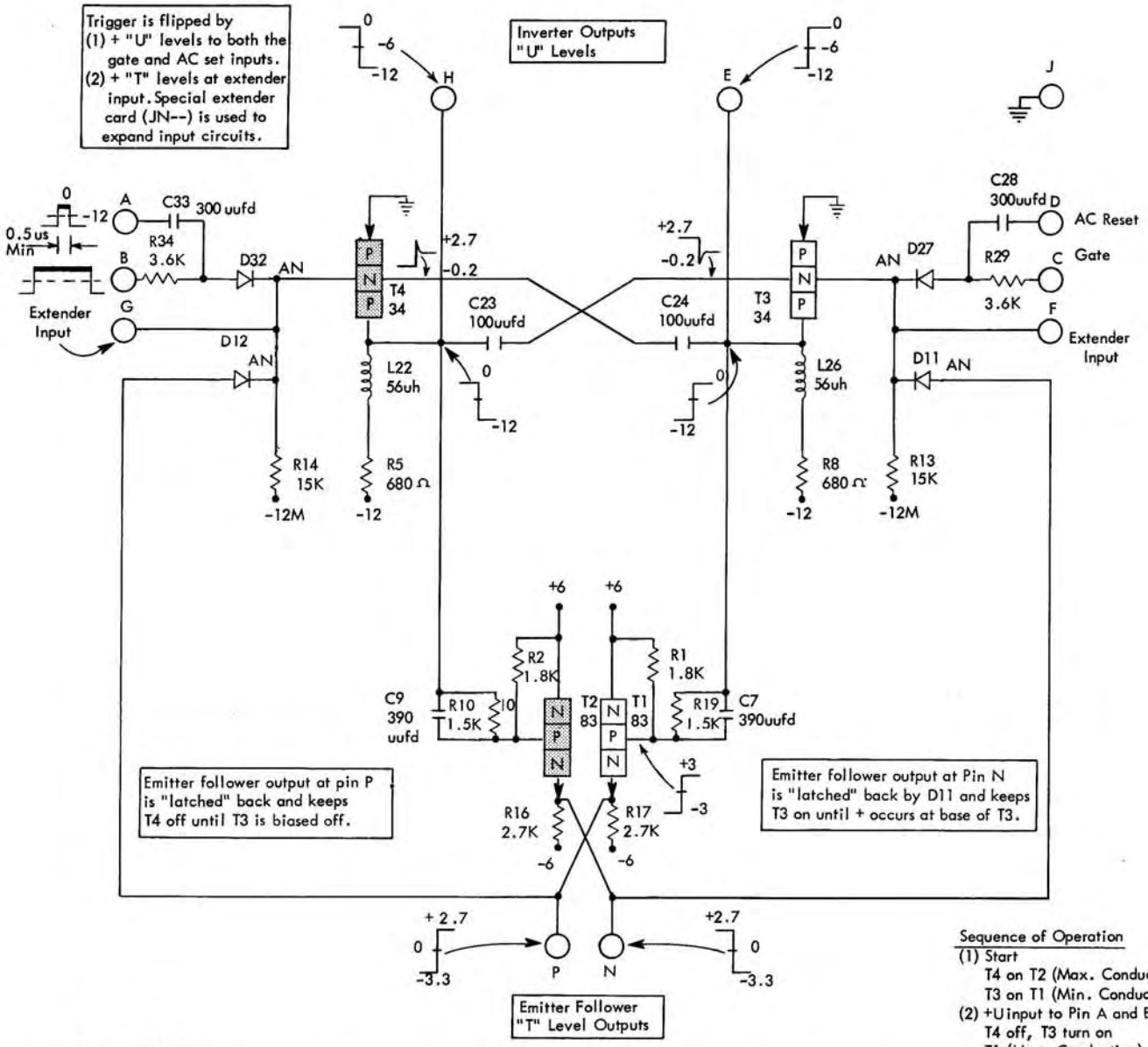
DC Set Input. A +T level input applied to pin E provides a positive input to the base of TX and starts the triggering action. Refer to JZ - - card for complete CTDL trigger circuit operation.

AC Set Input. A +U level at both the gate input at pin B and the signal input at pin A also provides a positive level at the base of TX to start the triggering action. D32 and D33 provide isolation between the input circuits.

Application

The extender cards are used with CTDL trigger circuits that require additional control inputs.





JZ-- 371082

Input Levels				Output Levels				Delays * (usec)				
Extender "T" In		AC Set and Gate		Emitter Follower		Inverter			Inverter		Emitter Follower	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
0.5 to -7.4	+0.2 to -12.4	1.4 to -0.7	6.2 to -6.2	1.4 to -0.7	3.1 to -5.2	-5.2 to -7.4	-0.8 to -9.2	Turn On	.1	.3	.08	.04
								Turn Off	.15	..8	.055	0.1

* Measured from 10% to 90% values

Sequence of Operation

(1) Start
T4 on T2 (Max. Conduction)
T3 on T1 (Min. Conduction)

(2) +U input to Pin A and B
T4 off, T3 turn on
T1 (Max. Conduction)
T2 (Min. Conduction)

(3) Emitter Follower outputs latch trigger in this state until + signal appears at base of T3 and returns trigger to its original state.

CTDL Trigger 2

The JZ - - card consists of a CTDL trigger circuit designed for use in clock and ring circuits and as a single bit memory device. The bistable circuit consists of two inverters and two emitter followers operated at a frequency near 250kc. A positive CTDL signal applied to the AC set and gate inputs or to the extender inputs control the triggering action. Both in-phase and out-of-phase outputs are available from this card.

This card differs from the CTDL trigger circuit on the CW - - card in that extender inputs are provided on this card in place of the DC set inputs. A special trigger extender card (JN - -) is available that permits additional inputs to control the trigger.

AC Set Input and Gate. When the trigger is used as a single-bit memory device, both the signal input and the gate input are driven by CTDL U lines. The gate sets the reference threshold for the AC set input and must be conditioned 3.75μs before the set signal is applied. If the gate is up, a positive U line shift having a minimum pulse duration of 0.5μs is required to flip the trigger.

Circuit Description

Assume a starting condition of T4 and T2 conducting and T3 and T1 off. When coincidence of +U levels occurs at pin A and pin B, the base of T4 becomes more positive than the emitter (ground potential). T4 becomes reverse-biased off and causes its collector voltage to drop to −12v.

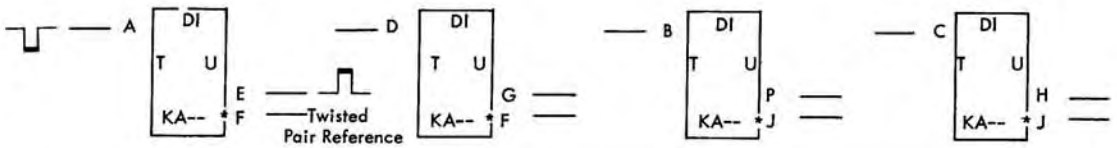
This negative swing is coupled through C23 to forward-bias T3 on and also to T2 to decrease the conduction through the emitter follower. Conduction through T3 causes its collector voltage to increase to 0v. This positive swing is coupled to T4 by C24 (keeping it cut off) and also to the base of T1. T1 becomes more forward-biased and conducts harder, causing the emitter follower output (pin P) to increase to +2.7v. This up level is latched back through D12 to keep T4 cut off. If +U levels are now applied to pins D and C, the trigger is flipped to its original state. The positive level at the input pins cuts off T3, causing its collector to drop to −12v.

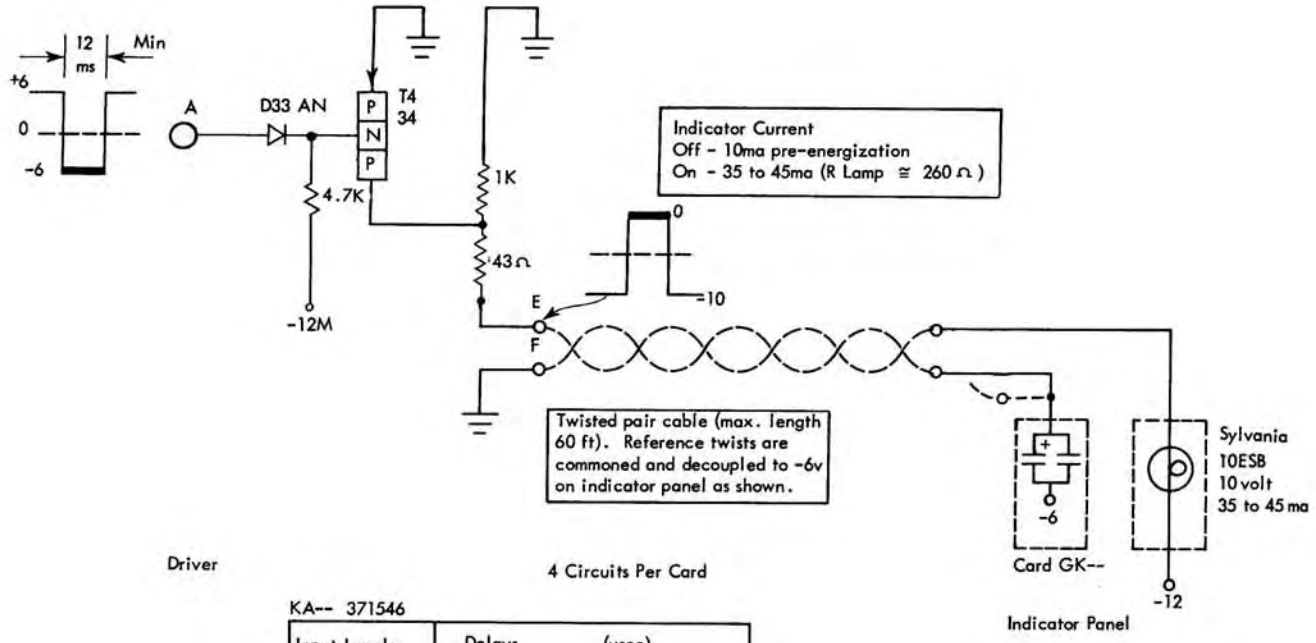
This negative shift is coupled through C24 to forward-bias T4, and drive it into conduction. The collector voltage of T4 goes to 0v and allows the emitter follower T2 to conduct more. The positive shift at the collector of T4 is also coupled through C23 to keep T3 cut off. The emitter follower output at pin N (+2.7v) is latched back through D11 to keep T3 cut off.

The turn-on and turn-off delays are a function of circuit loading and are noted above for nominal conditions. Overall trigger delays in flipping from state to state average from 0.12μs to 0.45μs.

Application

This circuit is used mainly in ring applications (e.g., digit and word rings) to provide output pulses of a specific duration. It is also used as a storage device in a binary operation. Various logic block configurations for the trigger are illustrated above.





Driver

4 Circuits Per Card

KA-- 371546

Input Levels	Delays (usec)		
+6.24 / +1.56 / -0.56 / -6.24	Turn On	Min.	Max.
		.17	.80
	Turn Off	.18	.29

High Current Indicator Driver

The high current indicator driver card (KA - -) supplies 35 to 45ma to a 10v incandescent lamp (Sylvania 10 ESB). The circuit is a basic PNP inverter requiring a −P pulse duration of 12 milliseconds to produce a visual indication within the lamp. Four indicator drivers are located on each card.

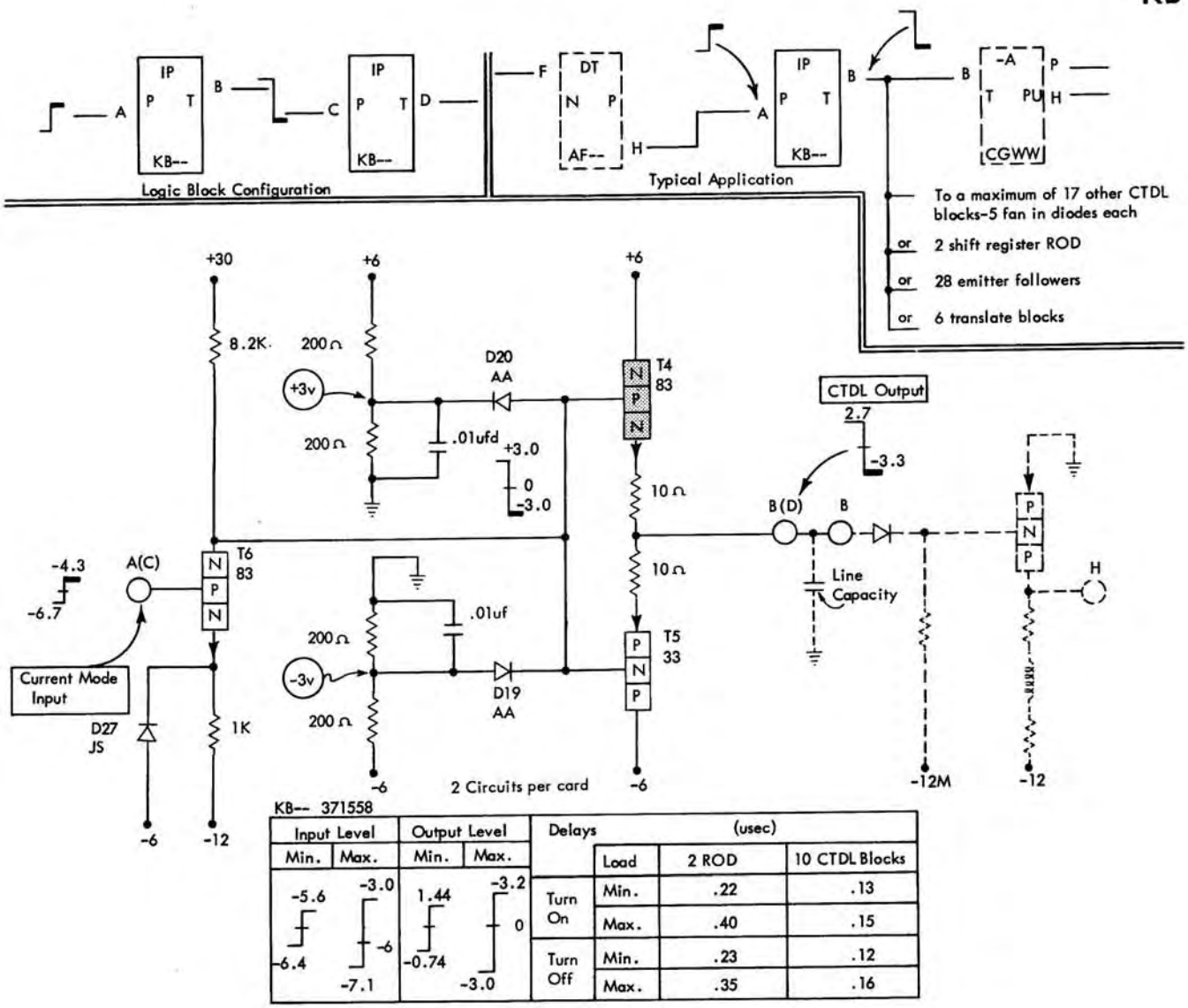
Circuit Description

With a +T input at pin A, T4 is reverse-biased off. A pre-energization current of 10ma flows through the lamp, the 43 ohm and the 1K resistors to ground. This current, however, is not sufficient to give a visual indication in the lamp. The voltage output at pin E is near −10v.

When the input drops to −6v (−T level), T4 becomes forward-biased on and appears as a low resistance in parallel with the 1K resistor. The output at pin E increases to 0v and 35 to 45ma flows through the transistor to give a visual indication within the lamp.

Application

Twisted pair cables are used to connect the driver to the indicator panels. The voltage reference twists are grounded at the driver end and are commoned and decoupled to −6v at the indicator panel as shown above. This circuit is capable of driving an indicator located a maximum of 60 feet from the driver. Two indicator drivers may be driven from one CTDL block.



KB-- 371558

Input Level		Output Level		Delays (usec)			
Min.	Max.	Min.	Max.		Load	2 ROD	10 CTDL Blocks
-5.6 to -6.4	-3.0 to -7.1	1.44 to -0.74	-3.2 to -3.0	Turn On	Min.	.22	.13
					Max.	.40	.15
				Turn Off	Min.	.23	.12
					Max.	.35	.16

CM to CTDL Power Inverter

This card consists of two power inverter circuits used for powering and converting a current mode P line input to an out-of-phase CTDL T line output. Each circuit on the card has an inverter controlling a complementary emitter follower. The input circuit is normally driven by current mode timing rings, or from current mode outputs available from CTDL circuitry. The power inverter outputs drive CTDL N blocks and shift register read-out drivers.

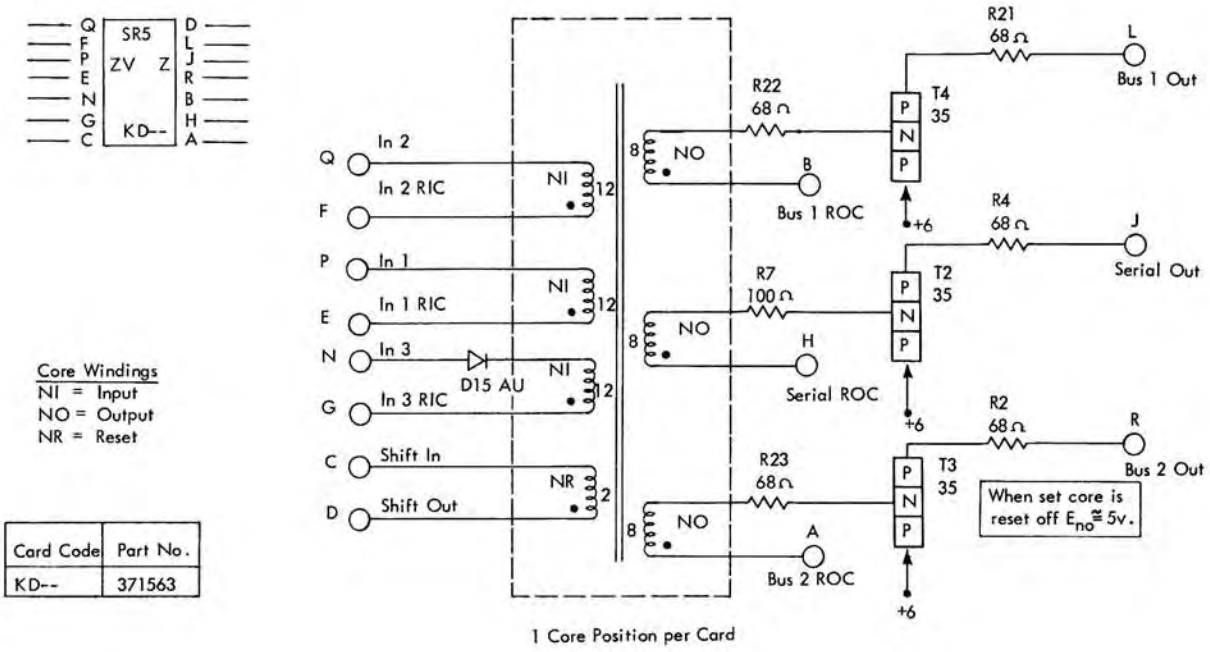
Circuit Description

Assume that the power inverter is driving into the CTDL block as shown above. T4 is on and T5 and T6 are off. The emitter of T6 is at −6v. With a −P input at pin A, T6 is reverse-biased off. The collector voltage of T6 attempts to go to +30v but is clamped to near +3v by conduction from the divider network and D20, to the 8.2K resistor to +30v. T4 is forward-biased on and T5 is reverse-biased off. Line capacity quickly charges and the output at pin B is a usable +T output.

When a +P input appears at pin A, T6 is forward-biased on. The collector voltage of T6 attempts to go to −6v but is clamped to near −3v by conduction through D19 to the divider network. T4 is reverse-biased off and T5 is forward-biased on. Conduction through T5 quickly discharges the line capacity and decreases the voltage at pin B to −3.3v. Use of the complementary emitter followers results in an output signal having sharp rise and fall characteristics.

Application

Maximum DC loading for this power inverter circuit is noted in the logic application illustrated above.



Magnetic Core Shift Register (Significant Digit Detection)

The KD - - card consists of a single magnetic core position used in circuits to detect the high-order significant digit of a magnetic core shift register. Each core position contains three input windings, three output windings, and a reset or read-out winding. The isolation diodes are removed from input windings 1 and 2, to permit their use in the significant digit detection circuits. Magnetic core operation is essentially the same as for other shift register cards. The three outputs from this card are used to charge capacitor storage networks.

Circuit Description

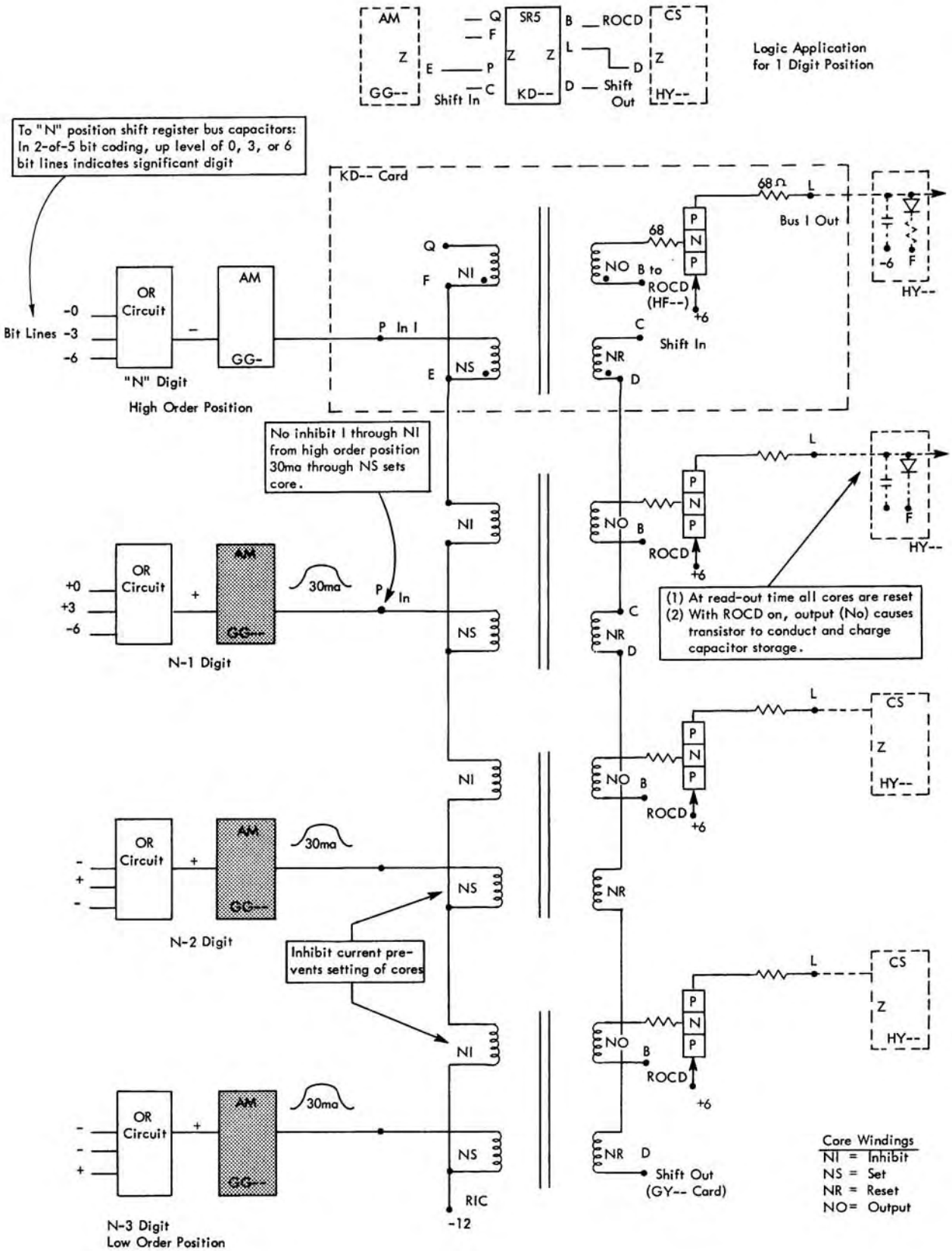
Figure KD-1 illustrates a typical application of the SR5 card. The figure shows several SR5 cards combined to form a circuit that determines which position of an N digit shift register contains the high-order significant digit. The digits from the capacitor bus lines are coded in the 2-of-5 bit code, with a zero being represented by a 1 bit and a 2 bit. Sampling the 0, 3 and 6 bit bus lines by an OR circuit indicates the presence of a significant digit and causes current to flow in the set input windings.

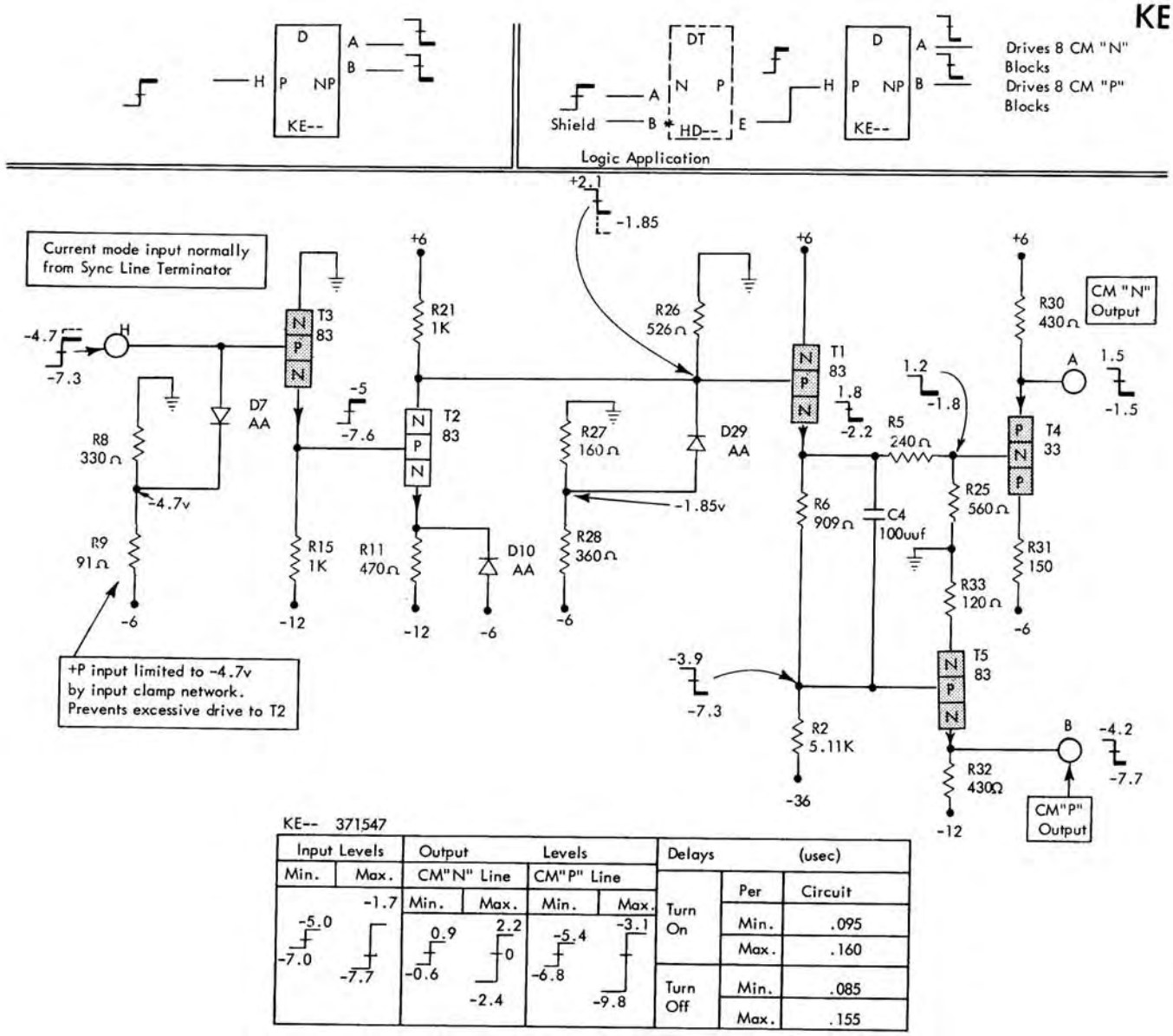
Assume the conditions as noted in Figure KD-1. The high-order digit position (N) of the shift register driving into the OR circuit contains a zero (1 bit and 2 bit only) and the remaining lower-order digit positions all contain significant digits (indicated by the plus entries to their respective OR circuits). When the outputs of the OR circuits are sampled, the sense amplifiers for the N-1, N-2 and N-3 digit positions are gated on and 30ma of current flows through their respective SR5 set windings (Ns) and the inhibit windings (Ni) to the −12v supply. The core for the high-order digit position (N) is not set, because a significant digit was not sensed and current does not flow through its set winding. The core for the N-1 digit position is set on because 30ma of current flows through its set winding (no current through its inhibit winding). Although the N-2 and N-3 cores also have 30ma through their set windings, they also have current flow through their respective inhibit windings that prevents the cores from being set on.

Thus, only the core for the N-1 position is set on and indicates that this is the high-order significant digit in the register. On the next read-out cycle, all the cores are reset off by a constant current pulse from a read-out driver and approximately 5v is induced in the output winding (No) of the N-1 digit core position, because of the switching of its core. At this time, the read-out control driver (ROCD) would be on (+6.5v), and would permit the transistor (TX) to be forward-biased on. This provides sufficient current to charge the bus capacitor storage for that position.

The total current through any one inhibit winding is a function of the number of significant digits sensed in the higher order positions.

For additional information on basic magnetic core shift register operation, refer to the FX - - card.


AM
Z
GG--
E
P
C
Shift In
Q
F
SR5
Z
Z
KD--
B
ROCD
L
D
Shift Out
CS
Z
HY--
Logic Application for 1 Digit Position
To "N" position shift register bus capacitors: In 2-of-5 bit coding, up level of 0, 3, or 6 bit lines indicates significant digit
KD-- Card
Bit Lines -0 -3 -6
OR Circuit
AM
GG-
"N" Digit
High Order Position
P In 1
NI
NS
Q
F
E
68 Ω
L
Bus 1 Out
68
P
N
P
NO
B to ROCD (HF--)
+6
C
Shift In
NR
D
-6
F
HY--
No inhibit I through NI from high order position 30ma through NS sets core.
+0 +3 -6
+
30ma
P In
N-1 Digit
ROCD
(1) At read-out time all cores are reset
(2) With ROCD on, output (No) causes transistor to conduct and charge capacitor storage.
- + -
N-2 Digit
Inhibit current prevents setting of cores
- - +
N-3 Digit
Low Order Position
RIC
-12
Shift Out
(GY-- Card)
Core Windings
NI = Inhibit
NS = Set
NR = Reset
NO = Output



KE-- 371547

Input Levels		Output Levels				Delays (usec)		
Min.	Max.	CM"N" Line		CM"P" Line			Per	Circuit
	-1.7	Min.	Max.	Min.	Max.	Turn On	Min.	.095
-5.0 / -7.0		0.9 / -0.6	2.2 / 0 / -2.4	-5.4 / -6.8	-3.1 / -9.8		Max.	.160
	-7.7					Turn Off	Min.	.085
							Max.	.155

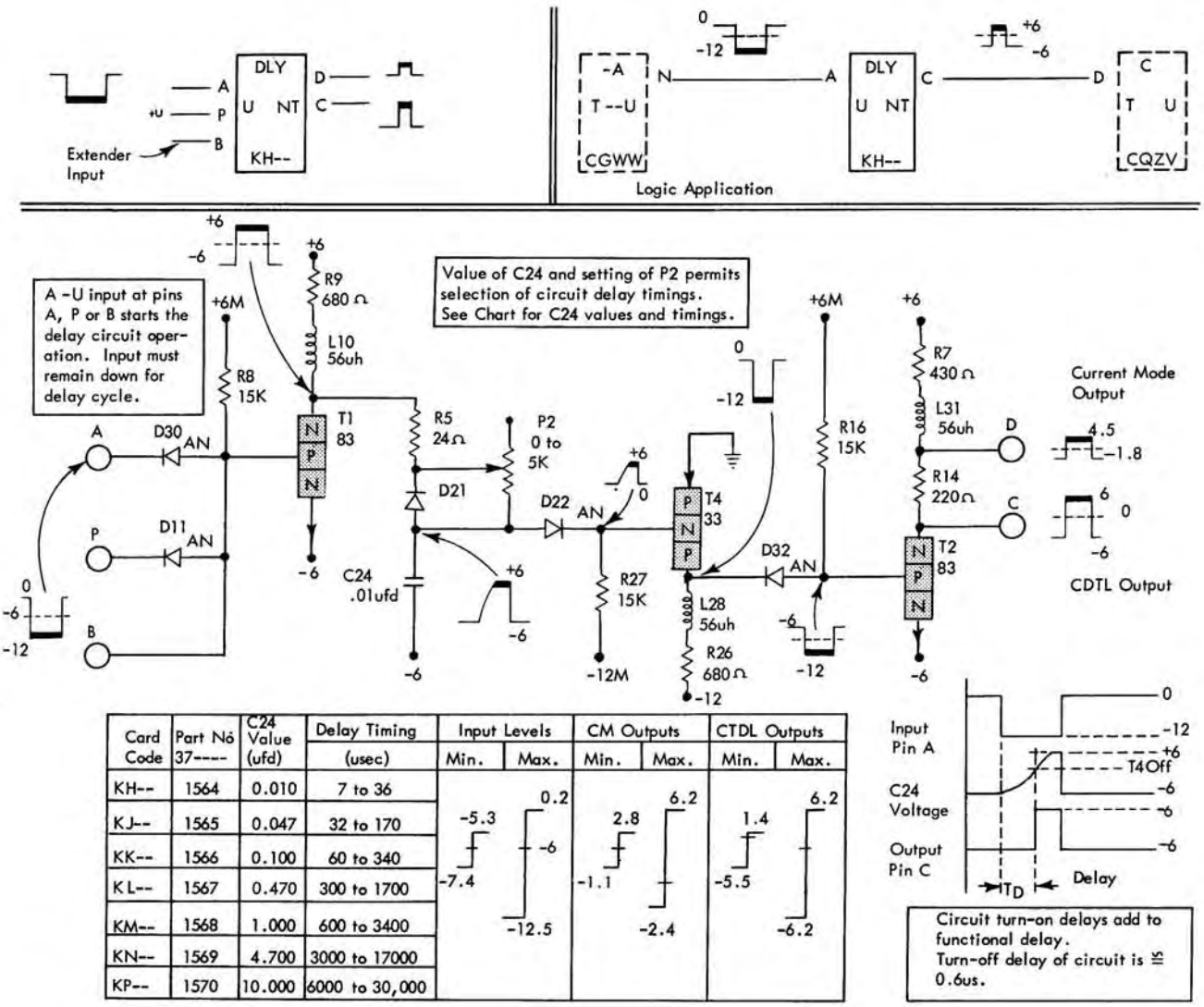
Current Mode P and N Driver

This special power driver was designed for operation as a current amplifier and dual line converter. The driver input is normally a 500kc current mode P line from a sync line terminator. Both P and N line out-of-phase outputs are available for driving into current mode blocks. These outputs are normally used to drive bi-polar timing rings. Each output is capable of driving eight current mode blocks.

Circuit Description

With a −P input at pin H, sufficient current flows through T3 to set the base voltage of T2 to −7.6v. The emitter of T2 is held at −6v by the current flow through R11 and D10. T2 is reverse-biased off and its collector voltage is limited to +2.1v by the divider action of R26 and R21 to +6v. This divider network prevents excessive drive to the base of T1. The emitter follower output T1 sets the base of T4 to +1.2v. Current flow through T4 provides a +N output at pin A. With the emitter of T1 at 1.8v, current flow through R2, R6, and T1 sets the base of T5 to −3.9v. Emitter follower action of T5 provides a +P output at pin B.

When a +P level is applied to pin H, the current flow increases through T3 and raises the base level of T2 to −5.0v. The input clamping network (D7 to R8 and R9) limits the +P input swing to −4.7v and prevents excessive drive into T2. Inverter T2 becomes forward-biased on and its collector voltage drops toward −6v but is clamped at −1.8v by D29, R27, and R28. The clamping action prevents T2 from operating in saturation and results in faster turn-off time of T2. The clamping action also limits the drive to T1. Current flow through T1 decreases and its emitter voltage drops to −2.2v. Divider R5 and R25 to ground set the base level of T4 to −1.8v. This increases the current flow through the transistor (T4) and provides a −N level output at pin A. Divider R2 and R6 set the base of T5 to −7.3v. Emitter follower action of T5 gives a −P level output at pin B.



Card Code	Part Nó 37----	C24 Value (ufd)	Delay Timing (usec)	Input Levels Min.	Input Levels Max.	CM Outputs Min.	CM Outputs Max.	CTDL Outputs Min.	CTDL Outputs Max.
KH--	1564	0.010	7 to 36	-5.3 / -7.4	0.2 / -6 / -12.5	2.8 / -1.1	6.2 / -2.4	1.4 / -5.5	6.2 / -6.2
KJ--	1565	0.047	32 to 170						
KK--	1566	0.100	60 to 340						
KL--	1567	0.470	300 to 1700						
KM--	1568	1.000	600 to 3400						
KN--	1569	4.700	3000 to 17000						
KP--	1570	10.000	6000 to 30,000						

CTDL Delay Circuit

The KH - - delay card provides an output pulse 7 to 36μs after the start of the input pulse. There is one delay circuit on each card that is controlled by an RC network. A 5K potentiometer is varied to obtain a desired delay within the 7 to 36μs range.

A −U level at any of the input pins starts the delay timing and provides out-of-phase N and T line outputs. The output duration is a function of the input signal and the circuit variables. This circuit is self-recycling, but requires a definite off period to insure the discharging of the timing capacitor (C24).

Circuit Description

Assume all inputs are in the up level, and T1, T4 and T2 are forward-biased and conducting. The CTDL output at pin C is near the −6v emitter potential of T2. C24, the timing capacitor, is discharged to −6v through T1, R5, and the forward-biased D21.

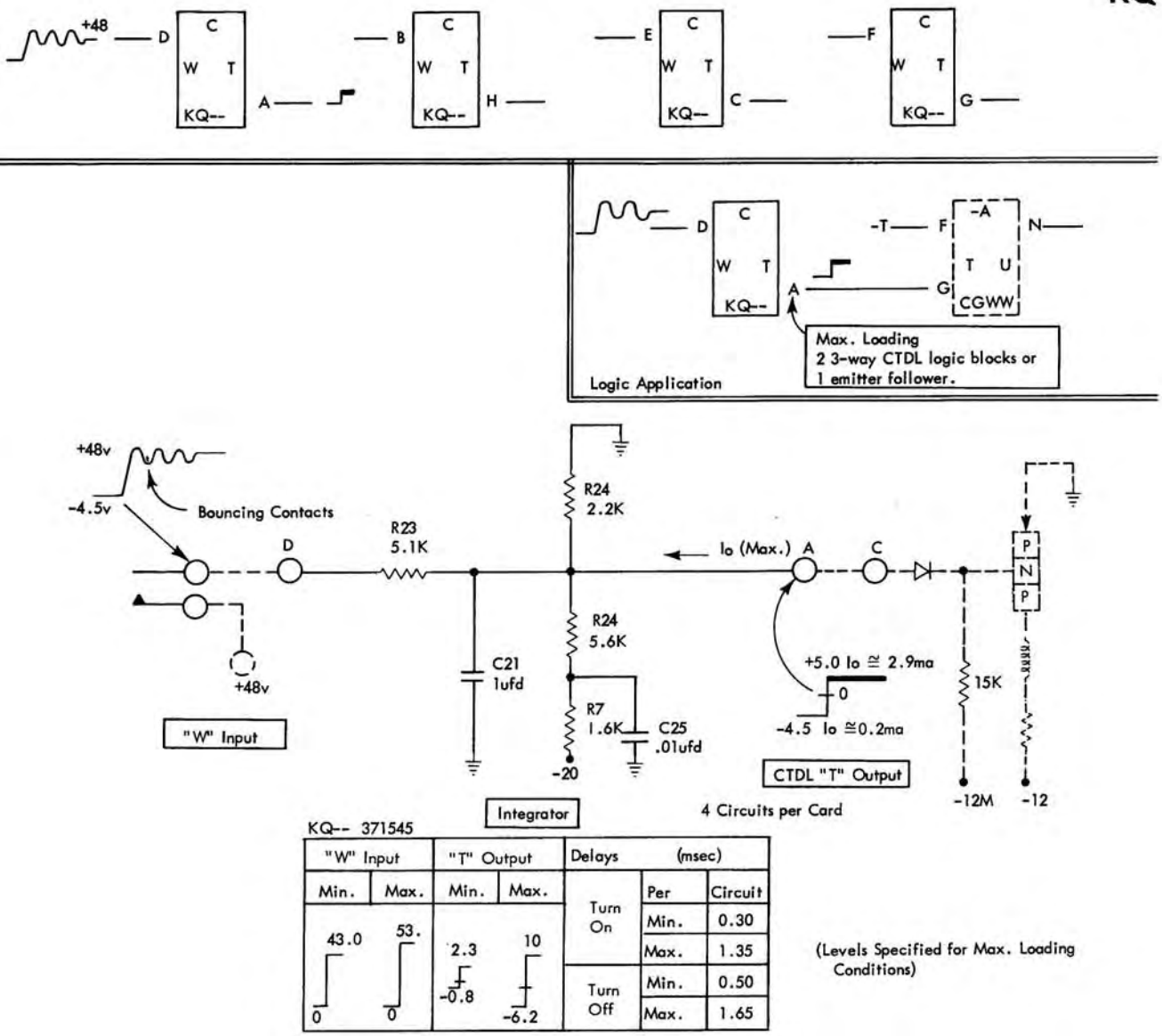
When a −U level appears at pin A, T1 is reverse-biased off. The collector voltage of T1 increases to +6v. D21 is no longer forward-biased, so C24 must now charge through the 5K potentiometer, R2 and R5 toward the +6v collector supply. T4 remains in conduction until the charge on C24 is positive enough to reverse-bias T4. When T4 is turned off, its collector voltage drops to −12v and cuts off T2. The collector output of T2 increases to +6v. This +T output (pin C) remains up until all inputs again are at the +U level. The RC charging time thus controls the cut-off time of T4 and delays the start of the positive output swing for the desired time interval.

Repetition Rate

The input must remain in the up level long enough to insure that the timing capacitor is fully discharged (approximately 1.3 to 1.6 times the circuit delay).

Application

Seven CTDL delay cards with various capacitor sizes provide continuous delay timings (with good overlap) from 7.0 to 30,000μs. The range of delay timings available and the value of C24 used for the various delay cards are noted in the chart.



KQ-- 371545

"W" Input		"T" Output		Delays (msec)		
Min.	Max.	Min.	Max.		Per	Circuit
43.0	53.	2.3	10	Turn On	Min.	0.30
0	0	-0.8	-6.2		Max.	1.35
				Turn Off	Min.	0.50
					Max.	1.65

(Levels Specified for Max. Loading Conditions)

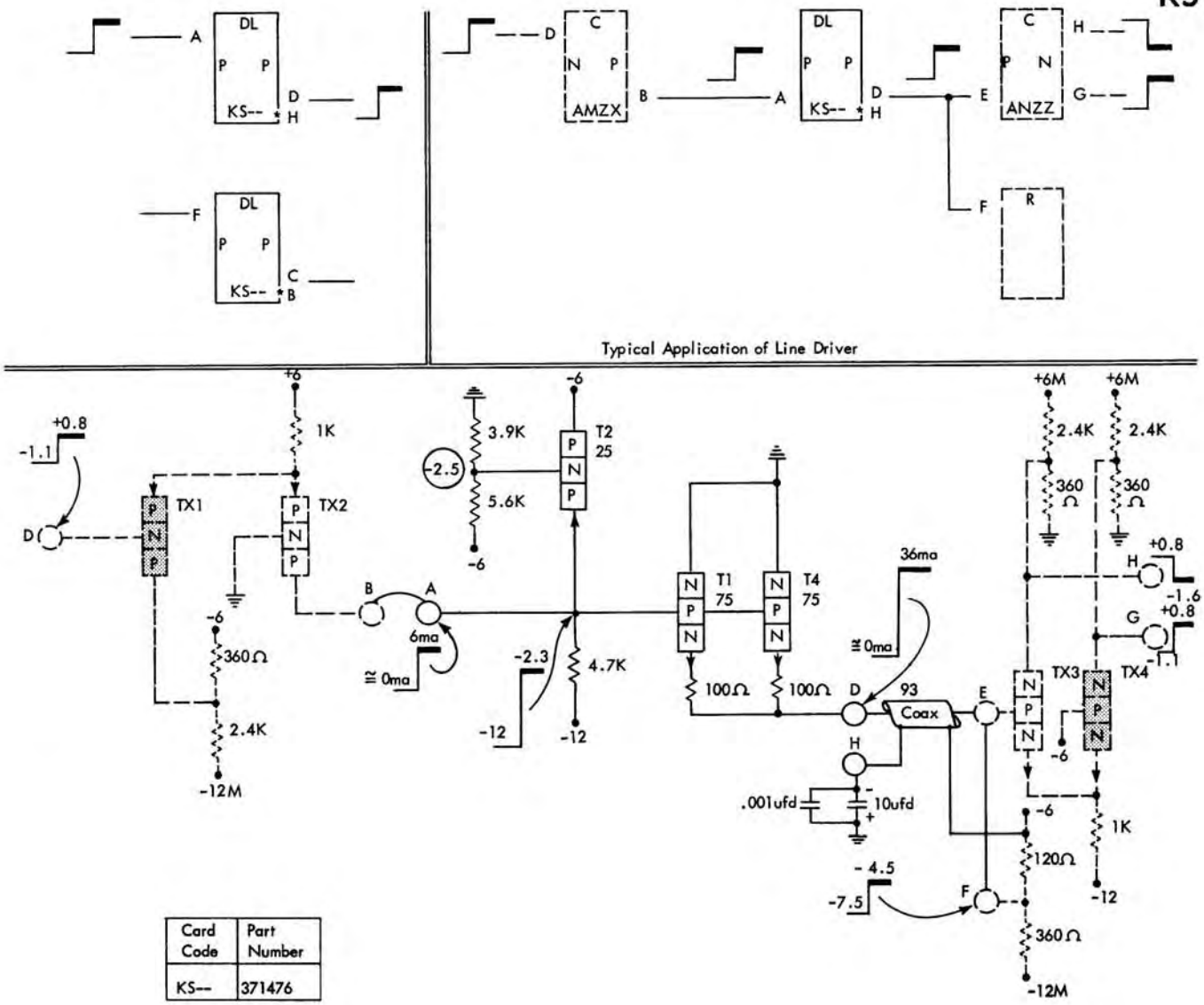
Converter W to T Line

The KQ - - card consists of four relay-to-CTDL integrator circuits. Each circuit converts a W line (+48v) input from the normally open contacts of a relay to a CTDL T line output. The T line output normally drives into CTDL N-type logic blocks.

Circuit Description

Assume that the integrator circuit is connected as shown above. When the relay is down and the N/O contact points are open, current flow from the −20v supply plus the slight load current (I_o) through the integrator divider network sets the output at pin A to −4.5v. When the relay is energized and the N/O contacts close, +48v is applied to pin D. Current flow from the load and the integrator network gives an output at pin A of +5.0v. C21 filters the oscillating input caused by the bouncing of the contact points when they are first made. External loading conditions affect the output voltage levels at pin A.

The integrator turn-on delays were measured from the time the relay was picked until the output of the integrator crosses the 0v reference. The turn-off delays were measured from the time the relay points opened until the output of the integrator crossed the 0v reference level.



Card Code	Part Number
KS--	371476

Current Mode, P-to-P Line Driver

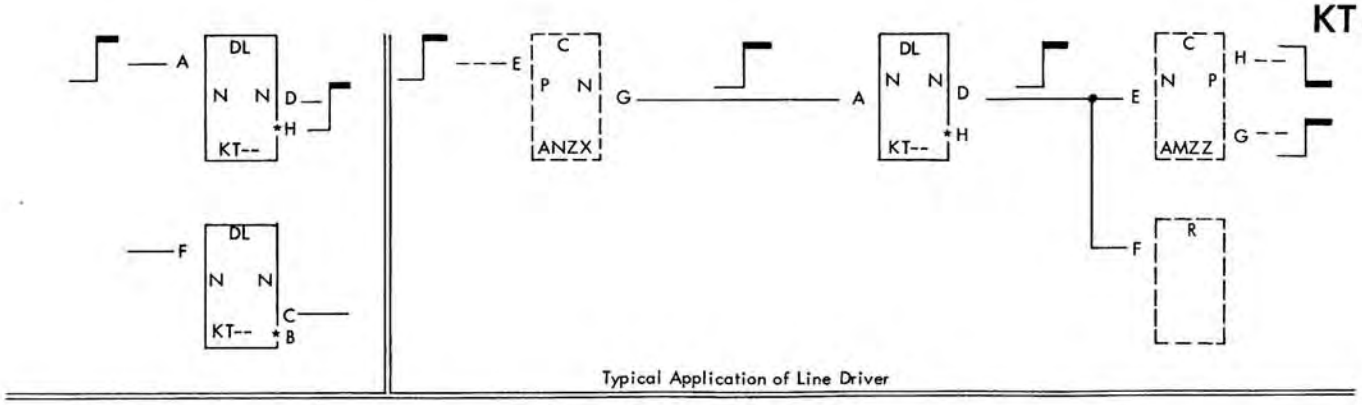
The line driver couples information between two widely separated points over a 93 ohm coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive up to ten circuits dispersed at random distances along the coaxial line. Line levels are established by the coupling network which terminates the line. Considering these line levels, the driver develops an in-phase P line output for a P line input.

Circuit Description

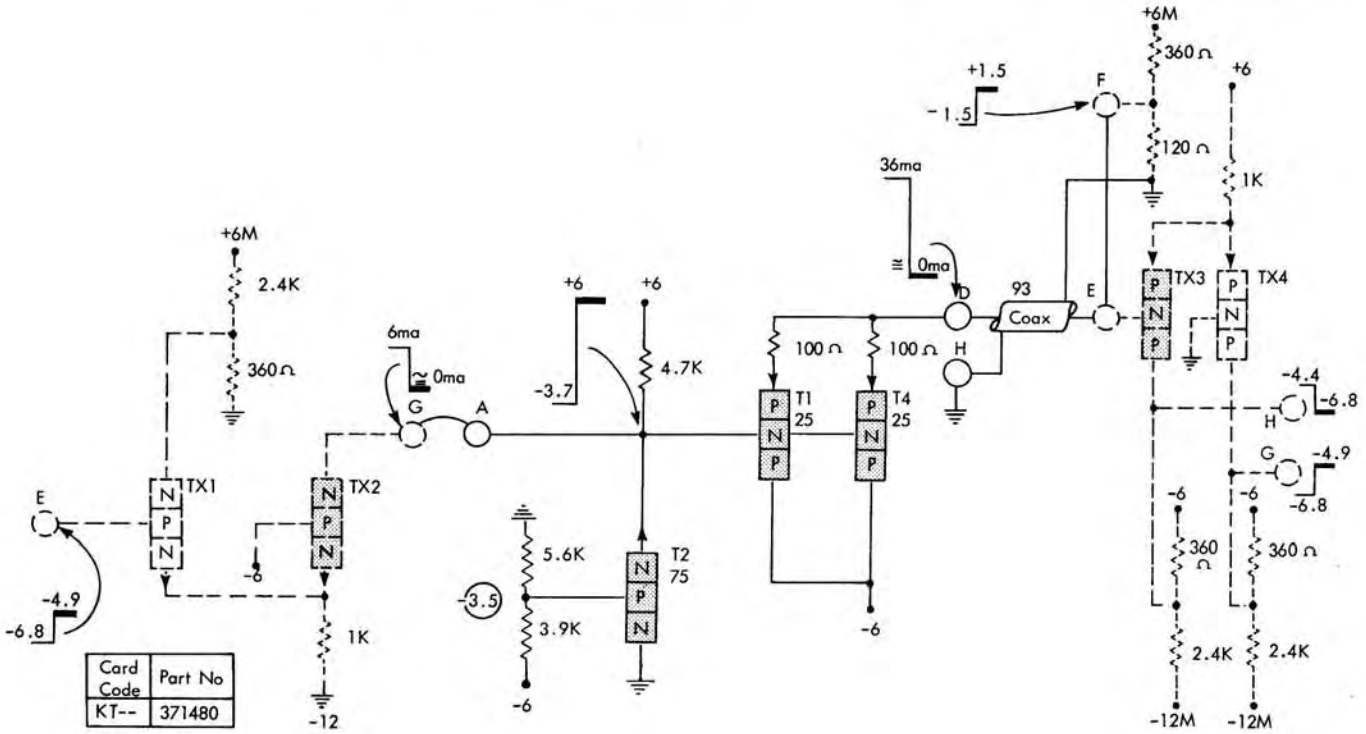
As shown, TX2 is cut off and the input current to the line driver is zero. T1, T4, and T2 are reverse-biased. The output of the coaxial line is at a −P level of −7.5v because of divider current through the 120 ohm, 360 ohm coupling network.

When the input signal to the converter rises, TX2 is forward-biased and 6ma flows out of the driver through TX2 to +6v. The sequence which results when input current increases from zero to 6ma is as follows. As input current increases from zero, the current flow from −12v through the 4.7K resistor increases and the voltage drop across this resistor increases. When current increases to 1ma, the base potential of T1 and T4 rises above −7.5v which forward-biases T1 and T4.

Base current for these transistors flows out of the 120 ohm, 360 ohm coupling network, through the emitter-base diodes and TX2 to +6v. When the current flow through the 4.7K resistor increases to 2.1ma the emitter of T2 rises above −2.5v and T2 is forward-biased. Its emitter clamps to its base potential and current flows from −6v, through T2, and TX2 to +6v. The 6ma current flow through TX2 has three components (current from −12v through the 4.7K resistor, Ib of T1 and T4, and Ice of T2). T2 functions as a clamp circuit; it sets the base voltage of T1 and T4 at −2.3v over a range of input current. In this state, a nominal current of 36ma flows out of the coupling network and the load, through T1 and T4 to ground. The output of the coaxial line rises to a +P level of −4.5v because of this current flow. The 100 ohm emitter resistors provide degeneration so currents through T1 and T4 tend to divide equally.



Typical Application of Line Driver



Card Code	Part No
KT--	371480

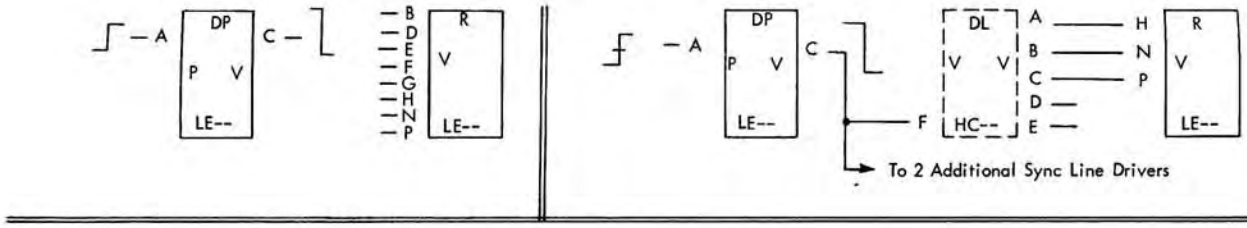
Current Mode, N-to-N Line Driver

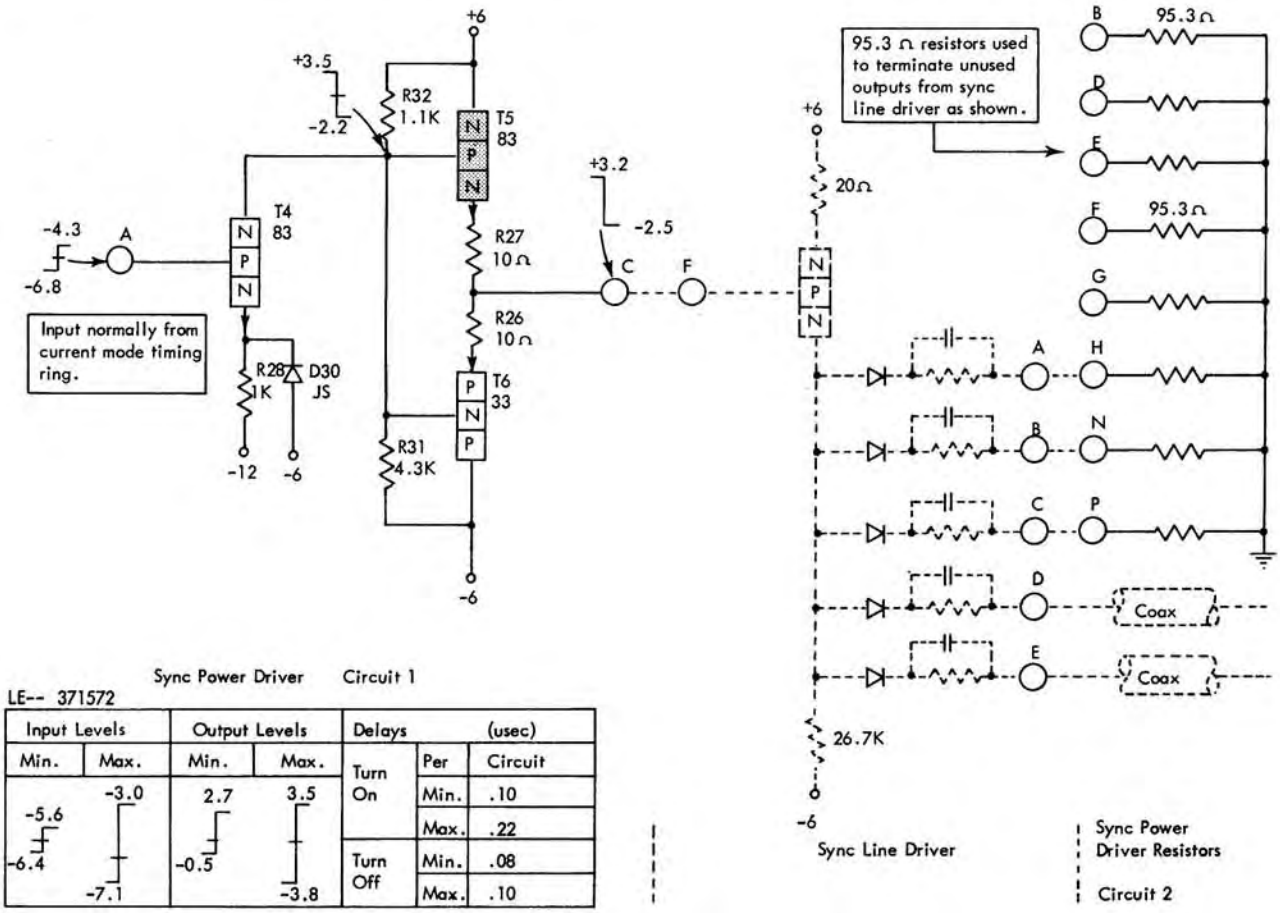
The line driver couples information between two widely separated points over a 93 ohm coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive up to ten circuits dispersed along the coaxial line. Line levels are established by the coupling network which terminates the line. Considering these levels, the driver develops an in-phase N line output for an N line input.

Circuit Description

In the state shown, TX2 is forward-biased and 6ma flows from −12v through TX2 into the driver. The sequence which results when input current increases from zero to 6ma is as follows. The input current through the 4.7K resistor to +6v is an increasing current which causes the voltage drop across this resistor to also increase. When this current increases to 1ma the base potential of T1 and T4 falls below +1.5v which forward-biases T1 and T4. Base current for T1 and T4 flows from −12v, through TX2 and the base-emitter diodes, into the 120 ohm, 360 ohm coupling network. When current flow through the 4.7K resistor increases to 2.1ma, the emitter of T2 falls below −3.5v and T2 is forward-biased. Its emitter clamps to its base potential and current flows from −12v through TX2 and T2 to ground. The 6ma input current divides into three components (current through the 4.7K resistor to +6v, Ib of T1 and T4 and Ice of T2). T2 functions as a clamp circuit; it sets the base voltage of T1 and T4 at −3.7v over a range of input current. In this state, a nominal current of 36ma flows from −6v through T1 and T4 and into the coupling network which establishes the output of the coaxial line at a −N level of −1.5v. The 100 ohm emitter resistors provide degeneration so currents through T1 and T4 tend to divide equally.

When the input signal to the converter rises, TX2 is cut off and input current falls to zero. T1, T4 and T2 are reverse-biased and the output of the coaxial line rises to a +N level of +1.5v.





Sync Power Driver Circuit 1

LE-- 371572

Input Levels		Output Levels		Delays		(usec)
Min.	Max.	Min.	Max.		Per	Circuit
-5.6 to -6.4	-3.0 to -7.1	2.7 to -0.5	3.5 to -3.8	Turn On	Min.	.10
					Max.	.22
				Turn Off	Min.	.08
					Max.	.10

Sync Power Driver

The LE - - card consists of two circuits, a sync power driver circuit and a resistor coupling network to ground. The eight 95.3 ohm coupling resistors are used to terminate the unused outputs of the sync line driver as shown on the circuit diagram; they maintain the proper impedance matching into the driven cables.

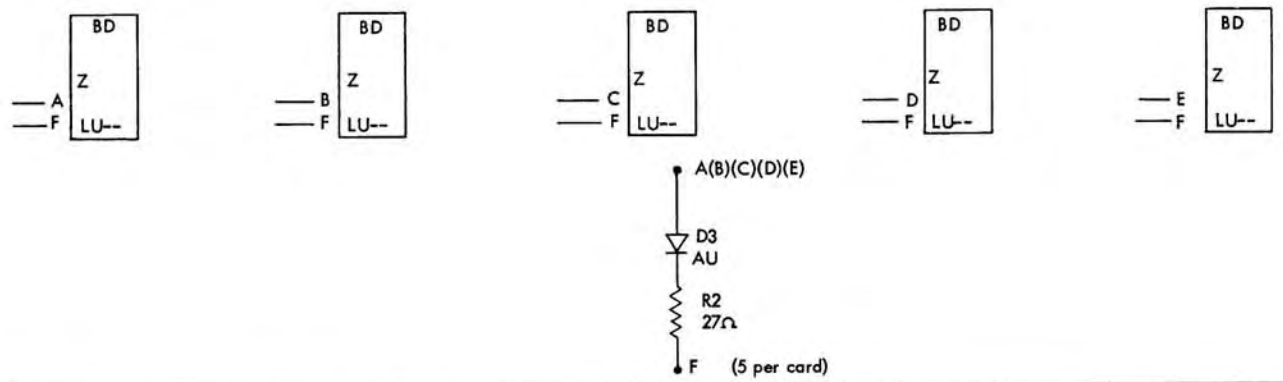
A current mode P line from a 500kc oscillator is the normal input to the sync power driver circuit. The special mode output from this circuit is sufficient to drive three sync line drivers. This circuit functions as a power inverter circuit because a positive input swing results in a negative output swing.

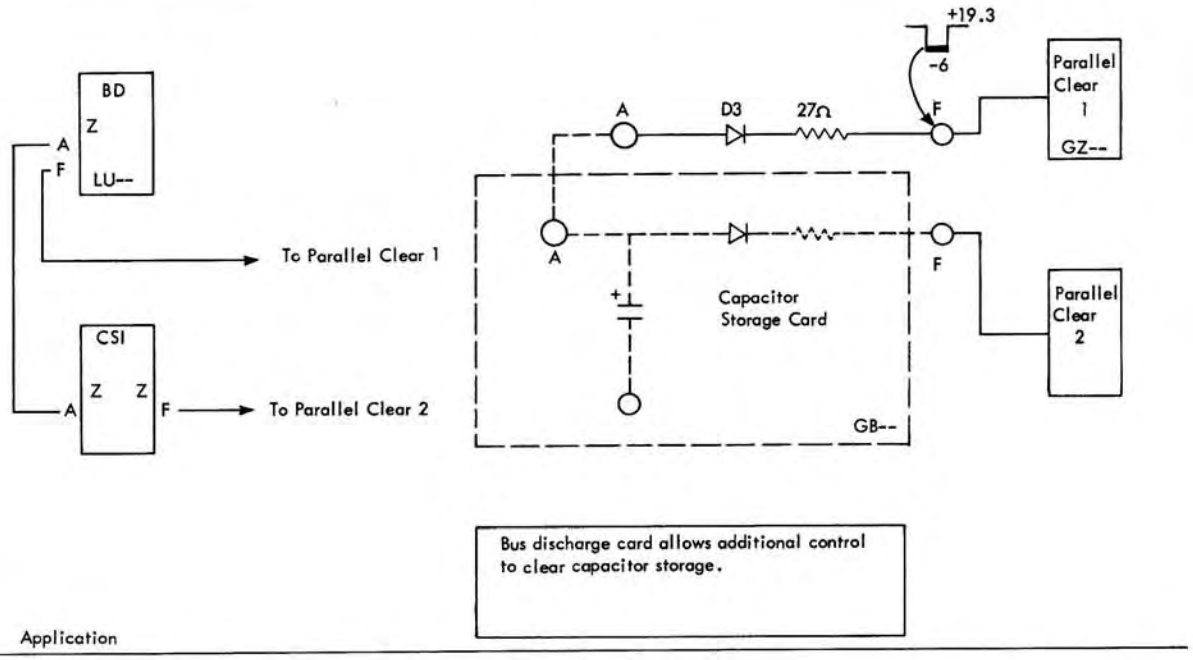
Circuit Description

(Sync Power Driver connected to load as shown.) Assume a starting condition of T6 off and T5 on. Current flow of 6ma through R28 and D30 keeps the emitter of T4 at −6v. A −P input at pin A reverse-biases T4 off. Conduction from the −6v supply, R31 and R32 to +6v, sets the base level of T5 and T6 to near +3.5v. Sufficient current flows from the load through R27 and T5 to +6v, and results in an output at pin C of approximately +3.2v. T6 is reverse-biased off at this time.

When a +P input is applied to pin A, T4 is forward-biased on and switches an additional 6ma of current through R32. The base level of the complementary emitter followers drops to near −2.2v. T5 becomes reverse-biased off and T6 is forward-biased on. Electron flow from the −6v supply, T6, and R26 into the load rapidly decreases the output at pin C to −2.5v. This down level exists until a −P input at pin A turns off T4.

Use of the complementary emitter followers results in sharp rise and fall characteristics of the output waveform controlling the sync line drivers.





Application

Card Code	Part No.
LU--	371575

Bus Discharge Card

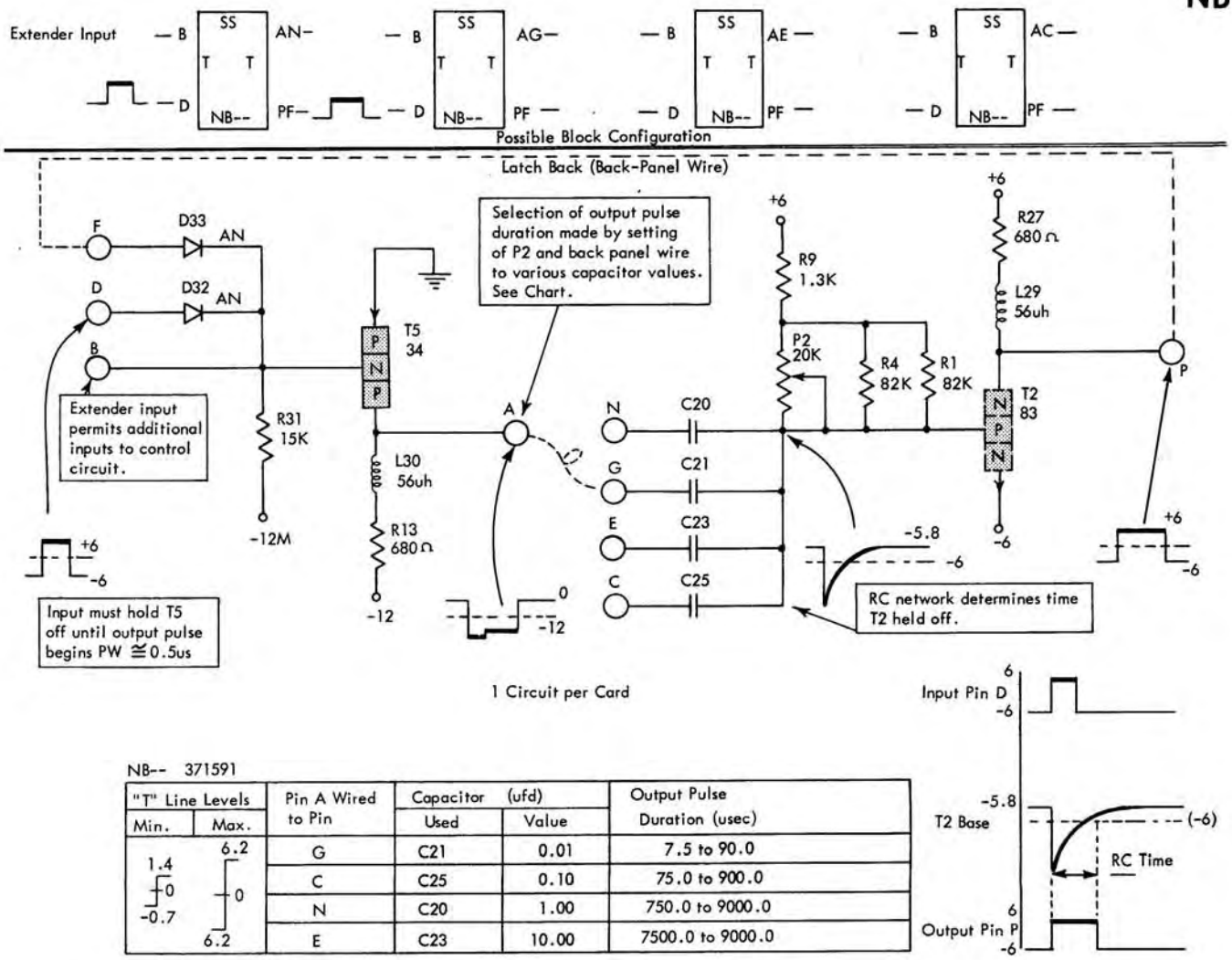
The LU - - card contains five diode-resistor networks, used in magnetic core shift register operations. These networks are used with parallel clear read-in drivers and allow additional circuits to control the discharge of bus capacitor storage units.

Circuit Description

In the application illustrated above, an additional parallel clear circuit and a bus discharge coupling network are wired to a capacitor storage card. When the parallel clear 1 driver is gated on (−6v), conduction through the 27 ohm resistor and D3 to the capacitor quickly discharges the capacitor to −6v. D3 provides isolation from the other driver circuits and R2 serves as a limiting resistor in this application.

Application

This card is used with capacitor storage cards (GB - -, HY - - or HZ - -).



NB-- 371591

"T" Line Levels Min.	"T" Line Levels Max.	Pin A Wired to Pin	Capacitor (ufd) Used	Capacitor (ufd) Value	Output Pulse Duration (usec)
1.4 +0 -0.7	6.2 +0 6.2	G	C21	0.01	7.5 to 90.0
		C	C25	0.10	75.0 to 900.0
		N	C20	1.00	750.0 to 9000.0
		E	C23	10.00	7500.0 to 9000.0

CTDL Single-Shot Trigger Card (T input)

The NB - - card consists of one CTDL single-shot trigger circuit. The triggering action is initiated by the leading edge of a +T input pulse to pin D or to the extender input pin B. The output is a +T signal having a desired pulse width. This circuit is self restoring, in that it is flipped to a certain state by the +T input signal, and then returns to its original status after a predetermined time set by an RC network. The output pulse duration is independent of an input signal except for its start and repetition rate. A definite off period is required between triggering pulses to allow for the discharge of the timing capacitor.

Back-panel wiring to one of the four capacitor values selects the range of the output pulse duration. P2 permits adjustment to a specific output pulse duration within the range selected. A back-panel wire is also required for the "latch back" of the circuit.

Circuit Description

Assume that the circuit is back-panel wired as noted above and that T5 and T2 are forward-biased on. C21 is discharged through the low resistance paths offered by T5 and T2 on.

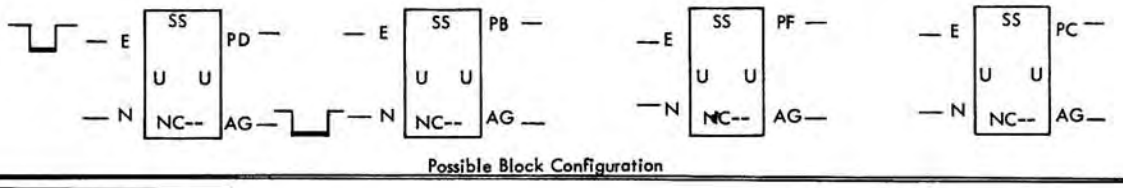
When a +T level is applied to pin D, T5 becomes reverse-biased off. The collector voltage of T5 drops to −12v. Because the voltage across C21 cannot change instantaneously, the sudden negative shift appears across the resistor network and is seen at the base of T2. T2 is reverse-biased off until the charge on C21 increases the base voltage of T2 above −6v. The charge path is through R4, R7, and P2 to R9 and +6v. While T2 is biased off, the +T output at pin P is "latched back" through D33 to hold T5 off for the RC charge time of C21.

When the base voltage of T2 increases to approximately −5.8v, T2 is forward-biased on and the output decreases to −6v. The latch-back circuit through D33 now turns on T5 and quickly discharges C21. A +T output, of a predetermined pulse width, is thus obtained from this circuit.

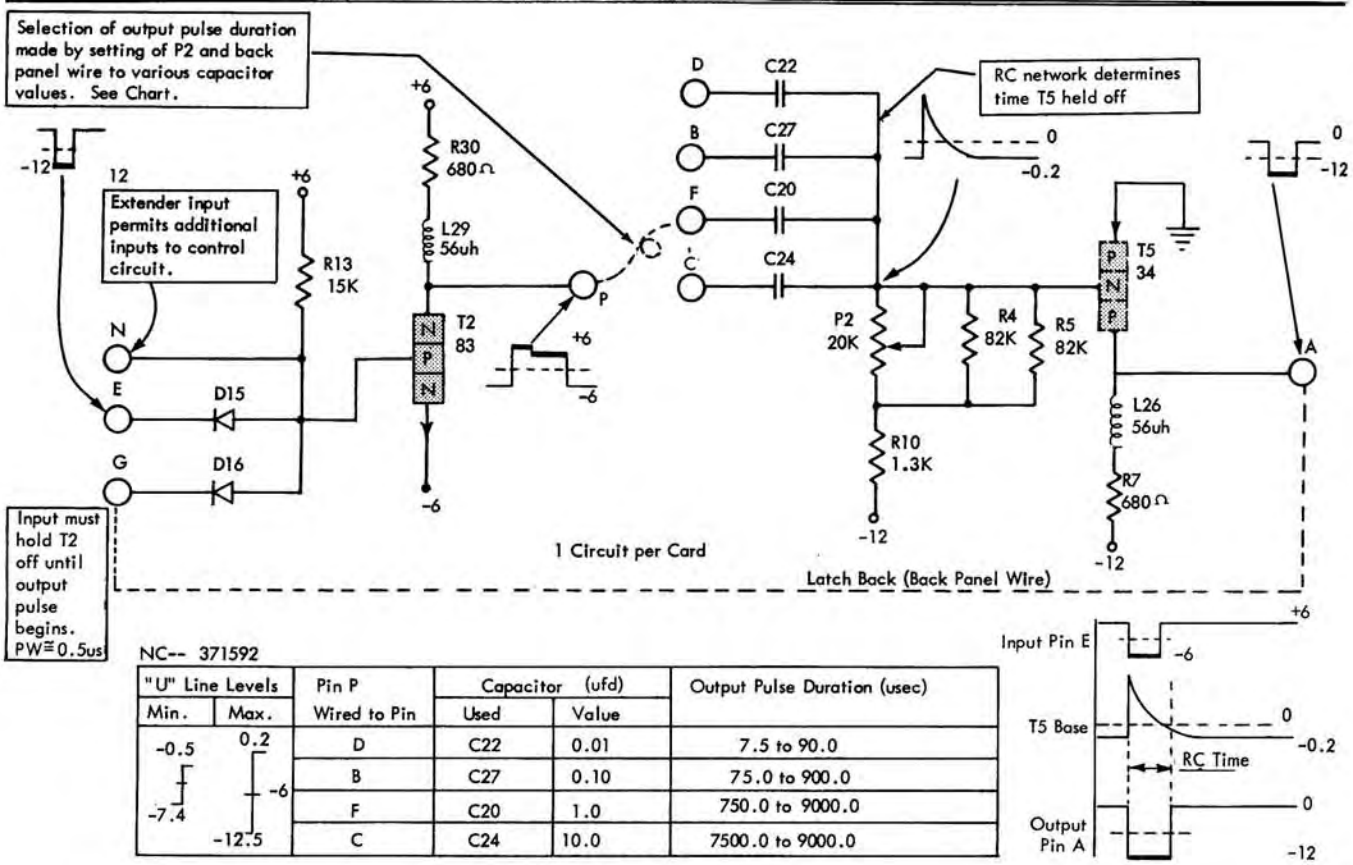
Application

The single-shot trigger card is used in pulse forming circuits, master clock circuits, and delay circuits. It is possible to produce output pulses having a shorter time duration than the input triggering pulse; however, a much poorer fall time of the output signal results.

The chart above relates the back-panel wiring to the various capacitor values used and to the range of the output pulse obtained.



Possible Block Configuration



NC-- 371592

"U" Line Levels		Pin P	Capacitor (ufd)		Output Pulse Duration (usec)
Min.	Max.	Wired to Pin	Used	Value	
-0.5	0.2	D	C22	0.01	7.5 to 90.0
-7.4	-6	B	C27	0.10	75.0 to 900.0
		F	C20	1.0	750.0 to 9000.0
	-12.5	C	C24	10.0	7500.0 to 9000.0

CTDL Single Shot Trigger Circuit (U Input)

The NC-- card consists of one CTDL single-shot trigger circuit. The triggering action is initiated by the leading edge of a −U input pulse to pin E or to the extender pin N. The output is a −U signal having a desired pulse width. This circuit is self-restoring in that it is flipped to a certain state by the −U input signal, and then returns to its original status after a predetermined time set by an RC network. The output pulse duration is independent of the input signal except for its start and repetition rate. A definite off period is required between triggering pulses to allow for the discharge of the timing capacitor. Back-panel wiring to one of four capacitor values selects the range of the output pulse duration. P2 permits adjustment to a specific output pulse duration within the range selected. A back-panel wire is also required for the "latch back" of the circuit.

Circuit Description

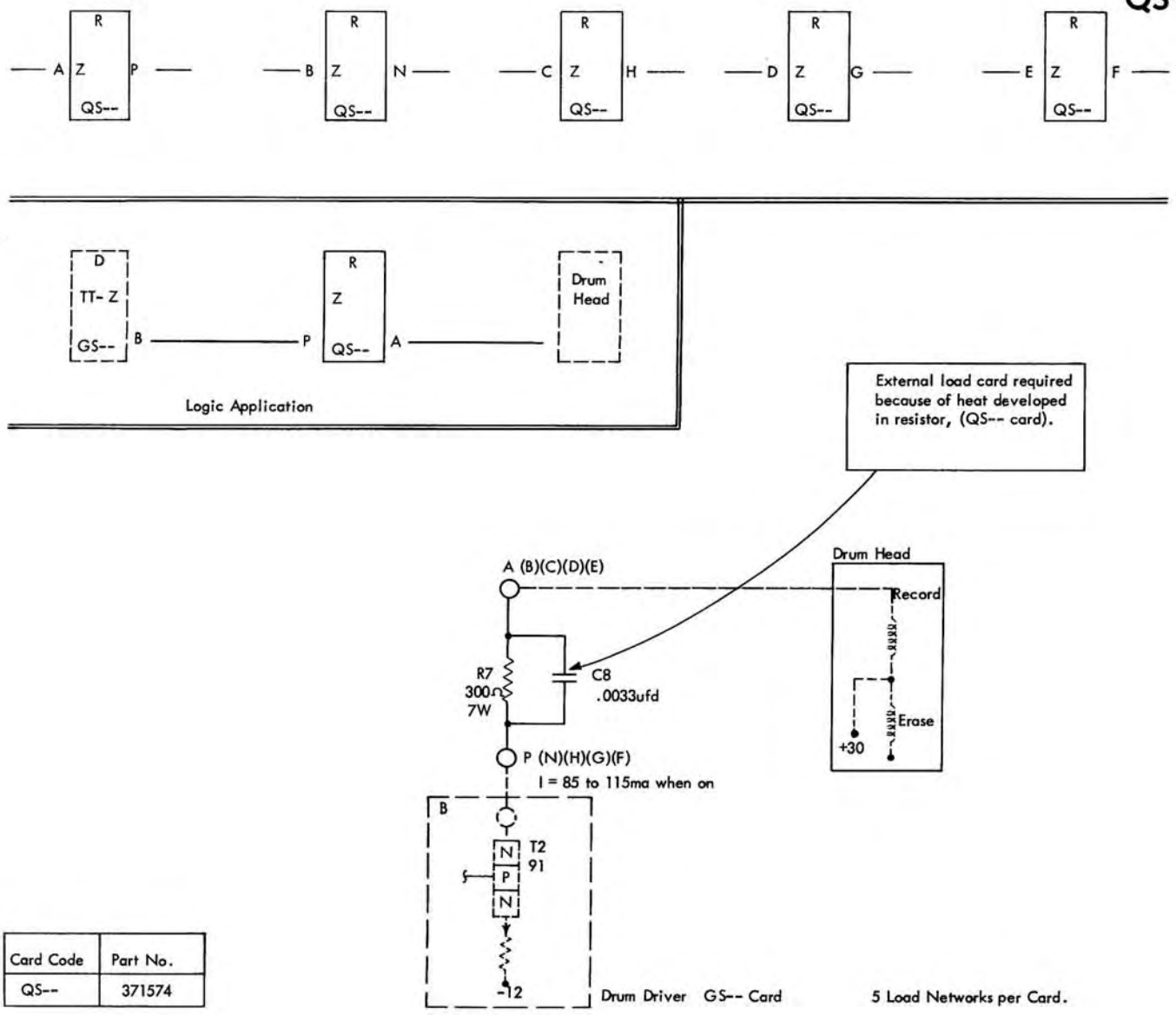
Assume that the circuit is back-panel wired as noted above and that T2 and T5 are forward-biased on. C20 is discharged through the low resistance paths offered by T2 and T5 on.

When a −U level is applied to pin E, T2 becomes reverse-biased off. The collector voltage of T2 increases to +6 volts. Because the voltage across C20 cannot change instantaneously, the sudden positive shift appears across the resistor network and is seen at the base of T5. T5 is reverse-biased off until the charge on C20 decreases the base voltage of T5 below ground potential. The charge path is through R4, R7 and P2 to R10 and −12v. While T5 is biased off, the −U output at pin A is "latched" back through D16 to keep T2 off for the RC charge time of C20.

When the base voltage of T5 decreases to approximately −0.2v, T5 is forward-biased on and the output is increased to 0v. The latch-back circuit through D16 turns on T2 and quickly discharges C20. A −U output of a predetermined pulse width is thus obtained from this circuit.

Application

The single-shot trigger card is used in pulse forming circuits, master clock circuits and delay circuits. It is possible to produce output pulses having a shorter time duration than the triggering pulse; however, a much poorer fall time of the output pulse results. The chart relates the back-panel wiring to the various capacitor values used and to the range of the output pulse obtained.



Card Code	Part No.
QS--	371574

Drum Load Card

The QS - - card contains five resistor-capacitor networks designed especially for use with the drum driver card (GS - -). These networks provide the proper load for the drum driver when writing or erasing information on a magnetic drum. An external load card was required for this application because of the excessive heat developed in the 300 ohm resistor and power transistor.

C8 acts as a low impedance to the current pulse when the power transistor is first turned on and results in sharp rise characteristics of the output current waveform.

Application

A typical application for the drum load card is shown above.

Appendix A. SMS Card Index by Function

Function	Sym-bol	Card Code	Ckts per Card	Inputs per Ckt	Internal Loading per Card	Application Notes
1. CURRENT MODE BASIC LOGIC						
Logic	+A	AA--	2	2	None	
		ZU	2	2	Out Ø	
		ZV	2	2	In Ø	
		ZW	2	2	All	
		ACYX	1	3	None	
		YY	1	3	Out Ø	
		YZ	1	3	In Ø	
		ZA	1	3	All	
		ACZF	1	4	None	
		ZG	1	4	Out Ø	
		ZH	1	4	In Ø	
		ZJ	1	4	All	
	+O	AB--	2	2	None	
		ZU	2	2	Out Ø	
		ZV	2	2	In Ø	
		ZW	2	2	All	
		ADYX	1	3	None	
		YY	1	3	Out Ø	
		YZ	1	3	In Ø	
		ZA	1	3	All	
		ADZF	1	4	None	
		ZG	1	4	Out Ø	
		ZH	1	4	In Ø	
		ZJ	1	4	All	
Extenders	E	ACYV	1	4		Extends N Blocks
		YW	1	2		
		ADYV	1	4		Extends P Blocks
		YW	1	2		
Converters	C	AMZX	2	1	None	
		ZY	2	1	Out Ø	N to P
		ZZ	2	1	In Ø	
		--	2	1	All	
		ANZX	2	1	None	
		ZY	2	1	Out Ø	P to N
		ZZ	2	1	In Ø	
		--	2	1	All	
		AQ--	4	1	All	CM to VM
2. CTDL BASIC LOGIC						
Logic	+A	CK--	2	3	0	
		VU	2	3	1	
		WV	2	3	2	
		YC	2	3	2	Additional Extender
		CH--	3	2	0	
		VV	3	2	1	
		VW	3	2	2	
		WW	3	2	3	
Logic	-A	CJ--	2	3	0	
		VU	2	3	1	
		WV	2	3	2	
		YC	2	3	2	Additional Extender
		CG--	3	2	0	
		VV	3	2	1	
		VW	3	2	2	
		WW	3	2	3	
		JG--	3	2	0	
		VV	3	2	1	High Speed
		VW	3	2	2	
		WW	3	2	3	
		JH--	2	3	0	
		VU	2	3	1	High Speed
		WV	2	3	2	
Extender	E	CLVQ	3			
		VR	4			See Card for Application Data
		VS	3			
		VT	4			
Converters	C	CQ--	4	1	0	
		YG	4	1	1	T to U
		ZT	4	1	2	
		ZV	4	1	4	
		CR--	4	1	0	U to T
		YG	4	1	1	
Converters	C	CRZT	4	1	2	U to T
		ZV	4	1	4	
		JF--	4	1	0	
		VA	4	1	1	T to U
		VN	4	1	2	
		VP	4	1	4	High Speed
		JJ--	4	1	0	
		VA	4	1	1	U to T
		VN	4	1	2	
		VP	4	1	4	High Speed
3. DIFFUSED JUNCTION BASIC LOGIC						
Logic	+A	DEZJ	1	4	All	
		ZH	1	4	In Ø	
		ZG	1	4	Out Ø	Type B
		ZF	1	4	None	
		DEZA	1	3	All	
		YZ	1	3	In Ø	
		YY	1	3	Out Ø	Type B
		YX	1	3	None	
		DBZW	2	2	All	
		ZV	2	2	In Ø	
		ZU	2	2	Out Ø	
		ZT	2	2	None	No Out Ø Load
		YD	2	2	All	on 2nd Ckt
		DEZN	1	4	All	
		ZL	1	4	Out Ø	Type A
		DEZE	1	3	All	
		ZC	1	3	Out Ø	Type A
		DAZW	2	2	All	
		ZU	2	2	Out Ø	Type A
	+O	DFZJ	1	4	All	
		ZH	1	4	In Ø	
		ZG	1	4	Out Ø	Type B
		ZF	1	4	None	
		DFZA	1	3	All	
		YZ	1	3	In Ø	
		YY	1	3	Out Ø	Type B
		YX	1	3	None	
		DDZW	2	2	All	
		ZV	2	2	In Ø	
		ZU	2	2	Out Ø	Type B
		ZT	2	2	None	
		DFZN	1	4	All	
		ZL	1	4	Out Ø	Type A
		DFZE	1	3	All	
		ZC	1	3	Out Ø	Type A
		DCZW	2	2	All	
		ZU	2	2	Out Ø	Type A
Exclusive Or	+OE	DBZS	1	4	All	
		ZR	1	4	In Ø	
		ZQ	1	4	Out Ø	
		ZP	1	4	None	
	-OE	DDZS	1	4	All	
		ZR	1	4	In Ø	
		ZQ	1	4	Out Ø	
		ZP	1	4	None	
Converters	C	DBZZ	2	1	All	
		ZY	2	1	In Ø	Type B (N to P)
		ZX	2	1	Out Ø	
		--	2	1	None	
		DAZZ	2	1	All	
		ZX	2	1	Out Ø	Type A (N to P)
		DDZZ	2	1	All	
		ZY	2	1	In Ø	
		ZX	2	1	Out Ø	Type B (P to N)
		--	2	1	None	
		DCZZ	2	1	All	
		ZX	2	1	Out Ø	Type A (P to N)
Converter Buffer Terminator	CBT	DEYR	1	1	All	
		YS	1	1	Out Ø	N to P
		DFYR	1	1	All	
		YS	1	1	Out Ø	P to N

Appendix A (continued)

Function	Sym-bol	Card Code	Ckts per Card	Inputs per Ckts	Internal Loading per Card	Application Notes
Converter Buffer	CB	DEYU	1	1	All	N to P
		DEYT	1	1	Out Ø	
		DFYU	1	1	All	P to N
		DFYT	1	1	Out Ø	
Extender	E	DEYV	1	4		Extends N Block
		DEYW	1	4		
		DFYV	1	4		Extends P Block
		DFYW	1	4		
4. SPECIAL FUNCTIONS						
Amplifiers	AM	GG--				Capacitor Sense
		HB--				
		VV				
		VW				
		WW				
		GU--				Drum Sense
		HH--				Tape Core Sense
Capacitor Storage	CS	GB--				
		HY--				
		HZ--				
Converters	C	CNWU				U to T
		CPWU				T to U
		GW--				U to X, X to U
		HAVE				Z to N
		HAVF				Z to U and T
Coupling Networks	R	AG--				Line Driver Loads
		AK--				Logic Block Loads
		CM--				CM to CTDL Loads
		GF--				Core Buffer Loads
		QS--				Drum Wr. Driver Ld.
Emitter Follower	DE	AEWY				N Output
		AEWZ				P Output
		CNWT				T Output
		CPWT				U Output
Delay Circuits	DLY	KH--				This Group of Cards
		KJ--				Provides 7 to 30,000
		KK--				us Delay of the Start
		KL--				of the Output Signal
		KM--				
		KN--				
		KP--				
Drivers	D	FU--				Gate and Reset
		GS--				Drum Write
		HR--				Coil Latch
		KE--				P and N Output
	DC	GLVG				Inverter(Core Driver)
		GLVH				Emitter Follower
		GX--				Bit Insert
		GY--				
		GZ--				
		HF--				
		HG--				
		HJ--				(Adder)
	DI	EA--				Indicator
		EB--				"
		GR--				"
		HX--				. "
		KA--				"
	DP	DMYP				Power (4-10 Bases)
		DMYQ				(4-10 Bases)
		DNYJ				(11-40 Bases)
		DNYL				(11-40 Bases)
		LE--				
	DR	GLVJ				Relay Driver
	DS	GT--				Drum Shaper

Function	Symbol	Card Code	Application Notes
Integrators	C	AQ--	CM to VM
		BGWA	W to N and P
		WB	W to N and P
		WC	W to N
		WD	W to P
		GP--	W to U
		KQ--	W to T
	CBL	GQ--	V to V
	R	HK--	Core Load (V to V)
Inverters	I	JLVB	Logic U to U
		JMVB	Logic T to T
	IP	CY--	T to U
		HE--	N to U
		HS--	Coil Drivers
		KB--	P to T
Line Drivers	DL	AMWX	N to P
		ANWX	P to N
		CS--	T to P
		CT--	U to N
		EF--	N to N
		EG--	P to P
		HC--	V to V
		KS--	P to P
		KT--	N to N
Line Terminators	DT	AF--	N to P
		AL--	P to N
		CU--	N to U
		CV--	P to T
		DH--	N to P
		DJ--	P to N
		DK--	P to P
		DL--	N to N
		HD--	N to P
Magnetic Core Cards	SR	FX--	Shift Register -2 Outputs
		FY--	" " Extender
		FZ--	" " -3 Outputs
		GA--	" " Extender
		KD--	" " (Significant Detection)
	VCK	GH--	Validity Check
	RDB	GM--	I/O Core Buffer
		GN--	" " "
Oscillator	OSC	GV--	Variable Gated (75KC-95KC)
Triggers	SS	AW--	CM "P" Out Single Shot
		EHVK	Diffused Junction P and N Out
		VL	
		VM	
		--	
		EJVK	Diffused Junction N and P Out
		VL	
		VM	
		--	
		NB--	CTDL "T" Out Single Shot
		NC--	CTDL "U" Out Single Shot
	T	CW--	CTDL U and T Outputs
		JZ--	CTDL U and T Outputs (Ext. Input)
	+TB	FG--	Binary Trigger N Out
		FH--	
	-TB	FF--	Binary Trigger P Out
		FJ--	
Special Purpose	FILT	GJ--	Filter Card for Supply Voltages
	CAP	GK--	Cable Decouple Capacitors
	DLY	HQ--	Capacitors used for Ring Delay
	E	JN--	Trigger Input Extender JZ--
	BD	LU--	Bus Capacitor Storage Discharge

Appendix B. Alphabetical Index of Card Codes

Card Code	Description	Part No.	Symbol
	CURRENT MODE		
AA--	Two-Way AND (no loads)	371207	+A
AAZU	Two-Way AND (out-of-phase load)	371206	+A
AAZV	Two-Way AND (in-phase load)	371205	+A
AAZW	Two-Way AND (both loads)	371204	+A
AB--	Two-Way OR (no loads)	371216	+O
ABZU	Two-Way OR (out-of-phase load)	371215	+O
ABZV	Two-Way OR (in-phase load)	371214	+O
ABZW	Two-Way OR (both loads)	371213	+O
ACYV	Four-Way AND-Block Extender	371227	E
ACYW	Two-Way AND-Block Extender	371226	E
ACYX	Three-Way AND (no loads)	371221	+A
ACYY	Three-Way AND (out-of-phase load)	371220	+A
ACYZ	Three-Way AND (in-phase load)	371219	+A
ACZA	Three-Way AND (both loads)	371218	+A
ACZF	Four-Way AND (no loads)	371225	+A
ACZG	Four-Way AND (out-of-phase load)	371224	+A
ACZH	Four-Way AND (in-phase load)	371223	+A
ACZJ	Four-Way AND (both loads)	371222	+A
ADYV	Four-Way OR-Block Extender	371237	E
ADYW	Two-Way AND-Block Extender	371236	E
ADYX	Three-Way OR (no loads)	371231	+O
ADYY	Three-Way OR (out-of-phase load)	371230	+O
ADYZ	Three-Way OR (in-phase load)	371229	+O
ADZA	Three-Way OR (both loads)	371228	+O
ADZF	Four-Way OR (no loads)	371235	+O
ADZG	Four-Way OR (out-of-ohase load)	371234	+O
ADZH	Four-Way OR (in-phase load)	371233	+O
ADZJ	Four-Way OR (both loads)	371232	+O
AEWY	N Line Complemented Emitter Follower	371238	DE
AEWZ	P Line Complemented Emitter Follower	371239	DE
AF--	N Line Terminator	371242	DT
AG--	Line Driver Coupling Network	371240	R
AK--	N and P Block Coupling Networks	371241	R
AL--	P Line Line Terminator	371243	DT
AM--	N to P Converter (no loads)	371203	C
AMWX	N Line Driver	371208	DL
AMZX	N to P Converter (out-of-phase load)	371202	C
AMZY	N toP Converter (in-phase load)	371201	C
AMZZ	N to P Converter (both loads)	371200	C
AN--	P to N Converter (no loads)	371212	C
ANWX	P Line Driver	371217	DL
ANZX	P to N Converter (out-of-phase load)	371211	C
ANZY	P to N Converter (in-phase load)	371210	C
ANZZ	P to N Converter (both loads)	371209	C
AQ--	P to S Current Mode to Voltage Mode Converter	371031	C
	CURRENT MODE		
AW--	3.2-215 Microsecond Universal Single Shot	371039	SS
BGWA	W to N and W to P Integrators	371430	C
BGWB	W to N and W to P Integrators	371429	C
BGWC	W to N Integrators	371428	C
BGWD	W to P Integrators	371427	C
	CTDL		
CG--	Two-Way-AND (no loads)	371263	-A
CGVV	Two-Way-AND (1 load)	371262	-A
CGVW	Two-Way-AND (2 loads)	371261	-A
CGWW	Two-Way-AND (all loads)	371251	-A
CH--	Two-Way+AND (no loads)	371266	+A
CHVV	Two-Way+AND (1 load)	371265	+A
CHVW	Two-Way+AND (2 loads)	371264	+A
CHWW	Two-Way+AND (all loads)	371252	+A
CJ--	Three-Way-AND (no loads)	371268	-A
CJVU	Three-Way-AND (1 load)	371267	-A
CJWV	Three-Way-AND (2 loads)	371253	-A
CJYC	Three-Way-AND (2 loads) (Ext. In)	371071	-A
CK--	Three-Way+AND (no loads)	371270	+A
CKVU	Three-Way+AND (1 load)	371269	+A
CKWV	Three-Way+AND (2 loads)	371254	+A
CKYC	Three-Way+AND (2 loads) (Ext. In)	371072	+A
CLVQ	Extender and Limiter Card	371255	E
CLVR	Extender and Limiter Card	371075	E

Card Code	Description	Part No.	Symbol
	CTDL		
CLVS	Extender and Limiter Card	371074	E
CLVT	Extender and Limiter Card	371073	E
CM--	CM to CTDL Coupling Network	371256	R
CNWT	Emitter Follower NPN	371260	DE
CNWU	U to T Converter	371258	C
CPWT	Emitter Follower PNP	371259	DE
CPWU	T to U Converter	371257	C
CQ--	T to U Converter (no loads)	371273	C
CQYG	T to U Converter (1 load)	371278	C
CQZT	T to U Converter (2 loads)	371272	C
CQZV	T to U Converter (4 loads)	371271	C
CR--	U to T Converter (no loads)	371276	C
CRYG	U to T Converter (1 load)	371277	C
CRZT	U to T Converter (2 loads)	371275	C
CRZV	U to T Converter (4 loads)	371274	C
CS--	N Type Line Driver	371520	DL
CT--	P Type Line Driver	371521	DL
CU--	N Type Line Terminator	371518	DT
CV--	P Type Line Terminator	371519	DT
CW--	Trigger	371534	T
CY--	Power Inverter	371542	IP
	DIFFUSED JUNCTION		
DAZU	Two-Way AND, Type A (out-of-phase load)	371281	+A
DAZW	Two-Way AND, Type A (both loads)	371280	+A
DAZX	N to P Converter, Type A (out-of-phase load)	371283	C
DAZZ	N to P Converter, Type A (both loads)	371282	C
DB--	N to P Converter, Type B (no loads)	371295	C
DBYD	Two-Way AND, Type B (Ckt 1, both loads) (Ckt 2, in-phase load)	371359	+A
DBZP	Plus Exclusive OR (no loads)	371291	+OE
DBZQ	Plus Exclusive OR (out-of-phase load)	371290	+OE
DBZR	Plus Exclusive OR (in-phase load)	371289	+OE
DBZS	Plus Exclusive OR (both loads)	371288	+OE
DBZT	Two-Way AND, Type B (no loads)	371287	+A
DBZU	Two-Way AND, Type B (out-of phase load)	371286	+A
DBZV	Two-Way AND, Type B (in-phase load)	371285	+A
DBZW	Two-Way AND, Type B (both loads)	371284	+A
DBZX	N to P Converter, Type B (out-of-phase load)	371294	C
DBZY	N to P Converter, Type B (in-phase load)	371293	C
DBZZ	N to P Converter, Type B (both loads)	371292	C
DCZU	Two-Way OR, Type A (out-of-phase load)	371297	+O
DCZW	Two-Way OR, Type A (both loads)	371296	+O
DCZX	P to N Converter, Type A (out-of-phase load)	371299	C
DCZZ	P to N Converter, Type A (both loads)	371298	C
DD--	P to N Converter, Type B (no loads)	371311	C
DDZP	Minus Exclusive OR (no loads)	371307	-OE
DDZQ	Minus Exclusive OR (out-of-phase load)	371306	-OE
DDZR	Minus Exclusive OR (in-phase load)	371305	-OE
DDZS	Minus Exclusive OR (both loads)	371304	-OE
DDZT	Two-Way OR, Type B (no loads)	371303	+O
DDZU	Two-Way OR, Type B (out-of-phase load)	371302	+O
DDZV	Two-Way OR, Type B (in-phase load)	371301	+O
DDZW	Two-Way OR, Type B (both loads)	371300	+O
DDZX	P to N Converter, Type B (out-of-phase load)	371310	C
DDZY	P to N Converter, Type B (in-phase load)	371309	C
DDZZ	P to N Converter, Type B (both loads)	371308	C
DEYR	N to P Terminator-Buffer-Converter (out-of-phase load)	371329	CBT
DEYS	N to P Terminator-Buffer-Converter (both loads)	371328	CBT
DEYT	N to P Buffer Converter (out-of-phase load)	371327	CB

Card Code	Description	Part No	Symbol
	DIFFUSED JUNCTION		
DEYU	N to P Buffer Converter (both loads)	371326	CB
DEYV	Four-Way AND-Block Extender	371318	E
DEYW	Two-Way AND-Block Extender	371325	E
DEYX	Three-Way AND, Type B (no loads)	371324	+A
DEYY	Three-Way AND, Type B (out-of phase load)	371323	+A
DEYZ	Three-Way AND, Type B (in-phase load	371322	+A
DEZA	Three-Way AND, Type B (both loads)	371321	+A
DEZC	Three-Way AND, Type A (out-of-phase load)	371320	+A
DEZE	Three-Way AND, Type A (both loads)	371319	+A
DEZF	Four-Way AND, Type B (no loads)	371317	+A
DEZG	Four-Way AND, Type B (out-of-phase load)	371316	+A
DEZH	Four-Way AND, Type B (in-phase load)	371315	+A
DEZJ	Four-Way AND, Type B (both loads)	371314	+A
DEZL	Four-Way AND, Type A (out-of-phase load)	371313	+A
DEZN	Four-Way AND, Type A (both loads)	371312	+A
DFYR	P to N Terminator-Buffer-Converter (out-of-phase load)	371348	CBT
DFYS	P to N Terminator-Buffer-Converter (both loads)	371347	CBT
DFYT	P to N Buffer Converter (out-of-phase load)	371346	CB
DFYU	P to N Buffer Converter (both loads)	371345	CB
DFYV	Four-Way OR-Block Extender	371336	E
DFYW	Two-Way OR-Block Extender	371344	E
DFYX	Three-Way OR, Type B (no loads)	371343	+O
DFYY	Three-Way OR, Type B (out-of-phase load)	371342	+O
DFYZ	Three-Way OR, Type B (in-phase load)	371341	+O
DFZA	Three-Way OR, Type B (both loads)	371340	+O
DFZC	Three-Way OR, Type A (out-of-phase load)	371338	+O
DFZE	Three-Way OR, Type A (both loads)	371337	+O
DFZF	Four-Way OR, Type B (no loads)	371335	+O
DFZG	Four-Way OR, Type B (out-of-phase load)	371334	+O
DFZH	Four-Way OR, Type B (in-phase load)	371333	+O
DFZJ	Four-Way OR, Type B (both loads)	371332	+O
DFZL	Four-Way OR, Type A (out-of-phase load)	371331	+O
DFZN	Four-Way OR, Type A (both loads)	371330	+O
DH--	N to P Line Terminator	371138	DT
DJ--	P to N Line Terminator	371139	DT
DK--	P to P Line Terminator	371140	DT
DL--	N to N Line Terminator	371141	DT
DMYP	P to P Power Driver (4-10 Bases)	371350	DP
DMYQ	N to N Power Driver (4-10 Bases)	371349	DP
DNYJ	P to P Power Driver (11-40 Bases)	371354	DP
DNYL	N to N Power Driver (11-40 Bases)	371351	DP
EA--	Minus N Line Indicator	371363	DI
EB--	Plus P Line Indicator	371364	DI
EF--	N to N Line Driver	371171	DL
EG--	P to P Line Driver	371375	DL
EH--	N Line Single Shot (no loads)	371369	SS
EHVK	N Line Single Shot (both loads)	371368	SS
EHVL	N Line Single Shot (in-phase load)	371367	SS
EHVM	N Line Single Shot (out-of-phase load)	371366	SS
EJ--	P Line Single Shot (no loads)	371374	SS
EJVK	P Line Single Shot (both loads)	371373	SS
EJVL	P Line Single Shot (in-phase load)	371372	SS
EJVM	P Line Single Shot (out-of-phase load)	371371	SS
	CURRENT MODE		
FF--	Negative Binary Trigger Card 1	371411	-TB
FG--	Positive Binary Trigger Card 2	371414	+TB
FH--	Positive Binary Trigger Card 1	371413	+TB

Card Code	Description	Part No.	Symbol
	CURRENT MODE		
FJ--	Negative Binary Trigger Card 2	371412	-TB
FU--	Coil Driver Gate and Reset Driver	371616	D
FX--	Magnetic Core Shift Register	371506	SR 1
FY--	Magnetic Core Shift Register Extender	371507	SR 2
FZ--	Magnetic Core Shift Register	371508	SR 3
GA--	Magnetic Core Shift Register Extender	371509	SR 4
GB--	Capacitor Storage	371505	CS
GF--	Bias Load and Coupling Networks	371538	R
GG--	Capacitor Sense Amplifier and Driver	371503	CSAD
GH--	Two of Five Validity Check Circuit	371504	VCK
GJ--	General Purpose Filter Card	371501	FILT
GK--	Cable Decouple Card	371533	CAP
GLVG	Inverter Core Driver	371536	DC
GLVH	Emitter Follower Core Driver	371537	DC
GLVJ	Relay Driver	371535	DR
GM--	Input Output Core Card No. 1	371532	RDB
GN--	Word Size Buffer Core	371523	WSB
GP--	W to U Line Converter	371502	C
GQ--	Core Buffer Integrator	371515	C
GR--	CTDL Low Current Indicator Driver	371528	DI
GS--	Drum Write Driver	371524	D
GT--	Drum Sense Shaper	371525	DS
GU--	Drum Sense Amplifier	371526	AM
GV--	Variable Gated Oscillator	371531	OSC
GW--	Converter (1) U to X Level (2) X to U Level	371522	C
GX--	Magnetic Core Bit Insert Driver	371514	DC
GY--	Magnetic Core Read-Out Driver	371511	D
GZ--	Magnetic Core Read-In Driver	371510	D
HAVE	Core Mode Z to N Converter	371516	C
HAVF	Core Mode to CTDL Converter	371513	C
HB--	Capacitor Sense Amplifier (no loads)	371561	AM
HBVV	Capacitor Sense Amplifier (1 load)	371560	AM
HBVW	Capacitor Sense Amplifier (2 loads)	371559	AM
HBWW	Capacitor Sense Amplifier (3 loads)	371500	AM
HC--	Sync Line Driver	371527	DL
HD--	Sync Line Terminator	371540	DT
HE--	Current Mode to CTDL Power Inverter	371541	IP
HF--	Magnetic Core Read-Out Control Driver	371512	D
HG--	Digit Read-In Driver	371517	D
HH--	Tape Core Sense Amplifier	371529	AM
HJ--	Core Adder Driver	371530	D
HK--	Integrator Load Card	371543	R
HQ--	Ring Delay Network	371544	DLY
HR--	Current Mode, Coil Driver Latch	371620	D
HS--	Current Mode, Coil Driver Power Inverter	371498	IP
HX--	Current Mode, Minus N Line Indicator	371049	DI
HY--	Capacitor Storage	371548	CS
HZ--	Capacitor Storage	371549	CS
	CTDL HIGH SPEED		
JF--	T to U Converter (no loads)	371579	C
JFVA	T to U Converter (1 load)	371578	C
JFVV	T to U Converter (2 loads)	371577	C
JFVP	T to U Converter (4 loads)	371576	C
JG--	Two-Way -AND (no loads)	371583	-A
JGVV	Two-Way -AND (1 load)	371582	-A
JGVW	Two-Way -AND (2 loads)	371581	-A
JGWW	Two-Way -AND (3 loads)	371580	-A
JH--	Three-Way -AND (no loads)	371586	-A
JHVU	Three-Way -AND (1 load)	371585	-A
JHWV	Three-Way -AND (2 loads)	371584	-A
JJ--	U to T Converter (no loads)	371590	C
JJVA	U to T Converter (1 load)	371589	C
JJVN	U to T Converter (2 loads)	371588	C
JJVP	U to T Converter (4 loads)	371587	C
JLVB	CTDL Logic Inverter (PNP)	371077	I
JMVB	CTDL Logic Inverter (NPN)	371079	I
JN--	CTDL Trigger Extender Card	371081	E
JZ--	CTDL Trigger 2	371082	T
KA--	High Current Indicator Driver	371546	DI
KB--	Current Mode to CTDL Power Inverter	371558	IP
KD--	Core Shift Register (Significant Digit Detection	371563	SR5

APPENDIX B (cont'd)

Card Code	Description	Part No.	Symbol
KE--	Current Mode P and N Driver	371547	D
KH--	CTDL Delay Circuit	371564	DLY
KJ--	CTDL Delay Circuit	371565	DLY
KK--	CTDL Delay Circuit	371566	DLY
KL--	CTDL Delay Circuit	371567	DLY
KM--	CTDL Delay Circuit	371568	DLY
KN--	CTDL Delay Circuit	371569	DLY
KP--	CTDL Delay Circuit	371570	DLY

Card Code	Description	Part No.	Symbol
KQ--	Converter W to T Line	371545	C
KS--	Current Mode, P to P Line Driver	371476	DL
KT--	Current Mode, N to N Line Driver	371480	DL
LE--	Sync Power Driver	371572	DP
LU--	Bus Discharge Card	371575	BD
NB--	CTDL Single Shot Trigger (T Input)	371591	SS
NC--	CTDL Single Shot Trigger (U Input)	371592	SS
QS--	Drum Load Card	371574	R

Appendix C. SMS Card Index by Part Number (System Usage Noted)

Part Number	Card Code	System Use 7070	7090
371031	AQ--		X
371039	AW--		X
371049	HX--		X
371071	CJYC	X	
371072	CKYC	X	
371073	CLVT	X	
371074	CLVS	X	
371075	CLVR	X	
371077	JLVB	X	
371079	JMVB	X	
371081	JN--	X	
371082	JZ--	X	
371138	DH--		X
371139	DJ--		X
371140	DK--		X
371141	DL--		X
371171	EF--		X
371174	DDYD		X
371200	AMZZ	X	X
371201	AMZY	X	X
371202	AMZX	X	X
371203	AM--	X	X
371204	AAZW	X	X
371205	AAZV	X	X
371206	AAZU	X	X
371207	AA--	X	X
371208	AMWX	X	X
371209	AMZZ	X	X
371210	AMZY	X	X
371211	AMZX	X	X
371212	AN--	X	X
371213	ABZW	X	X
371214	ABZV	X	X
371215	ABZU	X	X
371216	AB--	X	X
371217	ANWX	X	X
371218	ACZA	X	X
371219	ACYZ	X	X
371220	ACYY	X	X
371221	AZYX	X	X
371222	ACZJ	X	X
371223	ACZH	X	X
371224	ACZG	X	X
371225	ACZF	X	X
371226	ACYW	X	X
371227	ACYV	X	X
371228	ADZA	X	X
371229	ADYZ	X	X
371230	ADYY	X	X
371231	ADYX	X	X
371232	ADZJ	X	X
371233	ADZH	X	X
371234	ADZG	X	X
371235	ADZF	X	X
371236	ADYW	X	X
371237	ADYV	X	X
371238	AEWY	X	X
371239	AEWZ	X	X
371240	AG--	X	X
371241	AK--	X	X
371242	AF--	X	X
371243	AL--	X	X
371251	CGWW	X	
371252	CHWW	X	
371253	CJWV	X	
371254	CKWV	X	
371255	CLVQ	X	

Part Number	Card Code	System Use 7070	7090
371256	CM--	X	
371257	CPWU	X	
371258	CNWU	X	
371259	CPWT	X	
371260	CNWT	X	
371261	CGVW	X	
371262	CGVV	X	
371263	CG--	X	
371264	CHVW	X	
371265	CHVV	X	
371266	CH--	X	
371267	CJVU	X	
371268	CJ--	X	
371269	CKVU	X	
371270	CK--	X	
371271	CQZV	X	
371272	CQZT	X	
371273	CQ--	X	
371274	CRZV	X	
371275	CRZT	X	
371276	CR--	X	
371277	CRYG	X	
371278	CQYG	X	
371280	DAZW	X	X
371281	DAZU	X	X
371282	DAZZ		X
371283	DAZX		X
371284	DBZW		X
371285	DBZV		X
371286	DBZU		X
371287	DBZT		X
371288	DBZS		X
371289	DBZR		X
371290	DBZQ		X
371291	DBZP		X
371292	DBZZ		X
371293	DBZY		X
371294	DBZX		X
371295	DB--		X
371296	DCZW		X
371297	DCZU		X
371298	DCZZ		X
371299	DCZX		
371300	DDZW		X
371301	DDZV		X
371302	DDZU		X
371303	DDZT		X
371304	DDZS		X
371305	DDZR		X
371306	DDZQ		X
371307	DDZP		X
371308	DDZZ		X
371309	DDZY		X
371310	DDZX		X
371311	DD--		X
371312	DEZN		X
371213	DEZL		X
371314	DEZJ		X
371315	DEZH		X
371316	DEZG		X
371317	DEZF		X
371318	DEYV		X
371319	DEZE		X
371320	DEZC		X
371321	DEZA		X
371322	DEYZ		X
371323	DEYY		X

Part Number	Card Code	System Use 7070	7090
371324	DEYX		X
371325	DEYW		X
371326	DEYU		X
371327	DEYT		X
371328	DEYS		X
371329	DEYR		X
371330	DFZN		X
371331	DFZL		X
371332	DFZJ		X
371333	DFZH		X
371334	DFZG		X
371335	DFZF		X
371336	DFYV		X
371337	DFZE		X
371338	DFZC		X
371340	DFZA		X
371341	DFYZ		X
371342	DFYY		X
371343	DFYX		X
371344	DFYW		X
371345	DFYU		X
371346	DFYT		X
371347	DFYS		X
371348	DFYR		X
371349	DMYQ		X
371350	DMYP		X
371351	DNYL		X
371354	DNYJ		X
371359	DBYD		X
371360	EA--		X
371364	EB--		X
371366	EHVM	X	X
371367	EHVL	X	X
371368	EHVK	X	X
371369	EH--	X	X
371371	EJVM	X	X
371372	EJVL	X	X
371373	EJVK	X	X
371374	EJ--	X	X
371375	EG--		X
371411	FF--		X
371412	FJ--		X
371413	FH--		X
371414	FG--		X
371427	BGWD		X
371428	BGWC		X
371429	BGWB		X
371430	BGWA		X
371476	KS--	X	X
371480	KT--	X	X
371498	HS--		X
371500	HBWW	X	
371501	GJ--	X	
371502	GP--	X	
371503	GG--	X	
371504	GH--	X	
371505	GB--	X	
371506	FX--	X	
371507	FY--	X	
371508	FZ--	X	
371509	GA--	X	
371510	GZ--	X	
371511	GY--	X	
371512	HF--	X	
371513	HAVF	X	
371514	GX--	X	

Part Number	Card Code	System Use 7070	7090
371515	GQ--	X	
371516	HAVE	X	
371517	HG--	X	
371518	CU--	X	
371519	CV--	X	
371520	CS--	X	
371521	CT--	X	
371522	GW--	X	
371523	GN--	X	
371524	GS--	X	
371525	GT--	X	
371527	HC--	X	
371528	GR--	X	
371530	HJ--	X	
371531	GV--	X	
371532	GM--	X	
371533	GK--	X	
371534	CW--	X	
371535	GLVJ	X	
371536	GLVG	X	
371537	GLVH	X	
371538	GF--	X	
371540	HD--	X	
371541	HE--	X	
371542	CY--	X	
371543	HK--	X	
371544	HQ--	X	
371545	KQ--	X	
371546	KA--	X	
371547	KE--	X	
371548	HY--	X	
371549	HZ--	X	
371558	KB--	X	
371559	HBVW	X	
371560	HBVV	X	
371561	HB--	X	
371563	KD--	X	
371564	KH--	X	
371565	KJ--	X	
371566	KK--	X	
371567	KL--	X	
371568	KM--	X	
371569	KN--	X	
371570	KP--	X	
371572	LE--	X	
371574	QS--	X	
371575	LU--	X	
371576	JFVP	X	
371577	JGVN	X	
371578	JFVA	X	
371579	JF--	X	
371580	JGWW	X	
371581	JGVW	X	
371582	JGVV	X	
371583	JG--	X	
371584	JHWV	X	
371585	JHVU	X	
371586	JH--	X	
371587	JJVP	X	
371588	JJVN	X	
371589	JJVA	X	
371590	JJ--	X	
371591	NB--	X	
371592	NC--	X	
371616	FU--		X
371620	HR--		X

Appendix D. Functional Symbols Used in ALD Transistor Circuits

Name	Description	Std. Symbol	Symbols Prev. used in 7070
Positive AND	In-phase output is positive only when all inputs are positive. Out-of-phase output is negative for the above condition.	+A	
Negative AND	In-phase output is negative only when all inputs are negative. Out-of-phase output is positive for the above condition.	-A	
Amplifier	Provides increased strength to a detected signal or pulse.	AM	CSA CSAD TCSA DSA
DOT OR	An AND circuit whose output shares a common load with one or more other circuits to provide an OR function at the output.	AO	
Converter	Used to translate from one voltage level to another, or to change the amplitude of the voltage swing about the same reference level.	C	NIA XL INT
Converter Buffer	A converter block that uses the current mode transmission line driver signal sent from a transmitting frame to generate voltage swings referenced to voltage planes of other frames.	CB	
Converter Buffer Terminator	A converter buffer that terminates a coaxial line with its characteristic impedance.	CBT	
Capacitor Storage	Used as secondary storage devices.	CS	
Driver	Isolates a signal from its generating source and uses it to drive one or more other circuits without affecting or overloading the generating circuits. Can be used to supply the required power directly or only to activate the circuit through which power is actually supplied.	D	ROD RID DRID ROCD SLD DSS
Driver Core	Same as D, with the device being driven identified as a core.	DC	BID
Driver Emitter Follower	A driver, operating on the emitter follower principle, used for power amplification, impedance matching, and isolation without inversion. Often used as a logical element.	DE	
Driver, Emitter Follower, AND'ed	Same as DE but DOT AND'ed	DEA	
Driver, Emitter Follower, OR'ed	Same as DE but DOT OR'ed	DEO	
Driver, Line	Used to couple information between two widely separated points by means of coaxial line.	DL	
Delay	Delays a pulse for a certain specified constant time.	DLY	DEL PFN
Driver, Indicator	Driver operating into an indicating device.	DI	IND
Driver, Power	A power driver used to drive into multiple bases.	DP	
Driver, Relay	Same as D with the device being driven identified as a relay.	DR	RD

Name	Description	Std. Symbol	Symbols Prev. used in 7070
Driver Sample Pulse	Same as D, with the additional function of supplying a specific length pulse output when the input consists of a gate and a sample pulse spike. The input may also be the output of a current switching circuit without a gate.	DSP	
Driver, Sample Pulse OR'ed	Same as DSP but DOT OR'ed.	DSPO	
Driver, Terminator	A single-transistor class-A grounded-base amplifier used to terminate a transmission line.	DT	LT
Extender	Provides additional inputs to logical blocks and triggers. Adds to drivers the ability to drive more loads.	E	
Filter	Capacitor card used to filter voltage supplies.	FILT	
Gate	Provides a switching pulse of voltage or current, positive or negative, that conditions some other circuit so that it may become either activated or deactivated by one or more other pulses.	G	
Inverter	Changes a positive input to a negative output, or vice versa.	I	
Indicator	Visually indicates a function or an error.	IND	
Inverter, Power	Performs function of an inverter while also driving a line.	IP	PI
Limiter or Clamp	Limits or clamps a voltage or current to a predetermined value.	L	
Positive OR	In-phase output is positive if one or more input signals are positive. Out-of phase output is negative for the above condition.	+O	
Negative OR	In-phase output is negative if one or more input signals are negative. Out-of-phase output is positive for the above condition.	-O	
DOT AND	An OR circuit whose output is connected to the output of one or more logic blocks to provide an AND function at the output.	OA	
Positive Exclusive OR	In-phase output is positive only when inputs differ (A up, B down, or B up and A down). Out-of-phase output is negative for the above conditions.	+OE	
Negative Exclusive OR	In-phase output is negative only when inputs differ (A up and B down, or B up and A down). Out-of-phase output is positive for the above conditions.	-OE	
Oscillator	A free-running non-stable multivibrator used to provide pulses of a given frequency and amplitude.	OSC	
Photocell	A circuit that has an input signal obtained from a photovoltaic cell whose light source is varied.	P	
Photocell Converter Buffer	Same as converter buffer except that signal source is a photovoltaic cell.	PCB	
Pulse Generator	Provides pulses of a particular frequency, rise time, and amplitude.	PG	
Load	Provides proper terminating impedance or optimum coupling of one circuit to another at the correct operating voltage level.	R	CBL INT DC

Name	Description	Std. Symbol	Symbols Prev. used in 7070
Read Buffer Core	Used as card scanning buffer between card reader and central processing unit.	RDB	
Shift Register Cards	Used to form shift registers capable of serial and parallel shifting.	SR	
Single Shot	Provides a monostable output which can be pulsed into its quasi-stable state for a predetermined duration, with each input triggering pulse or triggering voltage change. Once triggered, the output pulse duration becomes independent of input time duration or amplitude.	SS	
Trigger	A conditioned bi-stable device whose steady-state outputs change from one stable state to the other with two separate triggering levels, pulses, or voltage changes. The set input turns the trigger on if the reset input is not on, and vice versa.	T	
Trigger (Binary)	A trigger whose steady state outputs change upon the transition of the input, i.e., usually going plus to minus, or sometimes going minus to plus.	TB	
TC Trigger	A converter used within a trigger	TC	
(+TA Trigger) (+TO Trigger)	Represent two logical halves of a trigger that is physically divided. The +TO symbol is usually applied to the SET side, TA to Reset (trigger resets with minus signals).*	TA TO	
(-TA Trigger) (-TO Trigger)	Same as TO and TA except that negative triggering is used.*	-TA -TO	
Validity Check	Used for checking information bits in the 2-of-5 bit code system.	VCK	

* Positive (+) and negative (-) signs for triggers.

A positive (+) sign indicates that to fulfill the condition stated by the title a Positive DC level, triggering pulse, or voltage change produces a Positive condition on the in-phase output lines.

A Negative DC level triggering pulse, or voltage change, produces a Negative condition on the in-phase output lines.

Appendix E. Index to Additional Cards

Card Code	Description	Part Number	Symbol	Page
AJWE	Voltage Mode Trigger 3 (CM Gates)	371424	TV	200
AJWF	Voltage Mode Trigger 3 (VM Gates)	371423	TV	200
AJWG	Voltage Mode Trigger 3 (CM Gate, VM Gate)	371422	TV	200
AJWH	Voltage Mode Trigger 3 (VM Gate, CM Gate)	371421	TV	200
AJWJ	Voltage Mode Trigger 3 (CM Gate, Reset)	371420	TV	200
AJWK	Voltage Mode Trigger 3 (VM Gate, Reset)	371419	TV	200
AJWL	Voltage Mode Trigger 3 (CM Gate, VM Reset)	371418	TV	200
AR--	Voltage Mode Trigger 1	371034	TV	202
AS--	Voltage Mode Trigger 2	371035	TV	204
AYWM	Gated Sample Pulse Driver 2 (CM, Collector Out)	371426	DSP	206
AYWN	Gated Sample Pulse Driver 2 (VM, Collector Out)	371425	DSP	206
AYWP	Gated Sample Pulse Driver 2 (CM, 6v out)	371044	DSP	206
AYWQ	Gated Sample Pulse Driver 2 (CM, 3v out)	371043	DSP	206
AYWR	Gated Sample Pulse Driver 2 (VM, 6v out)	371042	DSP	206
AYWS	Gated Sample Pulse Driver 2 (CM, 3v out)	371041	DSP	206
CA--	CTRL Three-Way NPN Translating Circuits	371026	+A	208
CB--	CTRL Three-Way PNP Translating Circuit	371027	-A	209
CC--	CTRL Three-Way NPN Non-Translating Circuits	371028	+O	210
CD--	CTRL Three-Way PNP Non-Translating Circuits	371029	-O	211
CEYB	CTRL Emitter Follower PNP	371032	DE	212
CFYA	CTRL Emitter Follower NPN	371033	DE	214
FA--	Free Running Crystal Oscillator (1000KC)	371406	Osc	216
FK--	Free Running Crystal Oscillator (64KC)	371416	Osc	216
FS--	Free Running Crystal Oscillator (240KC)	371404	Osc	216
FT--	Free Running Crystal Oscillator (360KC)	371405	Osc	216
GC--	Current Mode +N Indicator Driver	371040	DI	218
GD--	Free Running Crystal Oscillator (125KC)	371455	Osc	216
GE--	Free Running Crystal Oscillator (500KC)	371456	Osc	216
HW--	Voltage Mode Indicator Driver	371048	DI	219
KR--	Free Running Crystal Oscillator (720KC)	371457	Osc	216
KW--	Core Driver	371483	DC	220
KX--	Power Gate	371484	G	221
KZ--	Matrix Switch Driver	371482	D	222
LH--	Free Running Crystal Oscillator (667KC)	371626	Osc	216
MM--	Single Shot Timing Card 4	371624	SS	223
MN--	Single Shot Timing Card 5	371625	SS	223
MP--	Single Shot Timing Card 6	371638	SS	223
MQ--	Clamped Oscillator	371646	Osc	224
MR--	Voltage Mode Single Shot 2	371623	SS	226
ND--	CTDL Universal Delay	371573	DLY	228
NHWU	CTDL T to U Converter	371629	C	229
NJWU	CTDL U to T Converter	371630	C	230
NKWT	CTDL Emitter Follower PNP	371631	DE	231
NLWT	CTDL Emitter Follower NPN	371632	DE	232
NU--	CTDL Power Inverter NPN	371676	IP	233
RK--	Free Running Crystal Oscillator (363.4KC)	371788	Osc	216
RT--	Free Running Crystal Oscillator (75KC)	371785	Osc	216

Card Maintenance

Cleaning and Lubricating

Use the following procedure to clean SMS card tab contacts that have not been lubricated or that are visibly contaminated with foreign particles. This procedure insures low contact resistance and reduces wear of the gold-plated contact surface. If any doubt exists about the contamination of the card tabs, relubricate them. The cleaning and lubricating procedure permits relubricating any number of times without affecting contact reliability.

1. Use SMS card contact lubricant (to be released) or equivalent. The equivalent is 5% (±2%) petrolatum by weight in 1.1.1 trichloroethane.
2. Apply the lubricant indirectly by saturating a clean piece of cheesecloth or lint-free industrial tissue, or apply the lubricant directly by wetting all 16 card tabs with the lubricant.
3. Clean and lubricate the card tabs by wiping them with a moistened cloth or tissue from the leading edge *toward* the component section of the card.
4. Rub the contact with a clean piece of cloth or tissue until no trace of lubricant is visible. If the contacts have been properly cleaned, the cloth or tissue will not be soiled.
5. Repeat the procedure if the cloth or tissue is soiled.

Field Maintenance

Nonavailability of spares and economy sometimes require field repair of cards.

The printed circuit is comparatively easy to troubleshoot because conductors and components are easily accessible. Replacing defective components is not difficult if reasonable care is used. The printed card can be damaged, however, by excessive heat during unsoldering or resoldering components or if strong-arm methods are used to remove a component. Overheating deteriorates the adhesive bond between the conductor and insulating base material. Conductors cannot withstand heavy stresses applied by component leads if these stresses tend to pull the conductor away from the laminate. The conductors are practically immune to stresses directed toward the laminate, as shown in Figure 22.

A raised or unlaminated conductor should be clipped off to a point where the bond is not broken and then repaired with solder.

WARNING: Printed cards are delicate and can be easily damaged. Always use a low wattage soldering iron to apply heat. Remove the iron from the joint quickly. Be careful not to apply excessive heat to transistor leads; transistors can be damaged by heat.

Component Removal

The following procedure for replacing a component on a printed card is recommended for most repairs.

1. Cut defective component leads as close as possible to the base on the component side of the card. All components, including transistors, should be removed by using diagonal cutting pliers; be careful not to damage the card or adjacent components.
2. Hold the card in your hand and with a clean, tinned soldering iron heat the leads at the printed circuit land pattern side. When the solder just starts to flow, a rap of the hand on the work surface causes the solder and remaining piece of wire to leave the hole.
3. In most cases this procedure provides a clean hole in which to install a new component lead; use as little heat as possible to clean the hole.
4. In every case, before a repaired card can be considered repaired, it must be tested dynamically in a machine or test instrument.

The preceding procedure is destructive to the removed component because the leads are cut. When the leads of the component must be preserved and the leads are bent over on the *wiring side* of the card, take care when straightening the leads to apply no force tending to separate the conductor from the board. The leads can be straightened with the tip of the iron or long nose pliers (Figure 23). This operation usually requires the iron to remain on the card longer than in the first procedure, and should be used only when absolutely necessary. After the component leads are straightened, they can be heated and pulled from the board.

Installing New Component

1. Insert component and cut leads, leaving about 1/16 inch of lead to bend over on the land pattern.

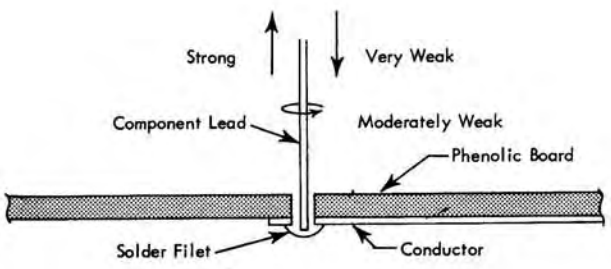


Figure 22. Stress Applied to Component Leads

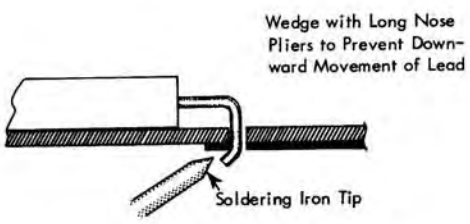


Figure 23. Component Removal

2. Apply heat to the component lead on the wiring side of the board, and allow the solder to run down the lead to the hole and land pattern. Use just enough solder and heat to fill the hole and to make a good electrical connection. If heat is applied equally to the component lead and the land pattern, the land pattern may be damaged before the component lead is hot enough to solder.

3. Wash the general area of repair using a typewriter cleaning brush and IBM cleaning fluid (P/N 450608); wipe the area with a clean piece of cloth or tissue.

Card Inspection

1. Visually inspect resistors, inductors, and capacitors for signs of physical damage, discolored value bands, melted wax, and other signs of overheating.

2. Inspect for damaged printed circuit card contacts and leading edge of card.

3. Inspect for solder splashes and short circuited printed wiring.

4. Check for improperly soldered components on the printed circuit board.

Transistor Measurement

WARNING: Always use the X100 scale of the ohmmeter to protect transistors from excessive current.

A good-bad test to indicate open or shorted transistor junctions may be performed on a transistor without removing it from the printed circuit card. For the test, transistors are considered as two back-to-back diodes, arranged in NPN or PNP configuration. Check forward and reverse resistance of each diode with an ohmmeter adjusted to the X100 ohm scale (Figure 24). If the resistance is high in both directions the transistor is open. If the resistance is low in both directions, the transistor is shorted.

NOTE: Before removing and discarding the transistor as a result of this test, check the printed card to establish that an apparently shorted transistor junction is not the result of its being shunted by a low resistance component.

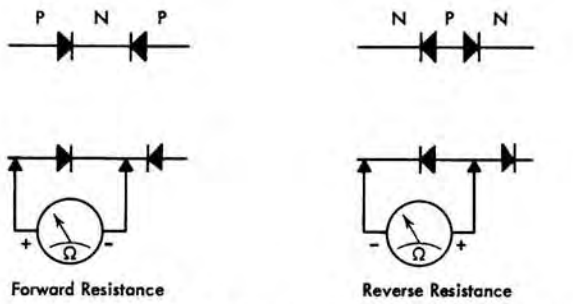


Figure 24. Transistor Measurements

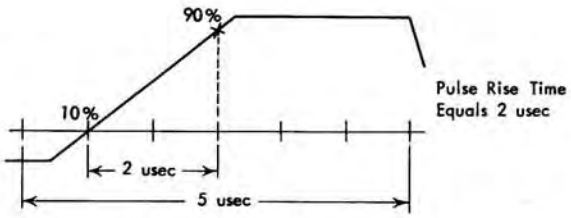


Figure 25. Pulse Rise Time Measurement

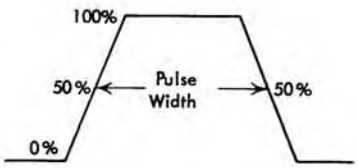


Figure 26. Pulse Duration Measurement

Circuit Measurements

Pulses

These measurements require an oscilloscope with a calibrated sweep time base and a frequency response high and low enough to pass all frequencies in the pulse spectrum to be measured. A high impedance (10:1 attenuating) probe is usually used in this type of measurement to avoid distorting the pulse. This type of probe must be calibrated to the oscilloscope used.

Pulse Rise Time is the time required for the leading edge of a pulse to complete 80 percent of its change in level as measured between the 10 percent and 90 percent points. Calibrate the oscilloscope sweep time for a slightly greater time than the rise time to be measured. The pulse rise time (Figure 25) can be read directly from the oscilloscope.

Pulse Duration is the time between a 50 percent point on the pulse rise time and 50 percent point on the pulse decay time (Figure 26). This quantity can be measured using the same techniques as for measuring pulse rise time.

Pulse Decay Time is the same as pulse rise time, except that it occurs on the trailing edge of the pulse.

Pulse Droop and Pulse Overshoot are measured as a percentage of total pulse amplitude (Figure 27).

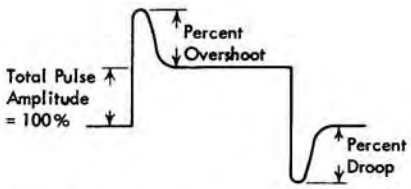


Figure 27. Pulse Droop and Overshoot

Signal Level Measurement

Use the oscilloscope for point-to-point P and N line measurements. A grease pencil line may be used to mark line levels and tolerance limits on the scope face (Figure 28). Note that oscilloscope calibration varies with the type of probe, plug-in-amplifier, and oscilloscope used.

Phase Shift and Time Delay Measurement

Phase shift is a time delay of less than one cycle of the fundamental frequency of the measured waveform. It is expressed in cycle degrees. Time delay is a delay of

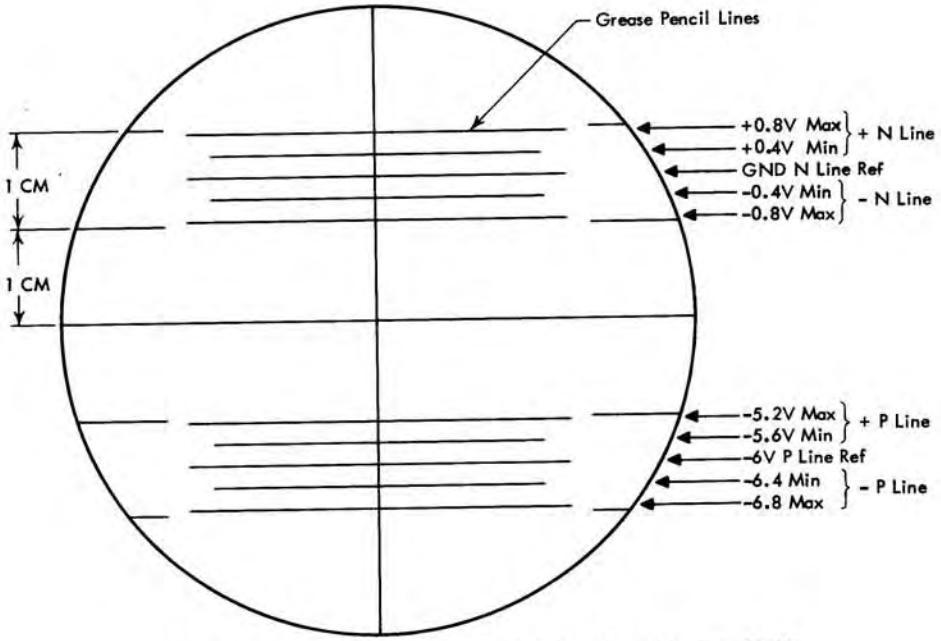


Figure 28. Signal Level Measurements (Oscilloscope)

more than one cycle. In this manual, both phase shift and time delay are measured in the same way.

Use a Tektronix oscilloscope with a dual channel amplifier. Connect one amplifier input to the reference or input terminals and the other to the delayed or output terminals. Adjust the oscilloscope time-centimeter and positioning controls to position the two pulses as shown in Figure 29. Find the time delay in milliseconds or microseconds by dividing the time scale indicated on the time/cm dial by the number of centimeters between the input and output pulse.

Current Measurement

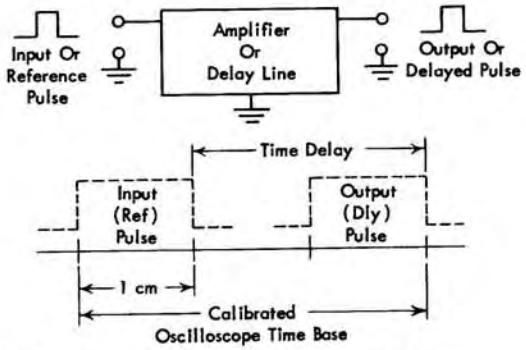
Current measurements are useful in troubleshooting totally inoperative machines or troubles that are widespread. They often take less time than more complex troubleshooting methods.

CAUTION: Remove power when connecting ammeters in circuit or when changing connections to the laminar bus.

Before measuring current, make sure that voltages are within specified tolerances. Then measure total current drain from the power supply to the machine for each voltage bus. If current drain is excessive on any voltage bus, remove the jumpers from the laminar bus to the card rows, one at a time, until the current indication is about normal. When the trouble is isolated to one card row, remove all power from the machine, and use resistance measurements to locate the defective component.

If the current drain for any one voltage bus is so excessive that power supply fuses blow as soon as they are replaced, remove all jumper wires from the laminar bus to the card rows and replace them one at a time until the shorted card row is discovered.

Alternating current, 60 cycles or 400 cycles, may be measured with a meter as follows: Connect a one-ohm, high wattage resistor in series with the load and measure the voltage drop across it. Because $I = E/R$ and $R = 1$, the current will equal the voltage indicated on the meter. Error introduced by the current limiting effect of the one-ohm resistor in series with the load may be disregarded.



* The leading edge, trailing edge or pulse center can be used as a reference point for measuring time delay.

Time/cm = 10 μsec/cm Time Delay = $\frac{10\,\mu\text{sec/cm}}{2\text{ cm}}$ = 5 μsec

Figure 29. Phase Shift and Time Delay Measurement

Frequency Measurement

To measure the fundamental frequency of a sine wave or square wave, adjust the time/centimeter and positioning controls of the Tektronix oscilloscope to center the waveform (Figure 30). The oscilloscope horizontal sweep dials indicate the time for the waveform to complete one cycle. The relationship between time in seconds and frequency in cycles per second is as follows:

$$\text{Frequency (CPS)} = \frac{1}{\text{Time (seconds)}}$$

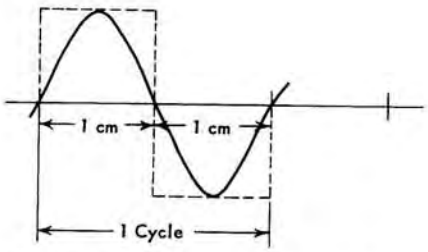


Figure 30. Frequency Measurement

Wire-Wrap

Wire-Wrap is a method of making solderless wire connections to terminals. A special Wire-Wrap tool wraps a length of skinned wire tightly around the square corners of a terminal. The resulting connection is one of the most reliable permanent connections available and is readily adaptable to production line manufacturing. Power tools for making Wire-Wrap connections are available as branch office tools to offices having installed systems that use Wire-Wrap terminal connections.

Wire-Wrap Tool

The Wire-Wrap tool is, basically, a metal rod containing two holes: a small hole for receiving the skinned wire, and a larger hole for receiving the terminal (Figure 31). The metal rod is called the wrapping bit. The skinned wire is placed in the wrapping bit. The bit is placed on the terminal and rotated, forming a tightly wrapped coil of wire around the terminal.

The Keller Wire-Wrap tool has an electric motor that drives a wrapping bit. The wrapping bit turns within a sleeve that contains a wire anchoring notch on each side. The notch holds the insulated portion of the lead to prevent the insulation from wrapping around the terminal.

The tool consists of: an electrically operated pistol tool, wrapping bits, and sleeves for the various wire sizes (Figure 32). The pistol tool, P/N 461012, is equipped with a 20 foot, three wire grounding cord.

Wrapping bits and sleeves for use with the above gun are as follows:

WIRE SIZE	WRAPPING BITS		SLEEVES	
	IBM P/N	KELLER P/N	IBM P/N	KELLER P/N
26 GA.	461008	A-24255	461014	17611-2
24 GA.	461009	A-17612-2	461014	17611-2
22 GA.	461010	A-18632	461015	18840
20 GA.	461011	A-18633	461016	18285

Wire-Wrap Procedure

1. Select the bit and sleeve for the wire size to be used.
2. Install bit and sleeve in the nose assembly of the power tool as follows:
   a. Loosen the collet nut on the nose assembly.
   b. Insert the wrapping bit into the collet. Rotate the bit while applying slight pressure against the end until it seats itself. (NOTE: To remove the bit, reverse this process.)
   c. Place the sleeve over the bit and into the collet. Rotate until sleeve is seated and positioned. With tool running apply slight pressure to the end of the sleeve and tighten collet nut.
3. Skin the wire to desired length. The length of the skinned wire determines the number of turns of wire on the terminal. For example: when using 24 gage wire, about ¼ inch bare wire is required for each turn. Because six turns are required for an acceptable connection, the skinned length should be 1½ inches.
4. Insert the skinned wire into the small hole of the wrapping bit (Figure 33a) taking care to insert the wire up to the insulation. Do not bend the skinned portion of the wire; it may be difficult to slide into the bit.

   WARNING: If the wire is not inserted in the wrapping bit up to the insulation, a shiner (bare wire between insulation and terminal) may result. There should be ¼ to ¾ of a turn of insulation at the beginning of each wrap.
5. Hold the wire with the fingers and bend the insulated portion of the lead into the retaining notch in the sleeve (Figure 33b). Use the right or left notch as determined by the direction of the approach (or exit) of the lead. Place the wrapping bit on the terminal. Be sure the terminal is inserted into the bit as far as it will go. Use reasonable care to hold the tool in line with the terminal.
6. Hold the tool on the terminal and squeeze the trigger to wrap the wire on the terminal. The tool will automatically recede as the wire coils on the terminal. Release trigger and remove tool from terminal. The Wire-Wrap connection is complete (Figure 33c).

NOTE: If too much pressure is used to push the tool on the terminal, a turn of wire may wrap over a previous

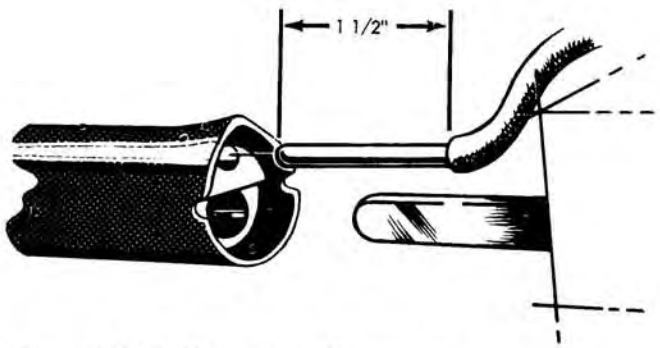


Figure 31. End of Wire-Wrap Wrapping Bit

Figure 32. Wire-Wrap Tool

FIGURE 33a

FIGURE 33b

FIGURE 33c

Figure 33. Wire-Wrap Procedure

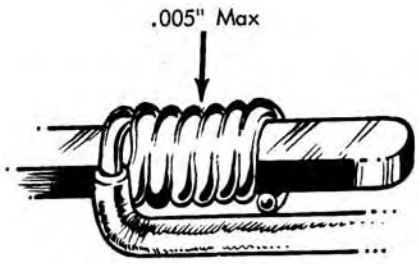


Figure 34. Wire-Wrap Connection

turn. If too little pressure is exerted, the adjacent wraps of wire may not touch each other. Maximum separation between individual turns on the terminal must not exceed .005" excluding the first and last wrap (Figure 34).

Removal of Wire-Wrap Connections

Wires may be removed from a terminal by using hand unwrap tool, P/N 461013 (Figure 35). The open end of the tool is placed over the terminal and rotated to the left screwing the tool under the wraps of wire.

WARNING: Once a wire is removed from a terminal, it may not be rewrapped. A new wire must be used or a new section of wire must be spliced to the existing wire.

A good quality splice may be made with a butt connector, P/N 216230 (Figure 36). Strip ⅛ inch of insulation from the wire, insert the wire into the butt connector, and crimp with Bare Wire Crimping Tool, P/N 450898.

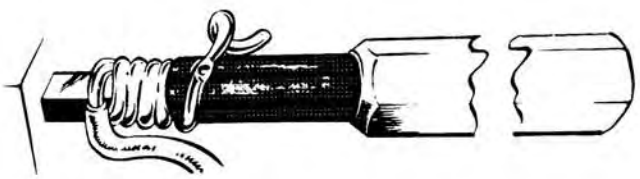


Figure 35. Hand Unwrap Tool, P/N 461013

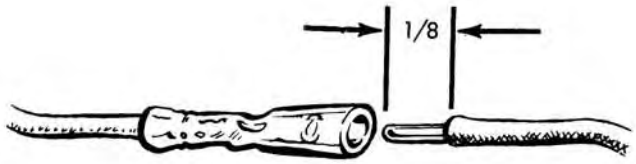


Figure 36. Butt Connector, P/N 216230

Service Aids

Tailgate Connector

Two gate assemblies, called tailgates, are in the rear of the frame. The tailgates are identified as gate E (top) and gate F (bottom). Two types of coaxial block connectors are used in the tailgate. One type is a 20-position connector; the other, a 40-position connector. These connectors are illustrated in Figure 6.

Make sure that all pins are clean and straight and that the latch is fully engaged, when trouble is suspected with a tailgate connector.

To attach terminals for use in the 40-pin block (biscuit) connectors, proceed as shown in Figure 37. To attach terminals for use in the 20-position coaxial block (biscuit) connectors, proceed as shown in Figure 38.

Ventilating System

The ventilating system has three parts: motor, blower, and filter. Figure 39 shows a typical motor-blower assembly.

MOTOR

The ventilating system motor is a 3-phase, 230-volt, 60-cycle induction motor. The speed is 3400 RPM at 1/30 HP.

The motor is wired with color coded four-wire lead: blue for phase 1, black for phase 2, red for phase 3, and

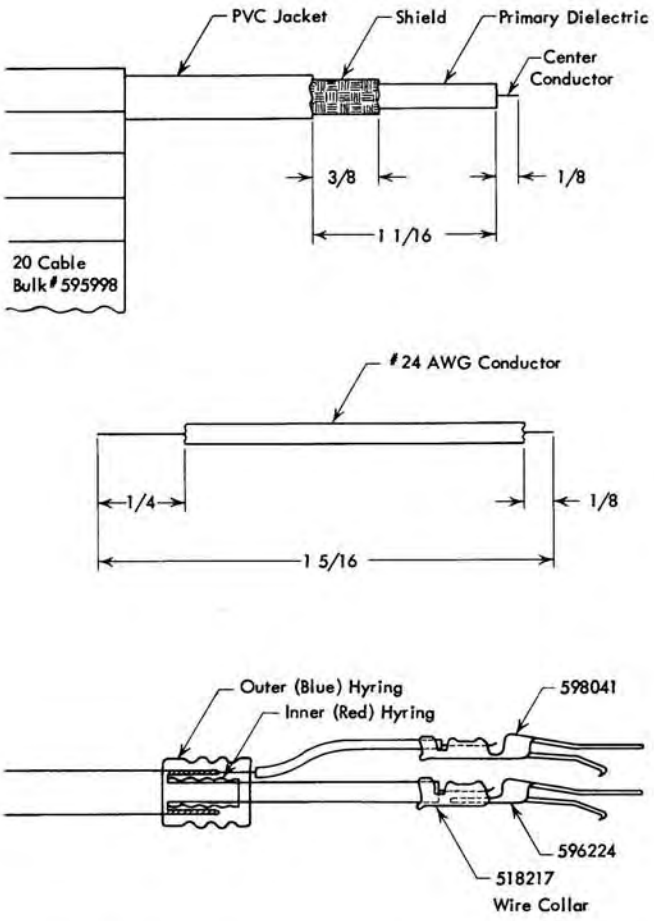


Figure 37. Attaching 40-pin Connector Terminals

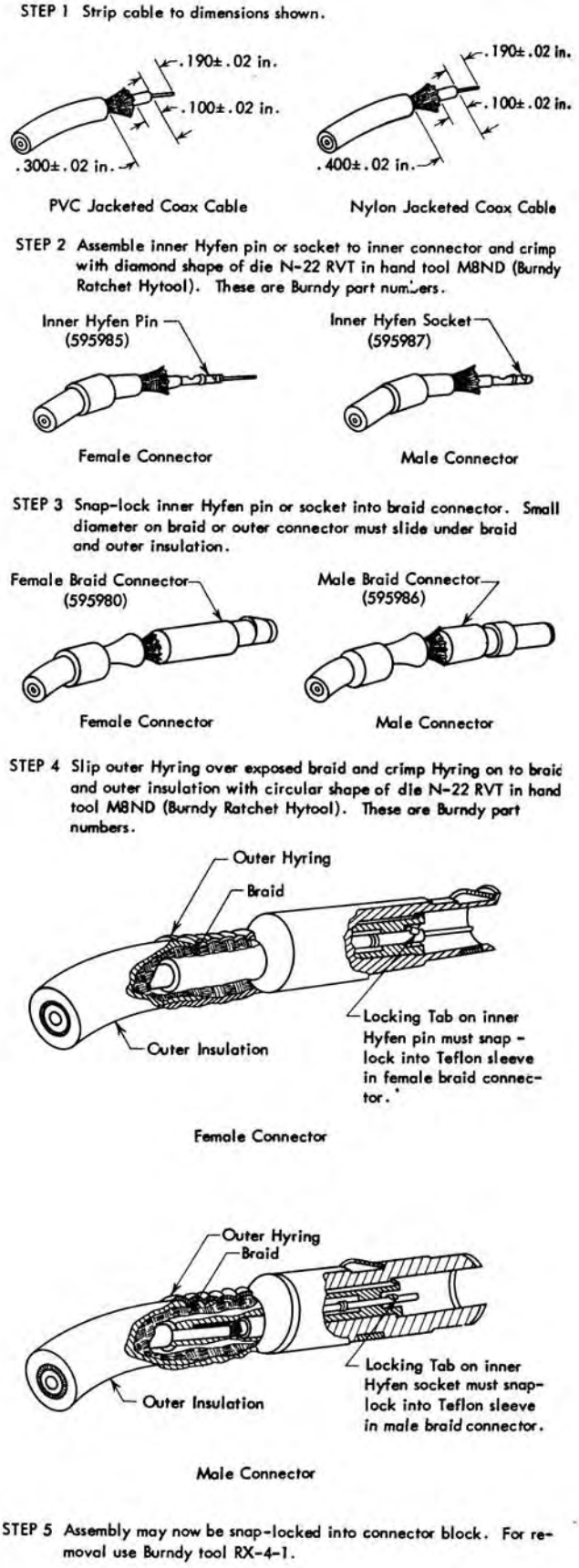


Figure 38. Attaching Coaxial Connector Terminals

green for ground (grounded to the motor frame). When viewed from the lead end of the motor, rotation is counterclockwise when the phase sequence is 1-2-3.

When the motor is first installed, check for correct rotation (counterclockwise when viewed from the hinged end of the gate). Inspect the motor for excessive noise, heat, or vibration. Motor bearings are sealed and require no periodic lubrication. Motor mounting bolts must be tight to insure proper alignment between the motor and blower shafts.

To remove the motor: turn power off; then open the gate as far as possible. Take out the filters, remove the motor wire connections, and loosen the setscrew in the coupling on the motor shaft. Remove the motor mounting bolts and lift the motor from the frame. To replace the motor, reverse the removal procedure.

Blowers

Seven scroll, squirrel cage type blowers are used in the ventilating system (Figure 40).

Check at the top of the frame for good air flow through the gates. Check for excessive noise or vibration. Blower bearings are sealed and require no periodic lubrication. All eight 8-32 mounting bolts must be tight to insure correct alignment of the blower and motor shafts.

To remove the blowers: turn power off; then take out the filters and remove the setscrew in the coupling on the blower shaft. Remove the eight mounting bolts and lower the unit beneath the frame to the floor. Carefully slide the assembly from under the frame.

To replace a blower assembly, reverse the removal procedure. The unit has seven blowers mounted on a common shaft; care must be taken during installation so that no physical damage comes to either the blowers or the shaft.

Filter

The ventilating system uses aluminum impingement type filters. Two filters are used for each motor-blower assembly.

Change filters periodically as specified in the scheduled maintenance routine card. If the filters appear to require changing more or less often than specified, note this change on the scheduled maintenance routine card. Insert the filter in the grooved metal holder properly to eliminate unnecessary noise.

To change filters: turn power off; then slide the old filter forward out of the metal holder on the bottom of the frame. The filters bend easily; when sliding in a new filter, use care not to damage it.

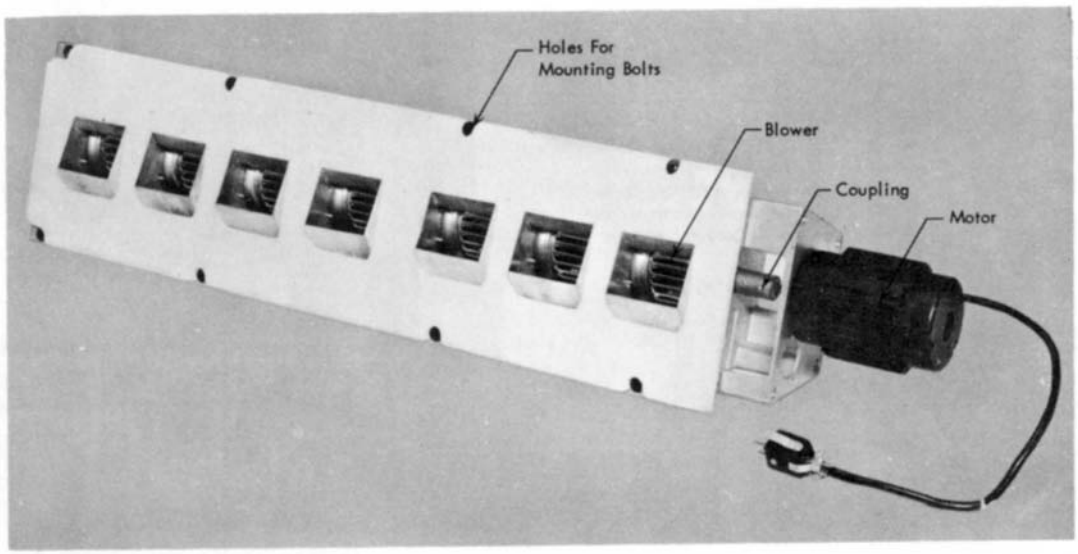


Figure 39. Motor-Blower Assembly

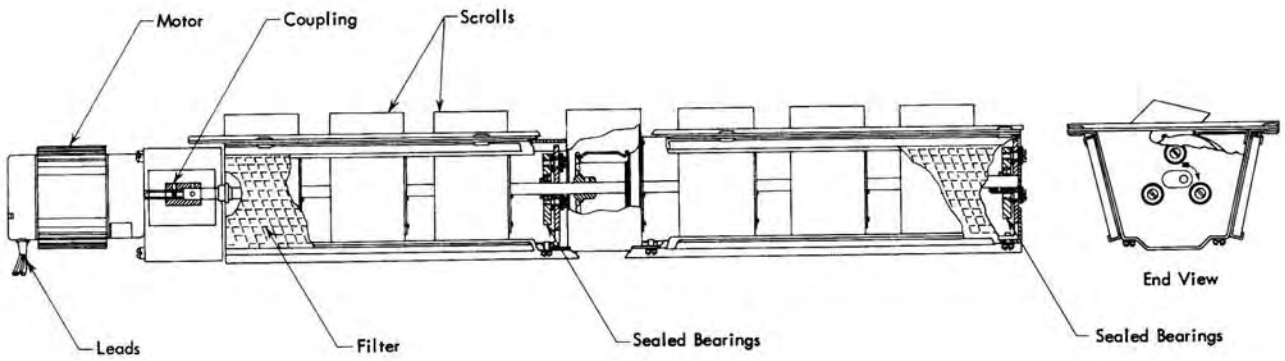
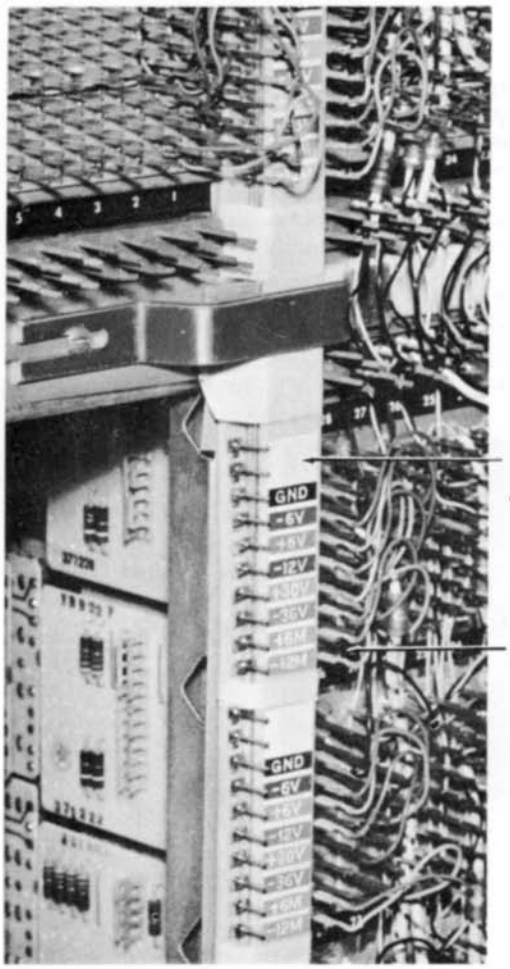


Figure 40. Motor-Blower Details

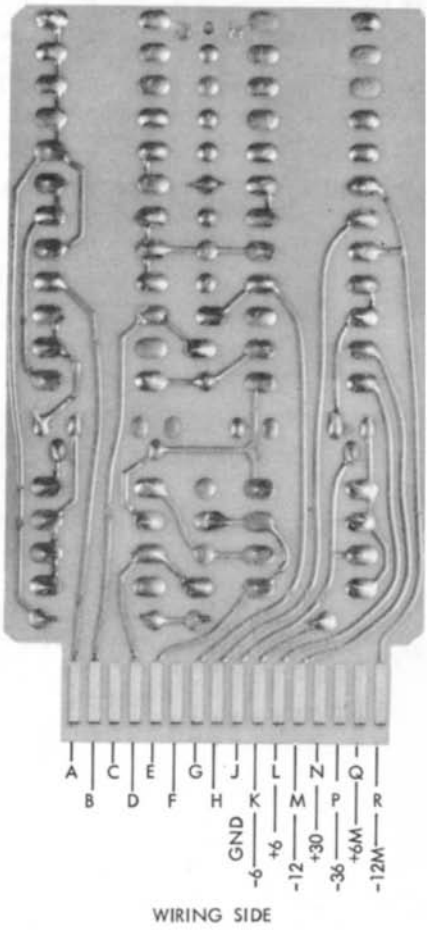
Voltage Distribution



Laminar Bus Consists of Layers of Copper Strips Separated by Mylar* Insulation.
*Trademark of E. I. du Pont de Nemours & Co. (Inc.)

Terminals for Attaching Spring Crimped Connectors from Laminar Bus to Card Receptacles

Laminar Bus Power Distribution



Voltage Contact Assignment to Typical SMS Card

Service Wiring Standard Color Code

VOLTAGE	WIRE COLOR CODE	VOLTAGE	WIRE COLOR CODE	VOLTAGE	WIRE COLOR CODE
+82 IND	Red	+12M	White	-12	Violet
+60	White, red tracer	+6	Orange	-12M	Aqua
+48	White, black tracer	+6M	Tan	-18 IND	White, brown tracer
+30	Pink	Ground	Black	-20	White, violet tracer
+30M	Pink, black tracer	-6	Blue	-36	Brown
+12	Gray	-6 Sp	White, blue tracer	-48	White, orange tracer

Component Color Codes

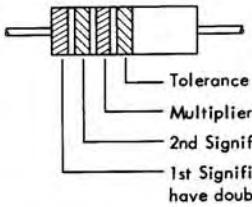
Color	First Ring - 1st Figure	Second Ring - 2nd Figure	Third Ring - Multiplier
Black	0	0	None
Brown	1	1	0
Red	2	2	00
Orange	3	3	000
Yellow	4	4	0,000
Green	5	5	00,000
Blue	6	6	000,000
Violet	7	7	0,000,000
Gray	8	8	00,000,000
White	9	9	000,000,000

NOTE: A fourth colored ring on resistors determines tolerance ratings as follows:

Gold = ± 5 %
Silver = ± 10 %

Absence of a fourth colored ring indicates ±20% tolerance.

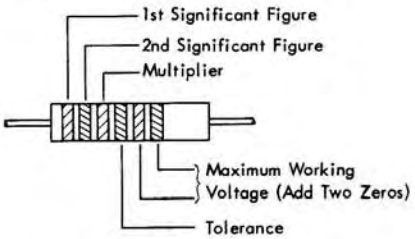
AXIAL LEAD RESISTOR



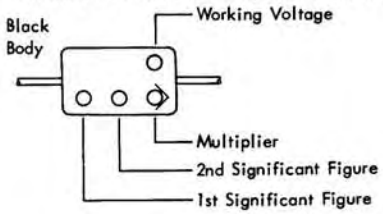
Resistor wattage rating is determined by physical size. However, resistors most commonly used at IBM are one-half watt and higher rated; resistors are progressively larger.

MOLDED PAPER TYPE CAPACITORS

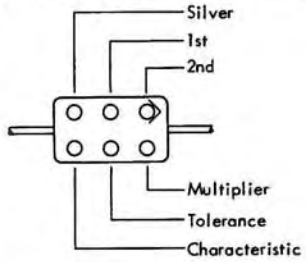
TUBULAR TYPE



MOLDED FLAT CAPACITOR (Commercial Code)



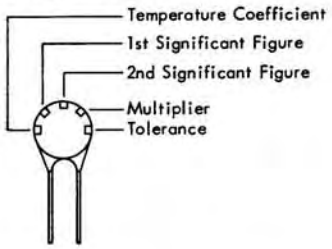
MOLDED FLAT CAPACITOR (JAN Code)



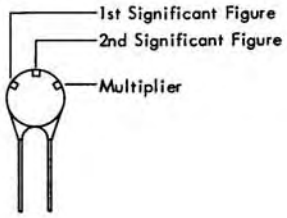
NOTE 1: Unless otherwise specified, the maximum working voltage rating of capacitors is obtained by multiplying the capacitor body color code value by 100.

NOTE 2: The tolerance rating of capacitors is determined by the color code value in percent. For example, Green equals ±5%.

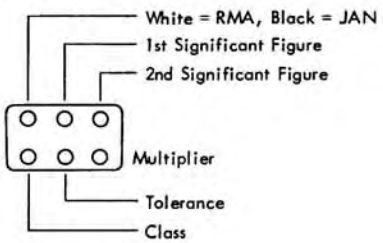
DISK TYPE CERAMIC CAPACITORS



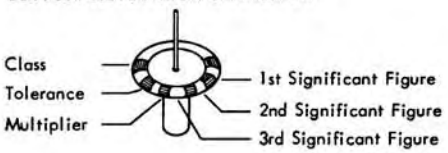
FIVE DOT DISK TYPE CERAMIC CAPACITOR



MOLDED MICA TYPE CAPACITORS



BUTTON SILVER MICA CAPACITOR



General Usage	Manufacturing Process	Form	IBM Type No.	IBM P/N	Circuit Application *	Notes
Logic	Alloy Junction	PNP	01	345741	VM (S)	
			02	345742	VM (NS)	
			13	344892	CS (NS)	1
			25	318322	CS, CTRL, CTDL(S) (NS)	2
			29	492451	CTDL(S)	
			33	318324	CS, CTRL, CTDL(S) (NS)	3
			34	535009	CTDL(S)	
		NPN	51	345747	VM (S)	
			52	345748	VM (NS)	
			63	344891	CS (NS)	6
			75	318323	CS, CTRL, CTDL(S) (NS)	7
			83	318325	CS, CTRL, CTDL(S) (NS)	8
	Diffused Junction	PNP	15	526797	CS (NS)	
			16	526880	CS (NS)	
			18	347592	CS (NS)	
		NPN	65	526798	CS (NS)	
			66	526881	CS (NS)	
			68	347593	CS (NS)	
Special Purpose	Power Drivers	NPN	04	345744	(S) Line Driver	
			06	345745	(S) Sense Amplifier	
			12	340709	(S) 48v Relay Driver	
			14	345763	(S) 45v Neon Driver	
			20	526795	(S) 25v Line Driver	
			21	526796	(S) Read-Write Driver	
			22	526898	(S) Prolay and Power Driver	4
			23	526899	(S) 48v Relay Driver	5
			26	535441	(S) 20v Relay Driver	
		NPN	71	492450	(S) Slow Speed Core Driver	
	Diffused Junction (Medium) (Power) Drivers	NPN	88	369558	(NS) Core Memory Driver	
			89	369559	(NS) Core Memory Driver	
			91	369561	(S) Shift Register and Drum Driver	
			92	369562	(S) Shift Register and Drum Driver	
			93	369560	(NS) Core Memory Driver	

* Circuit Application
VM - Voltage Mode
CS - Current Switching
CTRL- Complementary Transistor Resistor Logic
CTDL- Complementary Transistor Diode Logic
(S) - Saturating
(NS)- Non-saturating

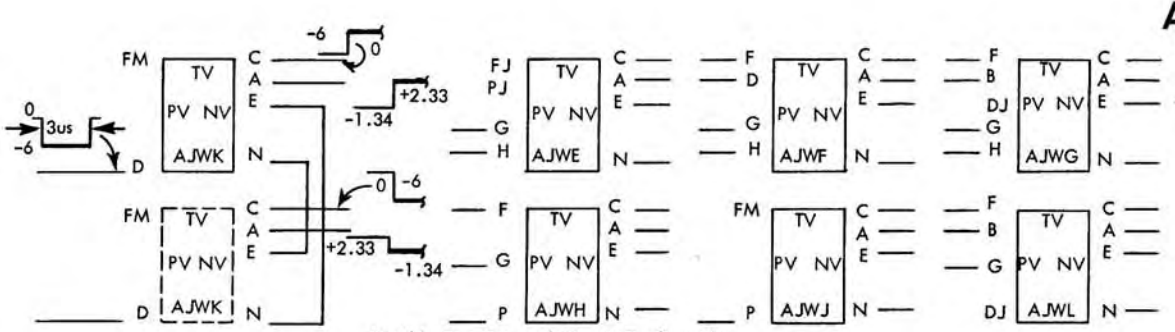
Notes:
1. Type 13 can be used for type 33 or 25
2. Type 25 cannot be used for type 33
3. Type 33 can be used for type 25
4. A Delco 2N174 can be used for type 22
5. A Philco 1229 can be used for type 23
6. Type 63 can be used for type 83 or 75
7. Type 75 cannot be used for type 83
8. Type 83 can be used for type 75

Diode Specifications

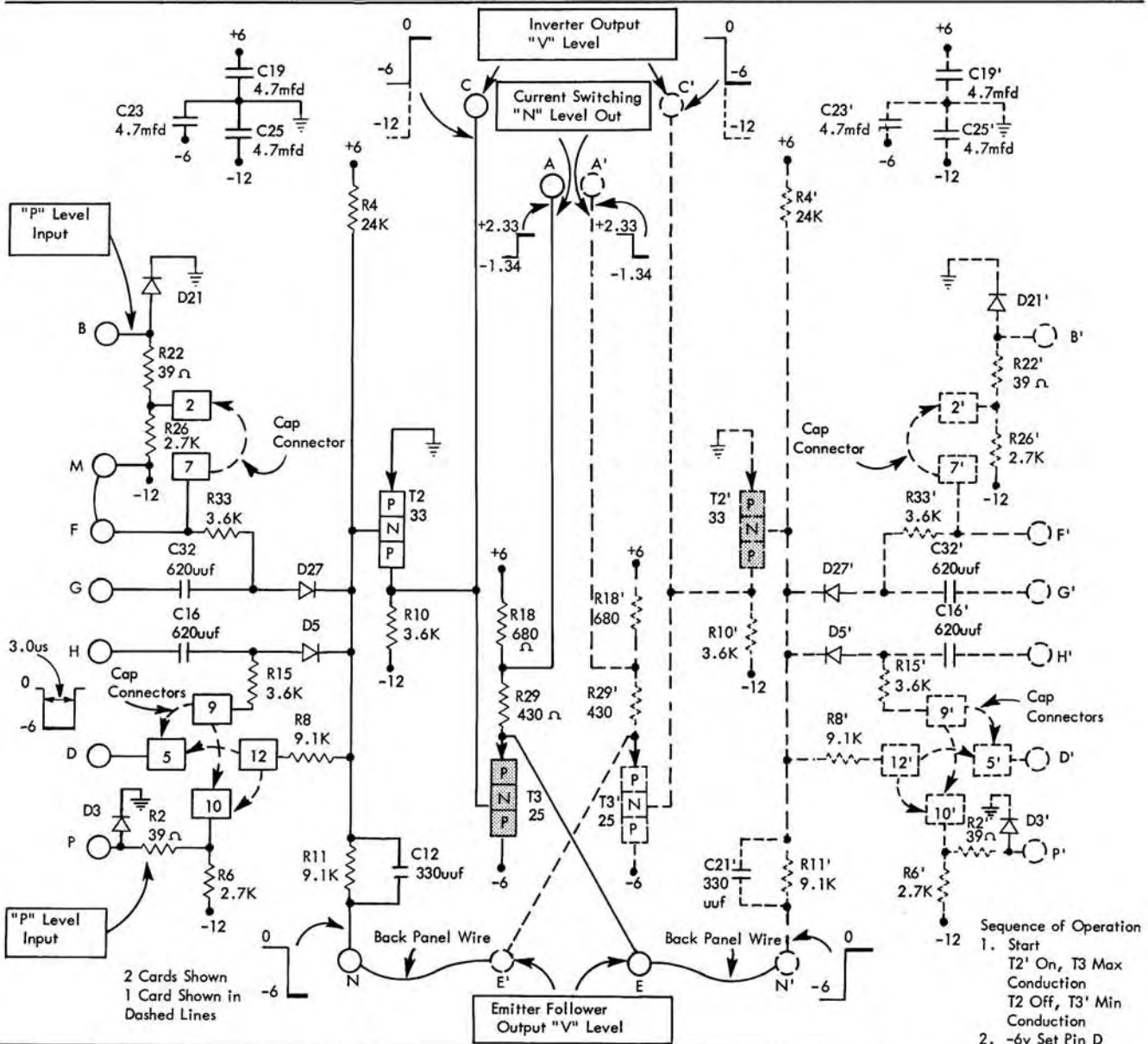
Type	IBM P/N	Type of Crystal	Maximum Forward Voltage Drop @ 25°C		Reverse Leakage Current @ 55°C		Reverse Recovery Time* (usec) @ 25°C
			E_F(v)	I_F(ma)	E_B(v)	I_L(ua)	
AAs	491008	Ge	0.4	5.0	15.0	75.0	0.5-4.0
AFs	492431	Ge	1.0	25.0	100.0	100.0	
AGs	492457	Ge	0.5	5.0	50.0	125.0	
ALs	2106333	Si	1.5	100.0	100.0	100.0	
AN	491007	Ge	1.0	3.0	15.0	150.0	
AR	419214	Si	1.1	200.0	50.0	75.0	
AS	491281	Ge	0.4	3.0	15.0	25.0	0.5
AU	491300	Si	1.0	100.0	40.0	10.0	1.5
Fs	503591	Ge	1.0	5.0	50.0	125.0	0.5-3.5
Gs	503592	Ge	1.0	5.0	50.0	250.0	0.5-3.5
Js	492430	Ge	1.0	200.0	10.0	100.0	4.0
M	334908	Ge	1.0	40.0	10.0	20.0	4.0
P	333264	Ge	0.5	100.0	65.0	1200.0	
R	504361	Ge	1.0	40.0	10.0	20.0	4.0

* Recovery time is the time necessary for the diode to stop conducting after it has been passing current in the forward direction.

AJWE
WF
WG
WH
WJ
WK
WL



Possible Cap Cuts and Circuit Configurations



Sequence of Operation

1. Start
   T2' On, T3 Max Conduction
   T2 Off, T3' Min Conduction
2. -6v Set Pin D
   T2 On, T3 Min Conduction
   T2' Off, T3' Max Conduction

Input						Levels		Output Levels					
AC Set		Gating				DC Set		Emitter Follower		Inverter		"N" Level	
Min	Max	Current Mode		Votlage Mode		Current Mode	Voltage Mode	Min	Max	Min	Max	Min	
		Min	Max	Min	Max								
2.6	Limited only by Gate Level and Reverse Bias Spec of Transistor	(ma) 4.82 / 0.186	7.3 / 0	+0.35 / -0.2 / -5.56	-12.48	$I_{IN} \leq$ 7.3ma $I_{IN} \geq$ 4.82 ma for set Operation	-0.2 / -5.56	-0.2 / -5.56	+0.35 / -6.24	-0.2 / -5.56	0 / -6.24	+2.05 / -0.42	

Voltage Mode Trigger 3

The AJ-- card consists of one inverter and one emitter follower connected to form half of a voltage mode trigger. Two cards are required to form a trigger that may serve as an isolated binary bit memory or may be used in a clock or ring circuit. By use of cap cuts, the basic card may be varied to provide seven different input configurations. Each of the seven different cap cut configurations, may then be backpanel wired to provide varied input and output applications. The following data show the relationship between part number, cap cut coding, cap connections, and input configurations.

Card and Cap Type	Part Number	Cap Connection	AC Sets	Input CM Gates	Input VM Gates	Types VM DC Set	Types CM DC Set
AJWE	371424	2 to 7 9 to 10	2	2	1	0	0
AJWF	371423	5 to 9	2	0	2	0	0
AJWG	371422	2 to 7 5 to 9	2	1	2	0	0
AJWH	371421	10 to 12	1	0	1	0	1
AJWJ	371420	2 to 7 10 to 12	1	1	1	0	1
AJWK	371419	5 to 12	1	0	1	1	0
AJWL	371418	2 to 7 5 to 12	1	1	1	1	0

In-phase and out-of-phase V level and N level outputs are available from this trigger. This trigger circuit operates at a frequency near 200KC.

Binary Operation: The trigger may be operated in a binary state by connecting the gate resistors to the emitter follower output on the same side of the trigger and connecting the AC inputs together to the output of a sample pulse driver.

AC Set Input: There are two gated AC sets per state (pins G and H) and either AC set may be gated by current mode (pins B and P) or voltage mode gating (pins D and F). The AC set pulse may be either a 3v or a 6v positive shift with a minimum rise rate of 2.6v in 0.9μs and a minimum pulse duration of 0.5μs.

The following data show levels and timings for gated operation:

AC Set	VM Gating	CM Gating	Gate Condition Time	Minimum Gate Level
3v	−12.48v		7.0μs	−.5v
3v	−6.2v		5.5μs	−.5v
6v	−12.48v		4.0μs	−2.0v
6v	−6.2v		3.0μs	−2.0v
6v		6.0ma	5.0μs	4.8ma

DC Set Input: A negative signal of −5.56v minimum and −12.48v maximum applied to the VM DC set (pin D) input triggers the circuit. A current mode signal of 4.82ma minimum and 7.3ma maximum applied to the DC current mode input (pin P) also triggers the circuit. The pulse duration for voltage mode DC set is 3.0μs.

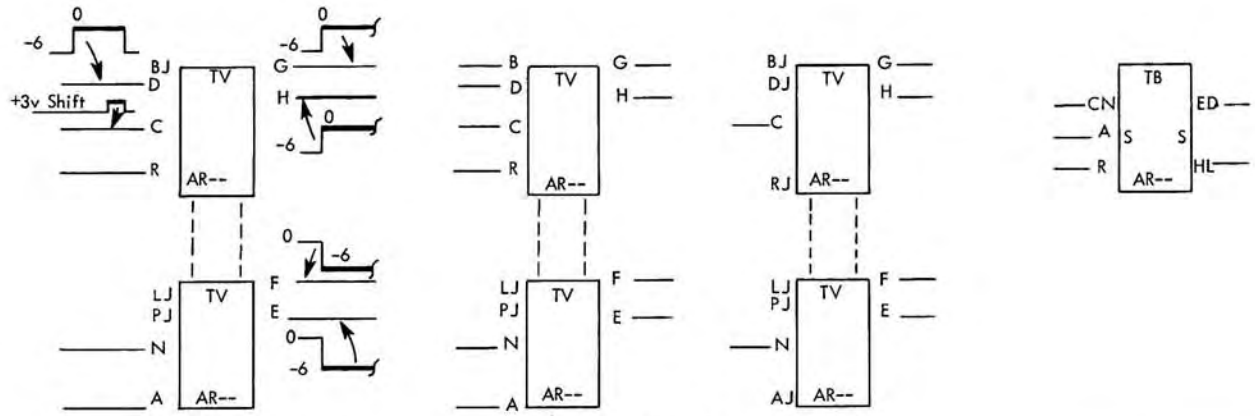
Circuit Description

Assume a starting condition of T2′ conducting, T3 in maximum conduction, T3′ in minimum conduction, and T2 off. With a 0v to −6v negative signal of at least 3.0μs duration on pin D, the base of T2 is forward-biased and goes into full conduction. The inverter output of T2 (pin C) rises from −6v to 0v. This voltage rise from −6v to 0v is fed to the base of T3, reducing its forward bias, and causing reduced current through the emitter follower T3. The reduced current through the emitter follower T3 allows its output to rise from −6v to 0v (pin E) and reverse bias T2′. T2′ is turned off because of the reverse bias, and its collector output tries to go to −12v. Because the base of the emitter follower T3′ is tied to the collector of T2′ and because the collector of T3′ is connected to −6v, the diode action between the collector and base of T3′ clamps the output of the inverter T2′ to −6v (pin C′). T3′ goes into full conduction, and because the emitter output of the emitter follower T3′ follows the base, its output (pin E′) goes from 0v to −6v. The current mode outputs (pins A and A′) follow the emitter follower outputs (pins E and E′) in proportion to the resistor divider networks and the loads that they are connected to. A negative pulse applied to pin D′ flips the trigger to its original state.

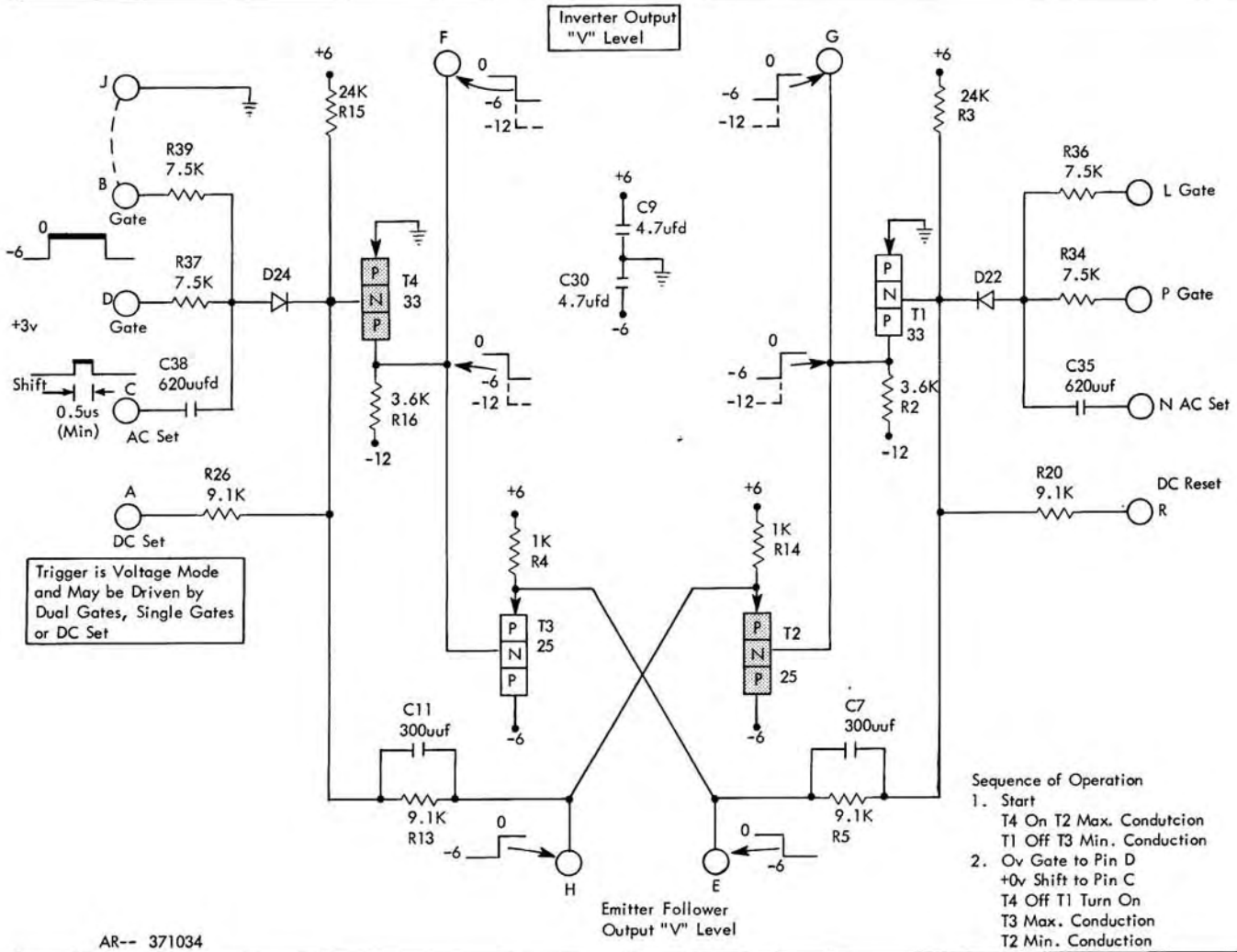
The maximum turn-on delay is 0.8μs and the minimum turn-on delay is 0.3μs. The maximum turn-off delay is 0.54μs and the minimum turn-off delay is 0.14μs.

Application

This circuit is used mainly for register and ring applications. Various logic block configurations and the seven cap cuts are shown.



Possible Logic Block Configurations



Sequence of Operation

1. Start
   T4 On T2 Max. Condutcion
   T1 Off T3 Min. Conduction
2. Ov Gate to Pin D
   +0v Shift to Pin C
   T4 Off T1 Turn On
   T3 Max. Conduction
   T2 Min. Conduction

AR-- 371034

Input Levels						Output Levels				Delays (Usec)				
AC Set		Gate		DC Set		Emitter Follower		Inverter			Trigger		Gate Condition Time	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		Min	Max	Min	Max
2.6v / 3.8v		-0.2 / -5.56	+0.35 / -12.48	-0.2 / -5.56	0 / -12.48	-0.2 / -5.56	+0.35 / -6.24	-0.2 / -5.56	0 / -6.24	Turn On	.30	.80	3.0	7.5
										Turn Off	.14	.54	—	—

The AR - - card consists of a voltage mode trigger circuit designed for use in clock and ring circuits and as an isolated binary bit memory. The trigger circuit uses two inverters and two emitter followers and operates at a frequency near 150KC. The trigger may be connected to be operated by many input configurations. It may be operated as a binary input, a single gated AC input, a dual gated AC input, or a DC set input. Both in-phase and out-of-phase outputs are available from this card.

Binary Operation: The trigger may be connected for binary operation (gated or not gated) by connecting one of the gate resistors to the emitter follower output on the same side of the trigger. The other gate input may be then used as an external gate or tied to ground. The two AC inputs are connected together and driven from a sample pulse driver to form the binary operation.

AC Set Input: For gated input operation, the AC set pulse may be either a 3v or a 6v positive shift with a minimum rise rate of 2.6v in 0.9μs and a minimum up duration of 0.5μs. The following data show the input shifts and the time required to condition the gates (The gates have to be at about ground level for a 3v AC input shift to flip the trigger.).

AC Set Input	Gate 1	Gate 2	Gate Condition Time	Minimum Gate Level
3v	−12.48v	−12.48v	7.5μs	−0.5v
3v	−12.48v	GND	6.0μs	−0.5v
3v	−6.2v	−6.2v	6.0μs	−0.5v
3v	−6.2v	GND	4.5μs	−0.5v
6v	−12.48v	−12.48v	4.5μs	−2.0v
6v	−12.48v	GND	3.0μs	−2.0v
6v	−6.2v	−6.2v	3.0μs	−2.0v

DC Set Input: A signal of −5.56v (or more negative) applied to the DC set input triggers the circuit. The negative set signal may go as far negative as −12.48 volts. The down input pulse must be at least 3.0μs in duration.

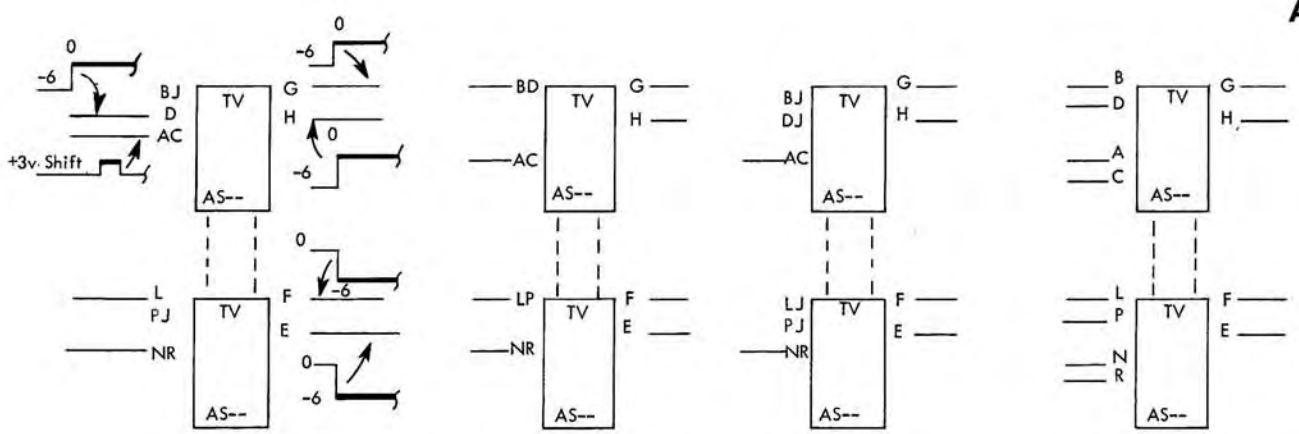
Circuit Description

Assume a starting condition of T4 and T2 in full conduction, T3 at minimum conduction, and T1 off. With one gate (pin B) tied to ground (pin J) and the other gate (pin D) gated from −6v to 0v for 4.5μs before the AC input shift is applied, a positive going 3v pulse of 0.5μs is applied to the AC set input (pin C). The output of the gate at D24 causes the base of T4 to become more positive than the emitter (ground potential). T4 becomes reverse-biased off and its collector voltage tries to go to −12v. Because of the diode action between the collector and base of T3, the collector of T4 is allowed to go only to −6v (pin F). This negative −6v forward biases T3 into full conduction. The emitter of the emitter follower (T3) follows the base to −6v. The output of the emitter follower (pin E) is coupled to the base of T1 through the voltage divider R3 and R5, forward biasing T1. The conduction of T1 causes its collector (pin G) to rise from −6v to 0v. This T1 collector voltage rise to 0v is fed to the base of T2 and reduces the forward bias of T2. The reduced bias on the emitter follower (T2) reduces its conduction so that its emitter rises to 0v. The emitter output of T2 (0v) at pin H is coupled back to the base of T4 and holds reverse bias on T4, thus providing latch back to the circuit. If gating of pins L and P and an AC set pulse to pin N are applied, the trigger is flipped to its original state.

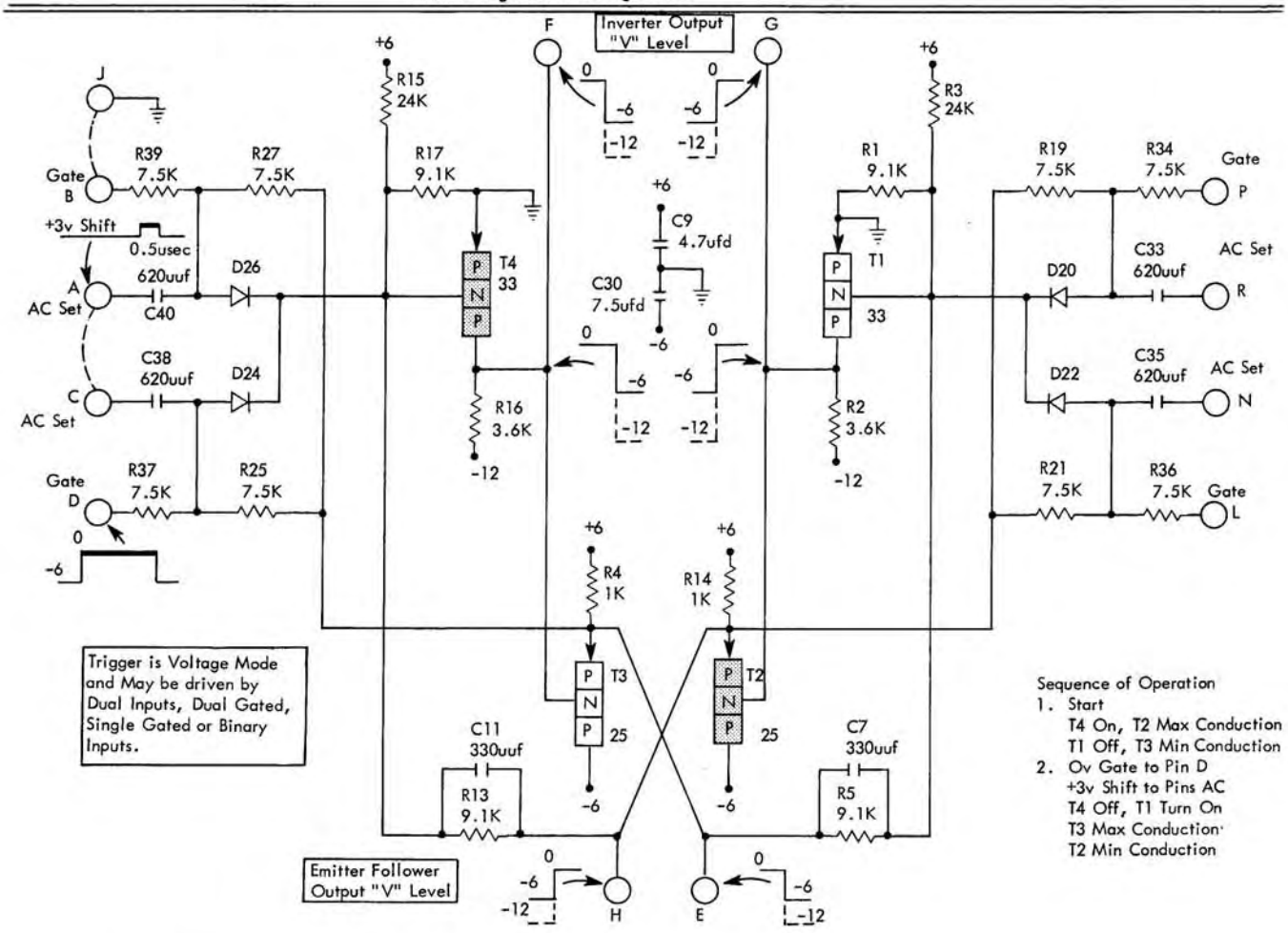
The turn-on and turn-off delays are a function of circuit loading.

Application

This circuit is used mainly for ring and register applications. Various logic block configurations for the trigger circuit are possible; some of these configurations are shown.



Possible Logic Block Configurations



AS-- 371035

Input Levels				Output Levels				Delays (usec)				
AC Sets		Gates		Emitter Follower		Inverter			Trigger		Gate Condition Time	
Min	Max	Min	Max	Min	Max	Min	Max		Min	Max	Min	Max
2.6v / 3.8v		-0.20 / -5.56	+0.35 / -12.48	-0.2 / -5.56	+0.35 / -6.24	-0.2 / -5.56	0 / -6.24	Turn On	.10	.30	3.0	6.0
								Turn Off	.14	.54		

The AS - - card consists of a voltage mode trigger circuit designed for use in clock and ring circuits and as an isolated binary bit memory. The trigger circuit uses two inverters and two emitter followers and operates at a frequency near 150KC. The trigger may be connected to operate in many configurations. It may be operated as a binary input or AC set input. Two AC set inputs per state are available. Both in-phase and out-of-phase outputs are available from this card.

Binary Operation: The trigger may be connected for binary operation (gated or non-gated). When it is used as a non-gated trigger, the gate inputs are tied to ground, and the AC set inputs are tied together and driven by a sample pulse driver.

AC Set Input: For gated input operation, the AC set pulse may be either a 3v or a 6v positive going pulse with a minimum shift of 2.6v in 0.9μs and a minimum up duration of 0.5μs. Because there are two AC set gates per state in this circuit, the trigger can be driven from either gate input as gated or non-gated, or the gates may be connected together and operated as a single AC set input. The following data show levels and timings for gated AC input operation:

AC Set Input	Gate 1	Gate 2	Gate Condition Time	Minimum Gate Level
3v	−12.48v	GND	6.0μs	−0.5v
3v	−6.2v	GND	4.5μs	−0.5v
6v	−12.48v	GND	3.0μs	−2.0v

Circuit Description

Assume a starting condition of T4 conducting, T2 in maximum conduction, T1 off and T3 in minimum conduction). When triggering only one capacitor input (pin C), pin D has to be gated from −6v to 0v for 4.5μs (minimum) before the positive going 3v pulse of 0.5μs is applied to the AC set input (pin C). The output of the gate at diode D24 causes the base of T4 to become more positive than the emitter (ground potential). T4 becomes reverse-biased off and its collector voltage tries to go to the −12v. Because of the diode action between the collector and base of T3, the collector of T4 is allowed to go only to −6v (pin F). This negative −6v forward biases T3 into full conduction and its emitter follows the base to −6v. The output of the emitter follower T3 (pin E) is coupled to the base of T1 by voltage divider R3 and R5 and forward biases T1 (−6v). Conduction of T1 causes its collector (pin G) to rise from −6v to 0v. This 0v at the collector of T1 is fed to the base of T2 and reduces the forward bias of T2. The reduced forward bias of T2 reduces its conduction so that the emitter of T2 (pin H) rises to 0v. The 0v output of T2 is coupled back to the base of T4 and holds reverse biasing on T4, providing latch back to the circuit. If gating of pins L or P and an AC set to pins N or R is applied, the trigger is flipped to its original state.

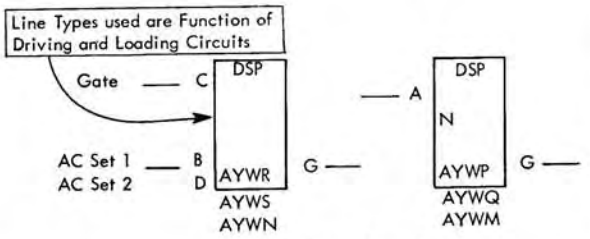
AC set inputs A and R and their respective gates B and P provide additional possible means of flipping the trigger. By use of both AC sets per state (pins A and C and pins R and N), bidirectional counters and registers can be constructed.

Turn-on and turn-off delays are a function of circuit loading.

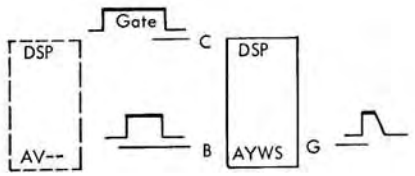
Application

This circuit is used mainly for counter and register applications. Various logic block configurations for the trigger circuit are possible and some of the configurations are shown.

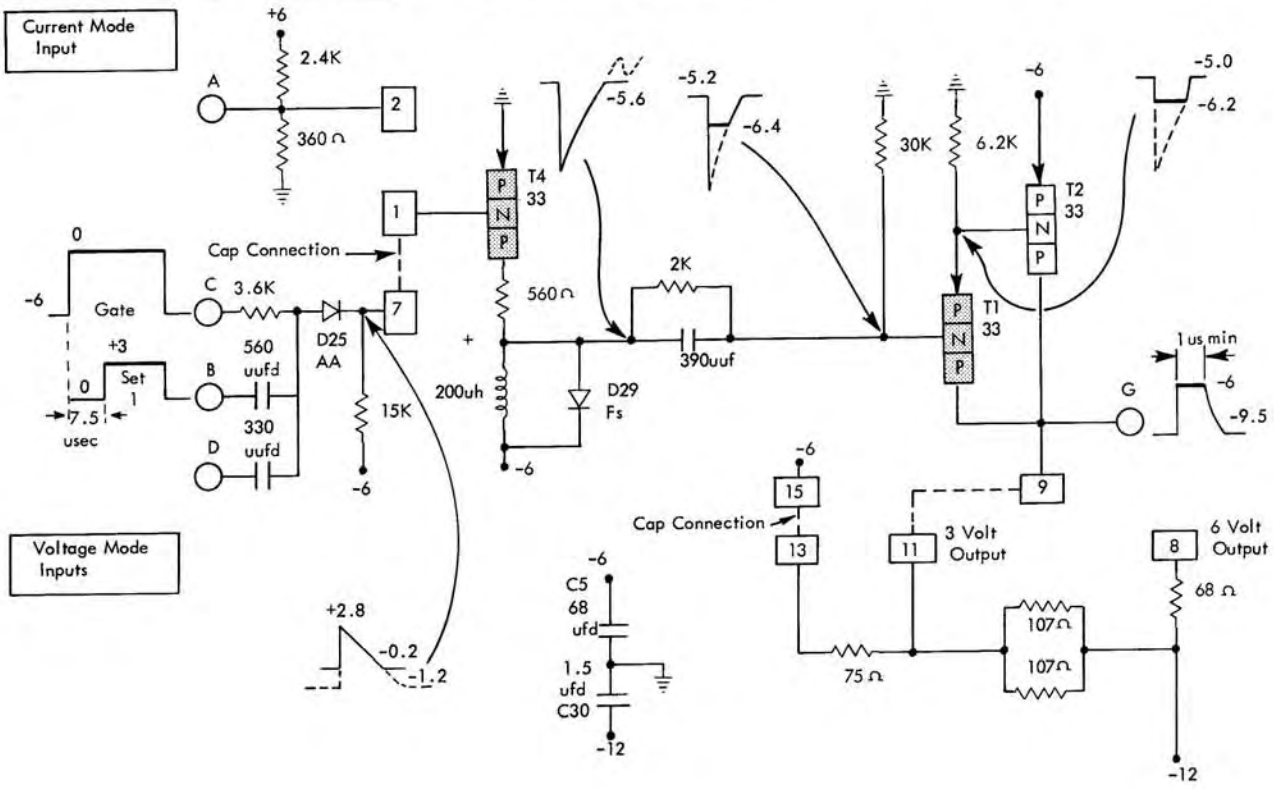
AYWM
WN
WP
WQ
WR
WS



Possible ALD Configurations



Logic Application



Card Code	Part No.	Cap Connections Used	Coupling Input Used	Collector Loading
AYWM	371426	1 to 2	CM	None
AYWN	371425	1 to 7	VM	None
AYWP	371044	1 to 2 9 to 8	CM	Yes(6v)
AYWQ	371043	1 to 2 9 to 11 13 to 15	CM	Yes (3v)
AYWR	371042	1 to 7 9 to 8	VM	Yes (6v)
AYWS	371041	1 to 7 9 to 11 13 to 15	VM	Yes (3v)

Input Waveforms		Min	Max	Max Rise Time	Repetition Rate(Max)
Voltage Mode Inputs	Gate Pin C	-0.2 -5.56	0 -12.48	—	—
	AC Set 1 Pin B	2.6v	3.4v	1.0us for 2.6v Shift	150KC
	AC Set 2 Pin D	5.56v	6.2v	1.4us for 5.6v Shift	200KC
Current Mode Input	Pin A	+0.4 -0.4	+1.2 -2.5	1.0us for 0.5v Shift	200KC

Output Waveforms

At Pin G For:

3 Volt Output

Min	Max
-6.54 -8.72	-6.06 -9.64

6 Volt Output

Min	Max
-6.54 -11.76	-6.06 -12.48

Rise Time (Max) = 0.9us
Pulse Duration = 1.0us (Nom)

Gated Sample Pulse Driver 2

This family of sample pulse drivers (DSP) is used to drive voltage mode triggers 1, 2 and 3. An output repetition frequency, independent of circuit loading, is obtained from each card in this group. Circuit operation is similar for all the cards and the different cap connections permit flexibility of application. These pulse generators are driven by either voltage mode or current mode circuits and have various collector loadings which produce either a 6v or a 3v output shift.

The circuits function as single-shot oscillators and provide about a 1μs output pulse regardless of the input signal duration. A gated, positive signal to the voltage mode inputs or a +N level at the current mode input starts the single-shot action.

Circuit Description

Cap connections on the schematic are those found on the AYWS card. The normal status of this circuit is: T4 conducting, T1 partially conducting, T2 cut off, and output pin G at −9.5v. There are two inputs, both conditioned by a single gate that must be up to 0v before either input can operate the circuit. The output expected is a 3v positive, 1μs pulse regardless of input duration in excess of 1μs.

With the input gate (pin C) at 0v for more than 7.5μs, a positive shift at input pin B cuts off T4. The attempt to reduce current through the 200μh inductance is resisted with a strong negative potential at the normally positive end of the coil. This negative spike passes through the 390$\mu\mu$f capacitor and drives T1 base negative. T1 emitter seeks to follow T1 base but is clamped by T2 emitter-base diode action. T1 base is, in turn, clamped by T1 emitter. T2 in full conduction brings output pin G up to −6v. This level is maintained while the 390$\mu\mu$f capacitor charges to −5.2v, through T1 emitter-base junction and T2 emitter-base junction. T2 is reverse-biased off when its base rises more positive than its emitter (−6.0v) and drops the output at pin G back to −9.5v.

The input signal must extend beyond the 1μs period to allow the circuit to time out. The 390$\mu\mu$f capacitor discharges through the 2K resistor.

Because of the large voltage developed by the collapsing field of the 200μh inductor, capacitors (C5, C30) are provided to short to ground any interference that might be introduced onto the −6v and −12v supply leads. The diode in parallel with the inductor prevents oscillation or ringing in the coil and speeds circuit recovery.

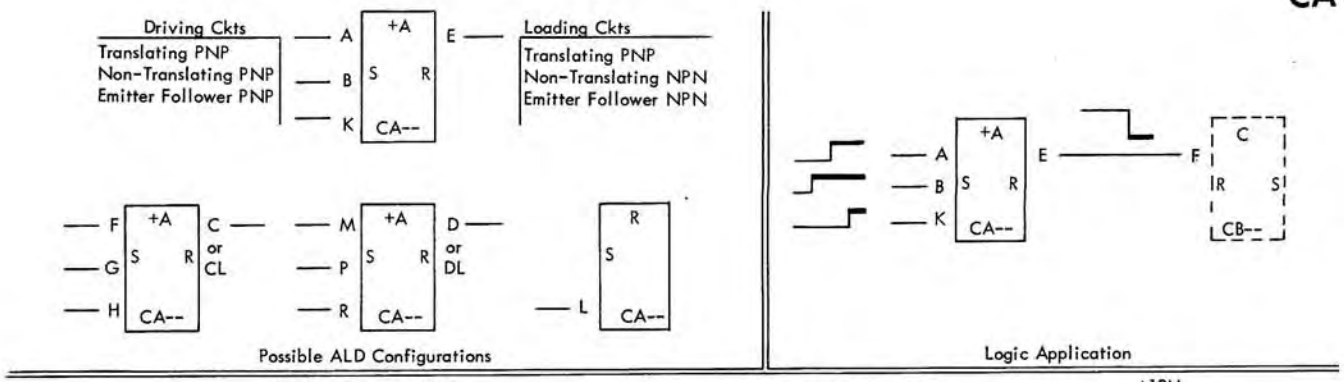
Other cap connections use the current mode input (pin A), which requires a current input; circuit operation is the same.

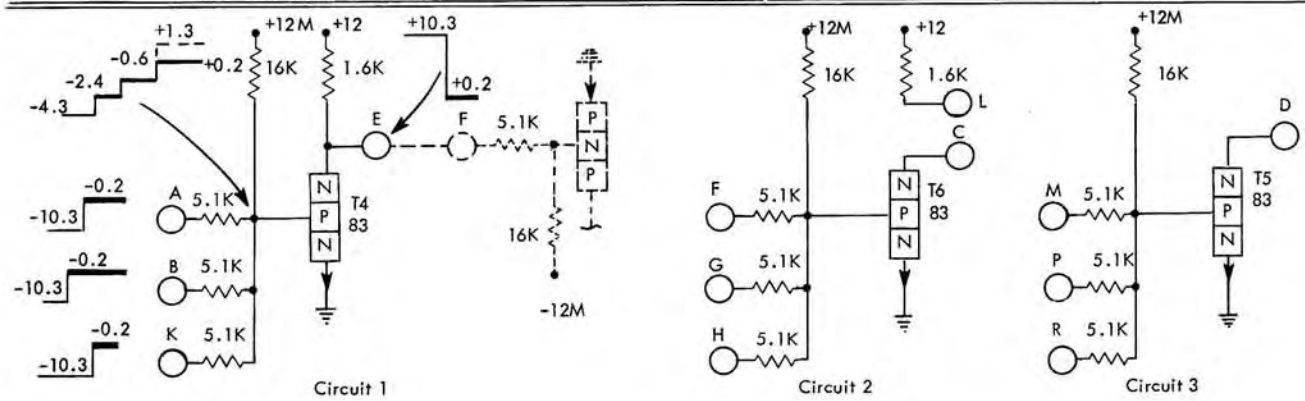
Application

The internal collector loading and input coupling network used are noted in the chart for the card code and cap connections. External collector loading is required for the unloaded circuits. Input and output waveform data are also given in the chart.

Gating: The gate input (pin C) is normally driven by CTDL, CTRL, or voltage mode trigger circuits that provide the required voltage levels. When the gate is used with the AC set 1 input, it must be conditioned 7.5μs before the set pulse is applied. When the gate is used with AC set 2 input, it must be conditioned 5.0μs before the set 2 pulse is applied.

Driving Capabilities: The 3v pulse from the DSP can drive 25 triggers (Voltage Mode Trigger 1 or 2) at a repetition rate of 150KC. The 6v pulse from the DSP can drive 25 type 3 triggers. A typical logic application is noted on the schematic.





CA-- 371026

Input Levels		Output Levels		Delays (usec)						Circuit Use
Min	Max	Min	Max	Measurements	Per		Block	Additional Load	Additional Input	100 uufd	
-0.2 / -5.56	+0.35 / -12.48	+5.56 / +0.2	+12.48 / -0.35	Input, GND, -0.6, -5.25, +5.25, +0.6, GND, T_{on}, T_{off}, Output	Turn On (T_{On})	Min	+0.34	-0.06	-0.04	+0.3	+A +AO +CO +TCO +TAO +TC -O -OA -CA
						Max	+1.35	0	+0.23	+0.15	
					Turn Off $T_{(off)}$	Min	+0.26	-0.02	-0.09	+0.09	
						Max	+2.26	+0.5	-0.03	+0.18	

CTRL Three-way NPN Translating Circuits

The CA - - card consists of 3 three-way NPN translating circuits used for repowering and level setting of CTRL signals. Each circuit on the card performs a basic logical function (+A, −O, C) and inverts an S input level to an R output level. The logical function is performed by the input resistor network, and the invert function is accomplished by the common emitter transistor configuration. Collector loading differs for each circuit and permits flexibility in driving external loads and for accomplishing the DOT functions.

In the +AND, invert logic application illustrated, a −R output is obtained only when all the inputs are up (+S).

Circuit Description (Circuit 1)

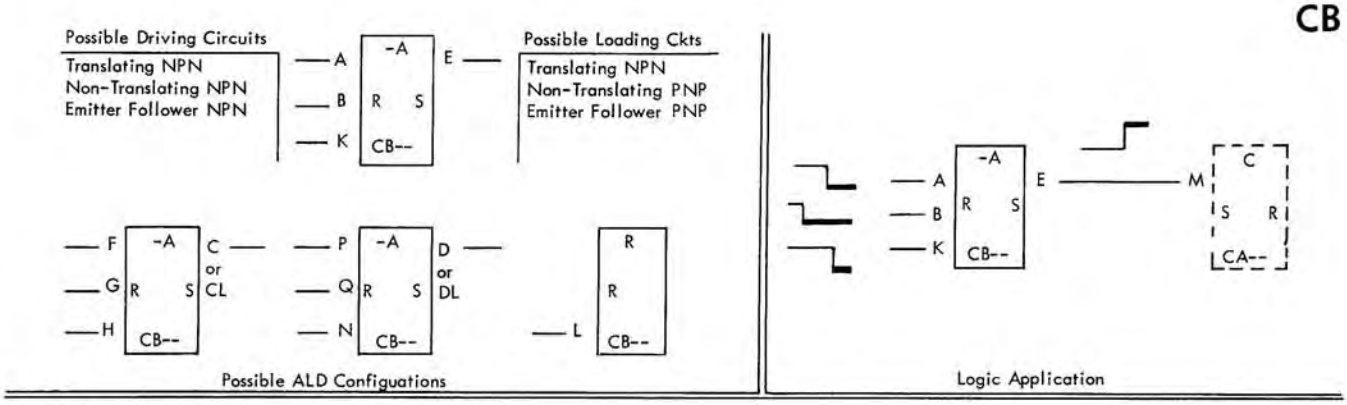
The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their levels. Input levels may vary at their low levels, but all will reach ground potential (+S) when up. A −S level at any input holds the base of T4 below the emitter voltage and keeps the transistor off, causing a +R output to exist at pin E. The exact output level at pin E is dependent on the circuit loading. A typical loading circuit, indicated by the dashed lines, is tied to the output.

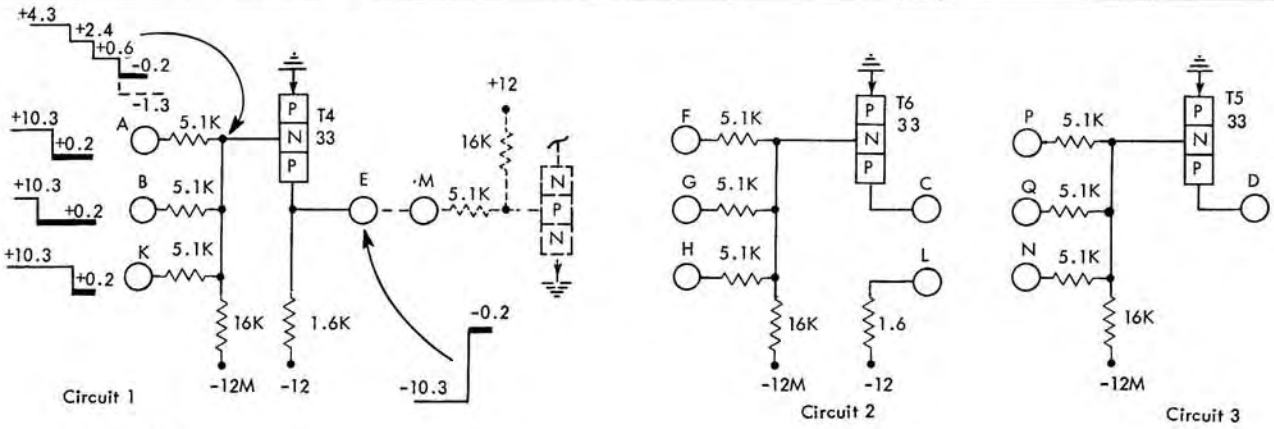
When all the inputs used are at the +S level, current flow into the divider network to the +12M supply raises the base voltage of T4 above ground potential. T4 is forward-biased into saturation and drops the output at pin E to the −R level.

Circuit delays are summarized in the chart for circuit and loading conditions. The delays are measured from the time the input signal reaches the circuit switching threshold until the output signal reaches the switching threshold of the loading stage.

Application

Possible logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by having similar output levels share a common collector load. This sharing of a collector load provides a second level of logic in the circuits. For example, output pins D and E are back-panel wired together to perform the +AO function. These circuits can also be combined with other CTRL logic circuits to make up trigger and latch configurations. Possible driving and loading circuits are also indicated with the ALD representations.





CB-- 371026

Input Levels		Output Levels		Delays (usec)						Circuit Use
Min	Max	Min	Max	Measurement	Per		Block	Load	Ad'tional Input	100 uufd	
+5.56 / +0.2	+12.48 / -0.35	-0.2 / -5.56	+0.35 / -12.48	Input +0.6 +5.25 Gnd	Turn On (T_{on})	Min	+0.34	-0.06	-0.04	+0.3	C R +O +OA +CA -A -AO -CO -TA -TC -TAO
						Max	+1.35	0	+0.23	+0.15	
				Output Gnd -0.6 -5.25 T_{on} T_{off}	Turn Off (T_{off})	Min	+0.26	-0.02	-0.09	+0.09	
						Max	+2.26	+0.5	-0.03	+0.18	

CTRL Three-way PNP Translating Circuits

The CB - - card consists of 3 three-way PNP translating circuits used for repowering and level setting of CTRL signals. Each circuit on the card performs a basic logical function (+O, −A, C) and inverts an R input level to an S output level. The logical function is performed by the input resistor network and the invert function is accomplished by the common emitter transistor configuration. Collector loading differs for each circuit and permits flexibility in driving external loads and for accomplishing the DOT functions. In the −AND, invert logic application illustrated, a +S output is obtained only when all the inputs are down (−R).

Circuit Description (Circuit 1)

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their levels. Input levels may vary at their high levels, but all will go to ground (−R) when down. A +R level at any one of the inputs holds the base of T4 above the emitter voltage and keeps the transistor cut-off, causing a −S level to exist at pin E. The exact output level at pin E is dependent on the circuit loading. A typical loading circuit, indicated by the dashed lines, is tied to output pin E.

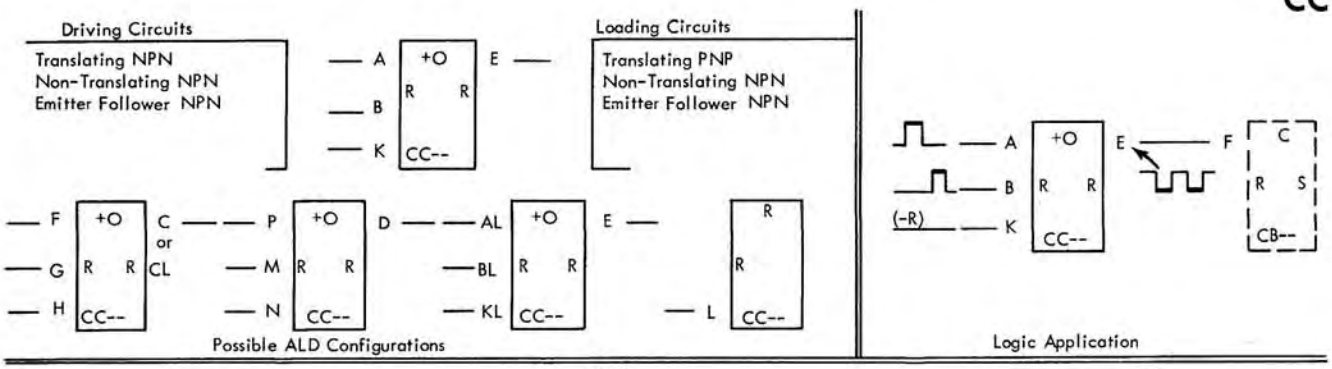
When all inputs used are at the −R level, current flow from the −12M supply decreases the base voltage of T4 below ground potential. T4 is forward-biased into saturation and increases the output at pin E to the +S level.

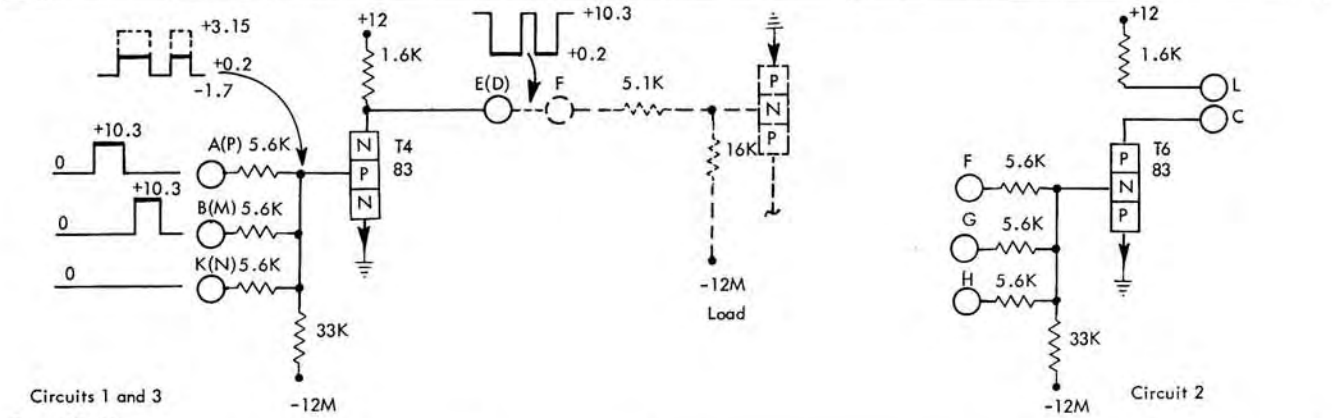
Circuit delays are summarized in the chart for circuit and loading conditions. The delays are measured from the time the input signal reaches the circuit switching threshold until the output signal reaches the switching threshold of the loading stage.

Application

Possible logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by having similar output levels share a common collector load.

This sharing of a common load provides a second level of logic in the circuits. For example, output pins D and E back-panel wired together could perform the −AO function. These circuits can also be combined with other CTRL logic circuits to make up trigger and latch configurations. Possible driving and loading circuits are indicated with the ALD representations.





CC-- 371028

Input Levels		Output Levels		Delays (usec)						Circuit Use
Min.	Max	Min	Max	Measurement	Per		Block	Load	Ad'tional Input	100 uufd	
+0.2	+5.56	+0.2	+5.56	Turn On (T_{On})	Min		+0.26	-0.03	-0.01	+0.01	E +O +I +IO +TO +TIO +TOO -A -IA -AO
-0.35	+12.48	-0.35	+12.48		Max		+0.84	-0.02	+0.2	+0.14	
				Turn Off (T_{Off})	Min		+0.6	+0.03	-0.12	+0.01	
					Max		+2.8	+0.06	-0.04	+0.18	

CTRL Three-way NPN Non-translating Circuits (Inverter)

The CC - - card consists of 3 three-way NPN non-translating circuits used for repowering and level setting of CTRL signals. This circuit is sometimes called the NOR circuit. Each circuit on the card performs a basic logical function (+O, −A, I) and inverts the R input signal. The logical function is performed by the input resistor network and the invert function is accomplished by the common emitter transistor configuration. Collector loading for circuit 2 differs from that of circuits 1 and 3 and permits flexibility in driving external loads and for accomplishing the DOT functions. In the +OR logic application illustrated, a −R output is obtained whenever a +R level occurs at any of the input pins.

Circuit Description (Circuit 1)

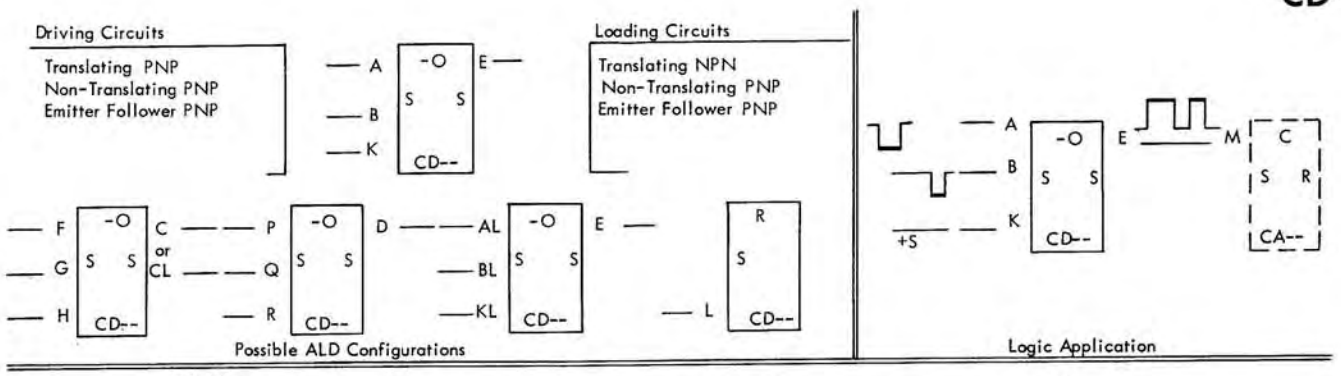
The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their level. Input levels may vary at their high levels (+R), but all will reach ground potential at the −R level. When −R levels exist at all the input pins, T4 base is at −0.7v. The transistor is held reverse-biased off as its emitter is connected to ground. Current flow from the load network through the 1.6K collector resistor to the +12v supply sets the off level at 10.3v.

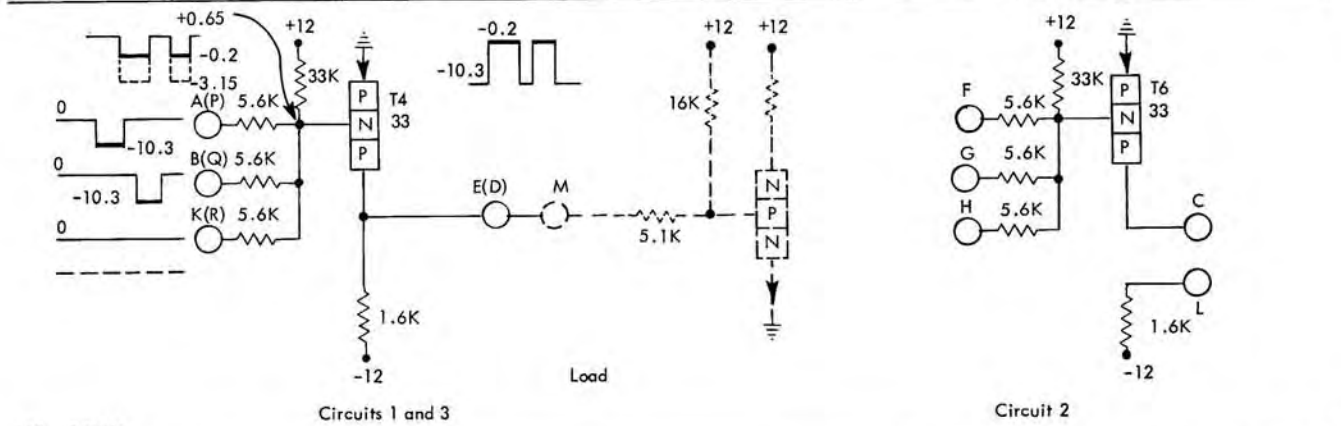
Increasing any input to the +R level causes T4 base to rise toward +3.15v. T4 becomes forward-biased and clamps the base at +0.2v. Saturation current flows through the transistor and quickly drops the output to the −R level (+0.2v). Coincidence of more than one +R level at the inputs drives the transistor further into saturation and increases the turn-off delay of the circuit.

Circuit delays are summarized in the chart. The delays are measured from the time the input reaches the circuit switching threshold until the output reaches the switching threshold of the loading stage.

Application

Possible logical functions of these circuits are indicated in the Circuit Use chart. DOT'ing the collectors (sharing of a common collector load by similar outputs) does not perform another level of logic, but merely increases the number of inputs. These inverter circuits are also combined with other CTRL logic circuits to make up trigger and latch configurations. Possible driving and loading circuits are indicated with the ALD representations.





CD-- 371029

Input Levels		Output Levels		Delays (usec)						Circuit Use
Min	Max	Min	Max	Measurement	Per		Block	Load	Ad'tional Input	100 uufd	
-0.2	+0.35	-0.2	+0.35	Input	Turn On (T_{on})	Min	+0.26	-0.03	-0.01	+0.01	E I R +A +IA -IO -O -OO -TIO -TO -TOO
-5.56	-12.48	-5.56	-12.48	Gnd, -5.25, -0.6		Max	+0.84	-0.02	+0.20	+0.14	
				Gnd, 0.6, -5.56	Turn Off (T_{off})	Min	+0.6	+0.03	-0.12	+0.01	
				T_{on}, T_{off}, Output		Max	+2.8	+0.06	-0.04	+0.18	

CTRL Three-way PNP Non-translating Circuits (Inverter)

The CD - - card consists of 3 three-way PNP non-translating circuits used for repowering and level setting of CTRL signals. This circuit is sometimes called the NOR circuit. Each circuit on the card performs a basic logical function (+A, −O, I) and inverts the S input signal. The logical function is performed by the input resistor network and the invert function is accomplished by the common emitter transistor configuration. Collector loading for circuit 2 differs from that of circuits 1 and 3, and permits flexibility in driving external loads and for accomplishing the DOT functions. In the −OR logic application shown, a +S output is obtained whenever a −S level occurs at any of the input pins.

Circuit Description

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their level. Input levels may vary at their low levels (−S), but all will reach ground potential at the +S level. When +S levels exist at all the input pins, T4 base is at +0.65v. The transistor is reverse-biased off as its emitter is returned to ground. Current flow from the −12v supply through the 1.6K collector resistor to the load divider network gives a −10.3v off output.

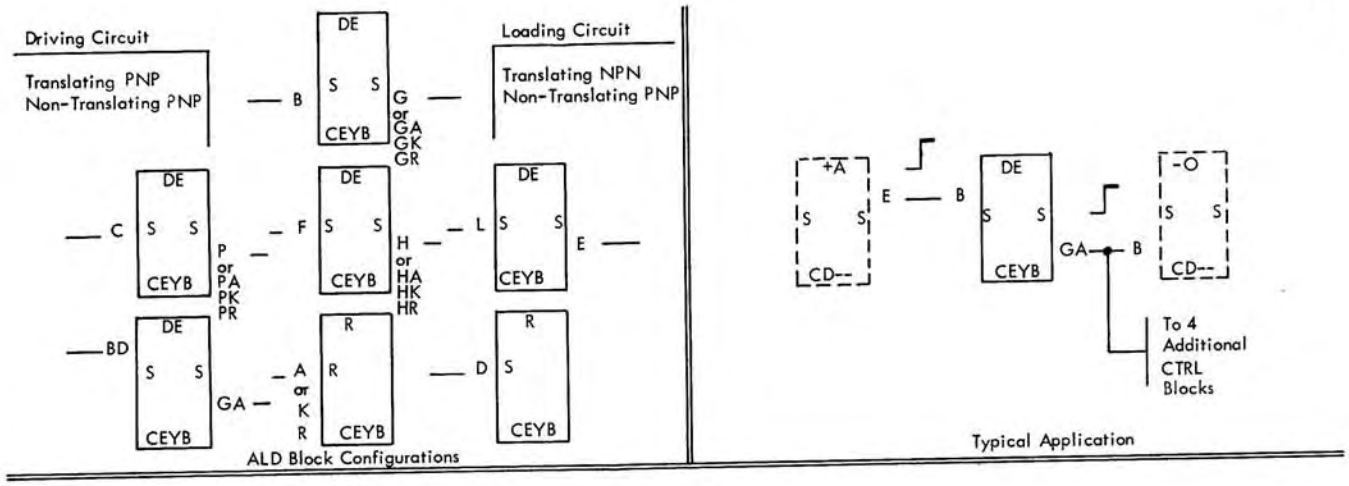
Dropping any input to the −S level causes T4 base to decrease toward −3.15v. T4 becomes forward-biased on and clamps the base at −0.2v. Saturation current flows through the transistor and quickly raises the output to the +S level (−0.2v).

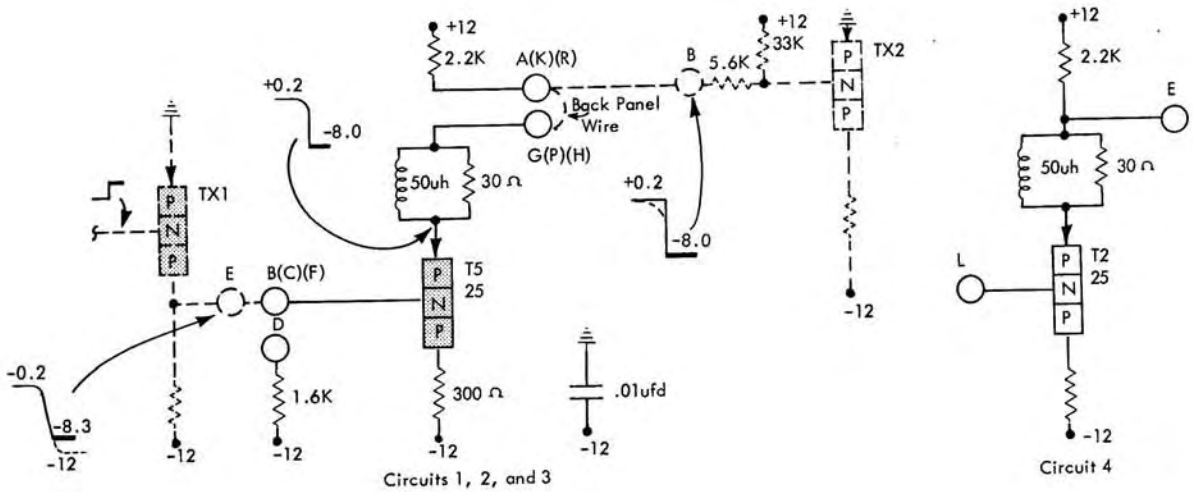
Coincidence of more than one −S level at the input drives the transistor farther into saturation and increases the turn-off delay of the circuit. Circuit delays are summarized in the chart. The delays are measured from the time the input reaches the circuit switching threshold until the output reaches the switching threshold of the loading stage.

Application

Possible logical functions of these circuits are indicated in the Circuit Use chart. DOT'ing the collectors (sharing of a common collector load by similar outputs) does not perform another level of logic, but merely increases the number of inputs. These inverter circuits are also combined with other CTRL logic circuits to make up trigger and latch configurations. Possible driving and loading circuits are indicated with the ALD representation.

CEYB





Card Code	Part Number	Input Voltage Levels		Maximum Output Current		Maximum Output Loading	Delay (usec)				Circuit Use
		Min	Max	Up Output	Down Output				CTRL-DE	Inv- DE	
CEYB	371032	-0.2 / -6.06	0 / -10.55	4.98ma	7.97ma	5 CTRL or 7 Inverter Circuits	Turn On	Min	+0.34	+0.3	DE +DEA -DEO
								Max	+1.55	+1.2	
							Turn Off	Min	+0.27	+0.65	
								Max	+2.3	+2.9	

The CEYB card consists of four one-way PNP emitter follower circuits. Each circuit serves as a non-translating current amplifier that drives additional logic or branching circuits. Emitter followers also serve as buffer devices to match impedances or provide isolation. A slight DC voltage shift results between the input and output voltage signals. Card and circuit design permit many variations in input and output loading connections of these emitter followers. A typical circuit application, input and output type loading, and some of the possible ALD block configurations are shown.

Circuit Description

Assume circuit 1 has the input and output loading indicated by the dash-line circuitry. With TX1 on, T5 base is at about −0.2v and T5 is in partial conduction. This current flows through the low resistance inductor into the 2.2K emitter follower resistor and input divider network of TX2 to the +12v supply. T5 base-emitter drop (0.2v to 0.4v) causes a slight voltage shift between the input and output signals. A +S output exists at pin A and reverse-biases TX2 off.

When TX1 turns off, its collector voltage drops toward −12v and increases the forward bias on T5. Current through T5 starts to increase but is momentarily resisted by the inductor. The voltage drop developed across the parallel LR network holds the output positive until the counter-EMF is overcome. Then, the output drops sharply to the −S level and the transistor is in full conduction. Additional current flow into the load network forward biases TX2 on.

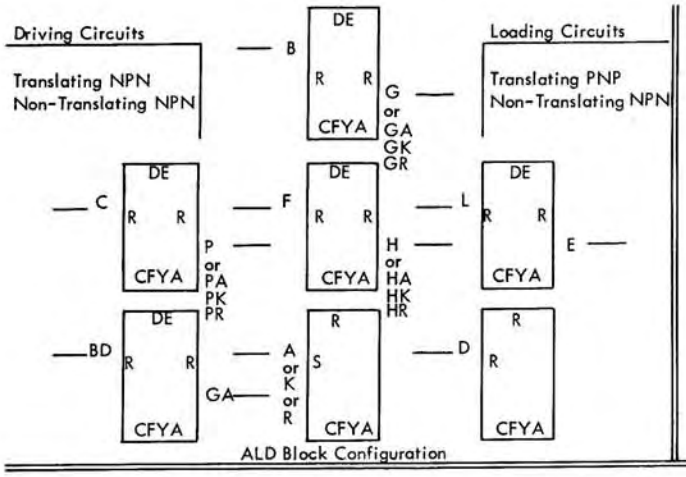
The circuit is returned to its original status by a +S level to T5. The rise to the former +S level is similarly resisted by the inductor and again a sharp shift results.

Because of the relatively low impedance offered by the emitter follower, the output level is little affected by the output loading (within limits). The 300 ohm collector resistor limits the power dissipation across T5. The 0.01μfd capacitor filters to ground any oscillation or ringing that might be introduced onto the −12v line by the coil. Because the emitter followers are normally driven by CTRL logic or inverter circuits, the delays given in the chart are the total delays encountered through the driving circuit and the emitter follower.

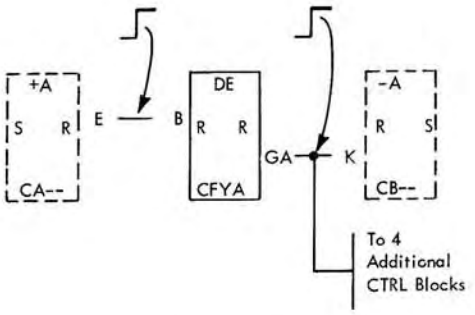
Application

The logical functions performed by these circuits are indicated in the Circuit Use chart. Back-panel wiring permits additional flexibility. For example, the DOT functions are accomplished by connecting similar output pins together to share a common emitter load. Wiring an input pin to pin D allows the DE to be driven from an unloaded logic circuit.

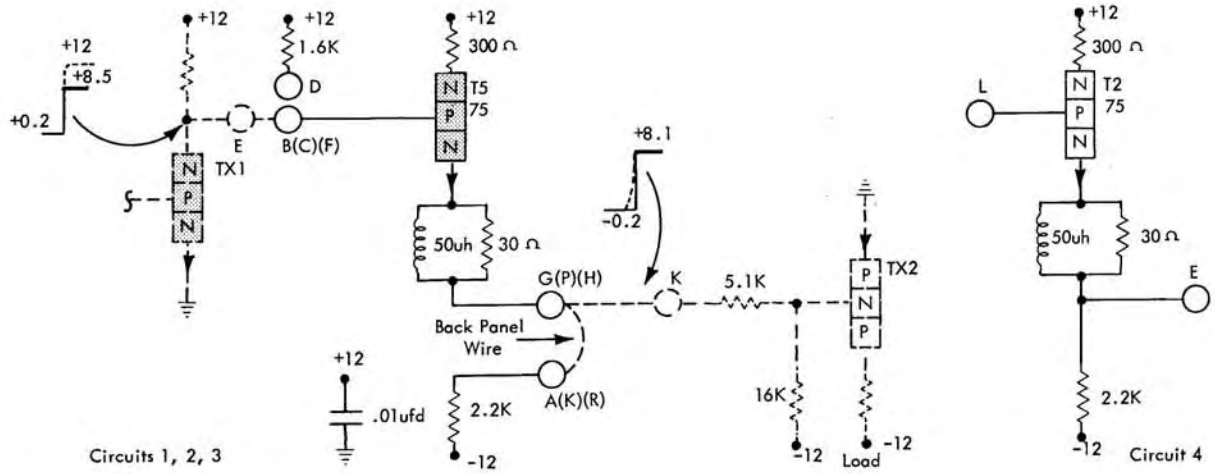
CFYA



ALD Block Configuration



Typical Application



Circuits 1, 2, 3

Card Code	Part Number	Input Voltage Levels		Maximum Output Current		Maximum Output Loading	Delays (usec)				Circuit Use
		Min	Max	Up Output	Down Output				Ctrl DE	Inv DE	
CFYA	371033	+6.39 / +0.2	+10.55 / 0	7.97ma	4.98ma	5 CTRL or 7 Inverter Blocks	Turn On	Min	+0.34	+0.3	DE +DEO -DEA
								Max	+1.55	+1.2	
							Turn Off	Min	+0.27	+0.65	
								Max	+2.3	+2.9	

The CFYA card consists of four one-way NPN emitter follower circuits. Each circuit serves as a non-translating current amplifier that drives additional logic or branching circuits. Emitter followers also serve as buffers to match impedances or provide isolation. A slight DC voltage shift results between the input and output voltage signals. Card and circuit design permit many variations in input and output loading connections of these emitter followers. A typical circuit application, input and output type loading, and some of the possible ALD block configurations are shown above.

Circuit Description

Assume circuit 1 has the input and output loading indicated by the dash-line circuitry.

With TX1 on, T5 base is at about +0.2v and T5 is in partial conduction. Most of the current from the load and the 2.2K resistor flows through the low resistance inductor into the transistor. T5 base emitter drop (0.2v to 0.4v) gives a slight voltage shift between the input and output signals. A −R output exists at pin G and reverse biases TX2 off.

When TX1 turns off, its collector voltage rises toward +12v and increases the forward-bias on T5. Current through T5 starts to increase, but is momentarily resisted by the inductor. The voltage drop developed across the parallel LR network holds the output positive until the counter-EMF is overcome. Then, the output increases sharply to the +R level and the transistor is in full conduction. Additional current flow into the load network forward-biases TX2 on.

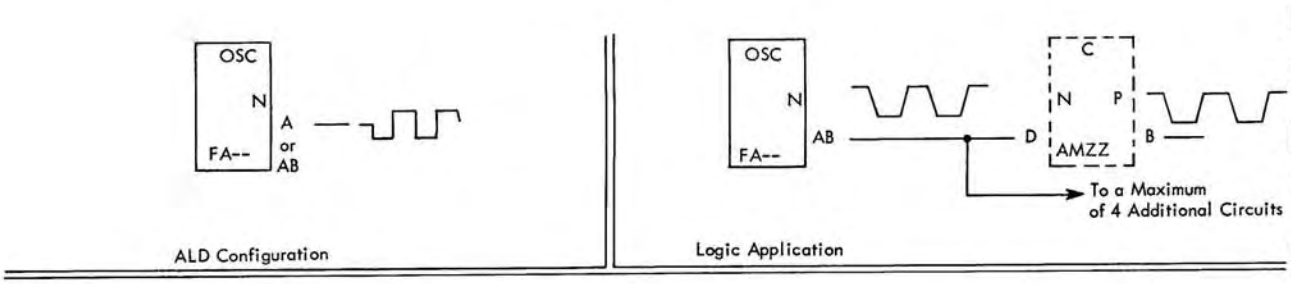
The circuit is returned to its original status by a −R level to T5. The drop to the former −R level is similarly resisted by the inductor and again a sharp shift results.

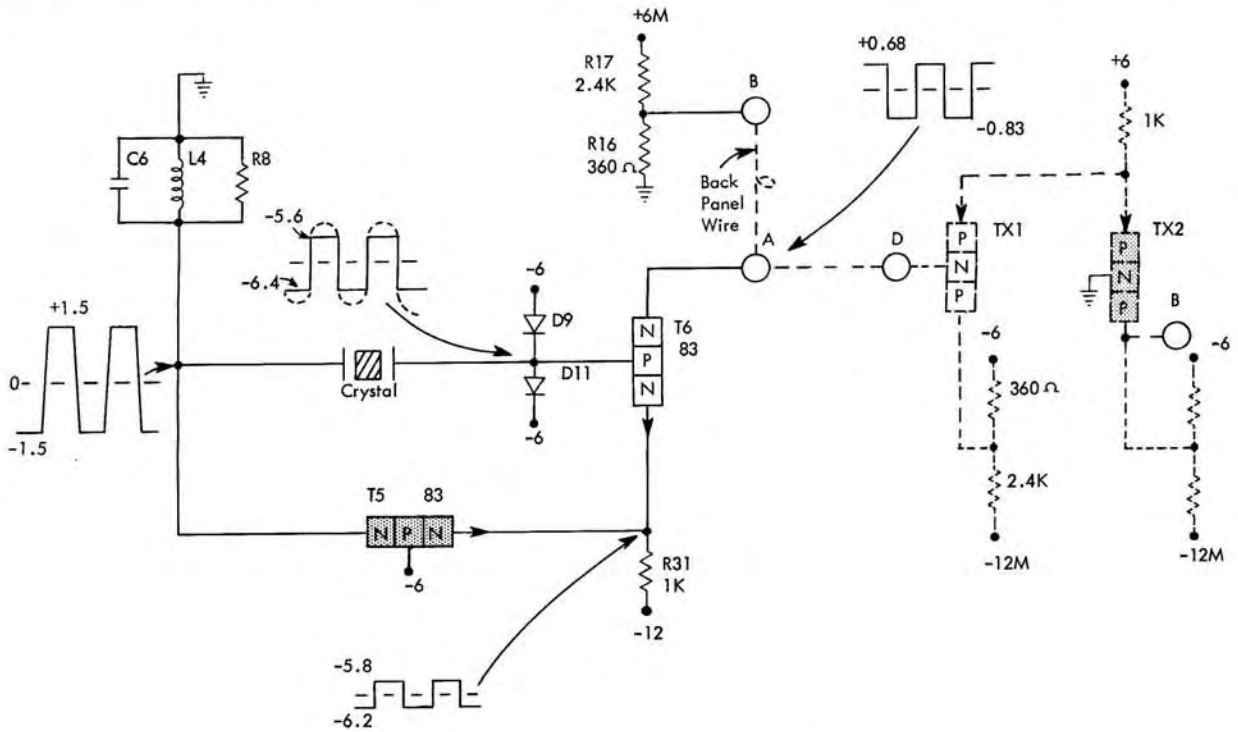
Because of the relatively low impedance offered by the emitter follower, the output level is little affected by the output loading (within limits). The 300 ohm collector resistor limits the power dissipation across T5. The 0.01 μfd capacitor filters to ground any oscillation or ringing that might be introduced onto the +12v line by the coil. Because the emitter followers are normally driven by CTRL logic or inverter circuits, the delays given in the chart are are the total delays encountered through the driving circuit and the emitter follower.

Application

The logical functions performed by these circuits are indicated in the Circuit Use chart. Back panel wiring permits additional flexibility. For example, the DOT functions are accomplished by connecting similar output pins together to share a common emitter load. Wiring of an input pin to pin D allows the DE to be driven from an unloaded logic circuit.

FA - -
FK - -
FS - -
FT - -
GD - -
GE - -
KR - -
LH - -
RK - -
RT - -





Card Code	Part Number 37----	Frequency KC	C6 uufd	L4 uh	Crystal Part No.	R8
FA--	1406	1000	150	100	491295	1.8K
FK--	1416	64	10,000	500	491282	1.8K
FS--	1404	240	1500	250	491293	1.8K
FT--	1405	360	680	250	491294	1.8K
GD--	1455	125	2500	500	492454	1.8K
GE--	1456	500	270	250	492455	1.8K
KR--	1457	720	125	250	492456	1.8K
LH--	1626	667	125	250	492567	1.8K
RK--	1788	363.4	680	250	492567	1.8K
RT--	1785	75	6800	500	492673	1.8K

Output Specifications	
Output	Levels
Min	Max
+0.47 / -0.49	+0.89 / -2.15
Available Load Current Minimum Values	
On	Off
1.33ma	0.82ma
Rise Time	Fall Time
0.8us	0.8us

Free Running Crystal Oscillators

These free running crystal oscillators serve as pulse generator circuits. Each card provides an oscillator type circuit that produces pulses or voltage variations of a definite frequency. The oscillators consist of a basic current switching circuit whose output frequency is determined by a quartz crystal. The crystal vibrates at a specific frequency and develops a sinusoidal voltage that controls and stabilizes the output frequency of the oscillator. An inductively tuned tank circuit provides regenerative feedback to sustain the crystal oscillations.

Circuit Description

Assume that T5 in the circuit shown starts to conduct when power is first applied to the circuit and sets the common emitter voltage of T5 and T6 to −6.2v. The initial surge of current into the tank circuit of C6, L4, and R8 quickly drops the collector voltage of T5 toward −1.5v and shocks the crystal into oscillation. The negative voltage transition of the crystal (acting as a tank circuit) causes the base voltage of T6 to go negative. D9 limits this negative swing to −6.4v (0.4v drop across the diode) and holds T6 reverse-biased off. With T6 off, only a small back current flows into the coupling network and the output at pin A is near +0.68v.

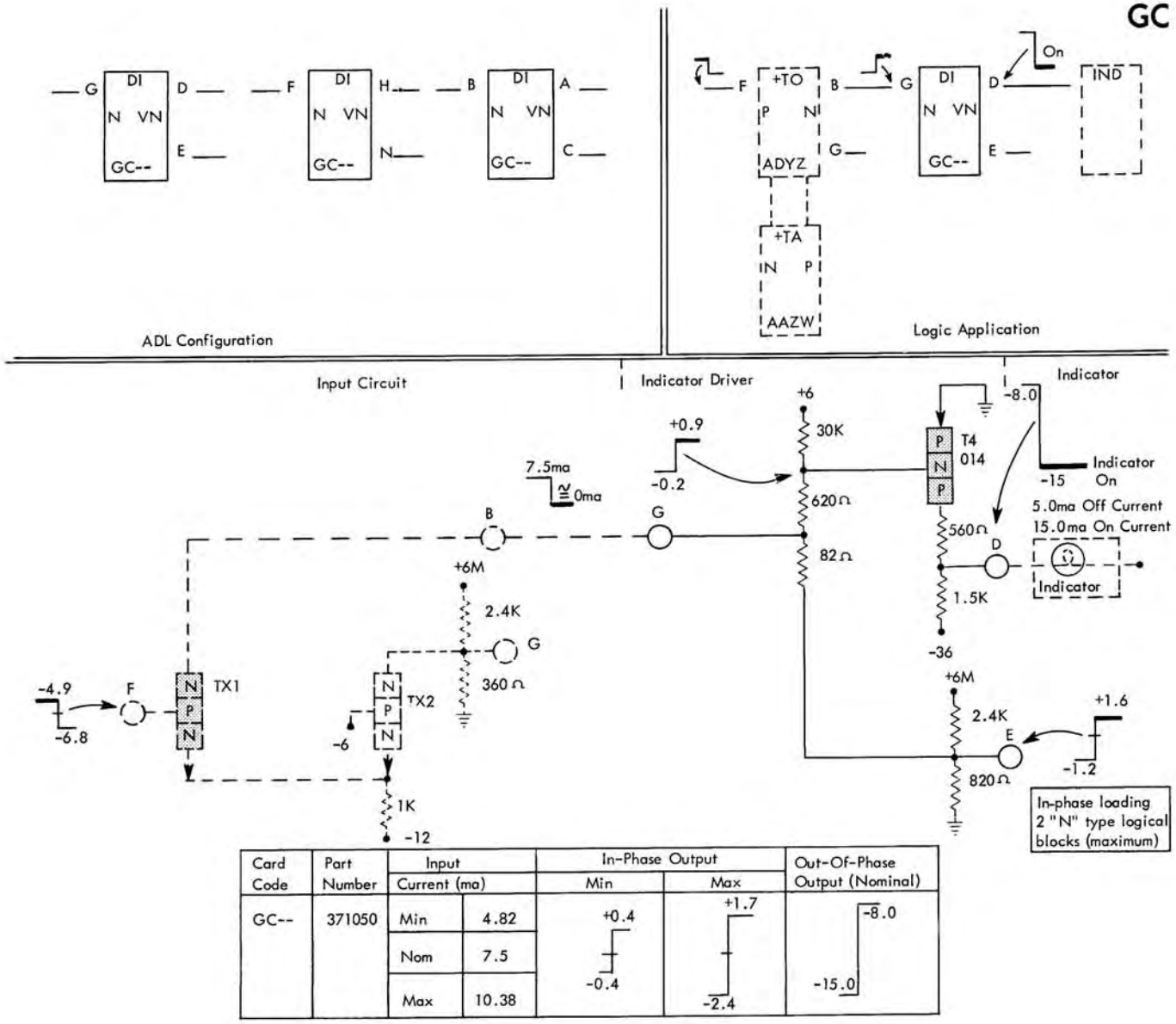
When the crystal output at the base of T6 starts to go positive and increases above −6.2v, T5 becomes reverse-biased off and T6 becomes forward-biased on. The positive base voltage swing is limited by D11 to −5.6v. Current (about 6ma), from the −12v supply and R31, switches from T5 to T6 and flows into the coupling network of T6. The output at pin A decreases to −0.83v. With T5 held off, its collector voltage becomes positive and feeds a regenerative voltage to the crystal which re-energizes the mechanical vibrations of the crystal. When the negative voltage transition of the crystal again drops below −6v, T6 is reverse-biased off and T5 is forward-biased on. The output at pin A again goes positive, as only the small back currents flow into the coupling network. Current flow through T5 into the tank circuit quickly drops the collector voltage of T5 and provides the necessary feedback. This action continues as long as power is applied to the circuit and results in the approximate square wave output noted on the schematic.

The tank circuit components C6, L4, and R8 are selected so that the feedback voltage to the crystal is of the proper phase and amount to sustain oscillations. The tank circuit also serves as a high frequency filter to eliminate the effects of the higher harmonics. D9 and D11 limit the drive to T6 so that it is not biased too far in cut off or near saturation. This permits linear operation of the circuit with little distortion of the output and quick switching of the output signal. Output specifications are noted in the chart shown.

Circuit operation is similar for all cards in this family. The values of C6, L4, R8, and the crystal are varied and provide output pulses of different frequencies. The chart relates the card code and component values to the various output frequencies.

Application

Typical loading on the oscillator circuit is noted in the circuit schematic. A maximum load of 5 current switching blocks is permissible. Back panel wiring of pin B is required when driving into standard current switching blocks. If the load circuit contains its own coupling network the back panel wire from A to B is disregarded and the output is taken from pin A.



Card Code	Part Number	Input Current (ma)		In-Phase Output Min	In-Phase Output Max	Out-Of-Phase Output (Nominal)
GC--	371050	Min	4.82	+0.4 / -0.4	+1.7 / -2.4	-8.0 / -15.0
		Nom	7.5			
		Max	10.38			

Current Mode + N Indicator Driver

The GC-- card consists of three voltage mode indicator driver circuits. Each circuit supplies up to 15ma to an incandescent lamp connected to its out-of-phase output pin. In addition, the in-phase output is capable of driving two N type logic blocks. The indicator drivers accept a current input from either the in-phase or out-of-phase outputs of a P type current switching block or its equivalent.

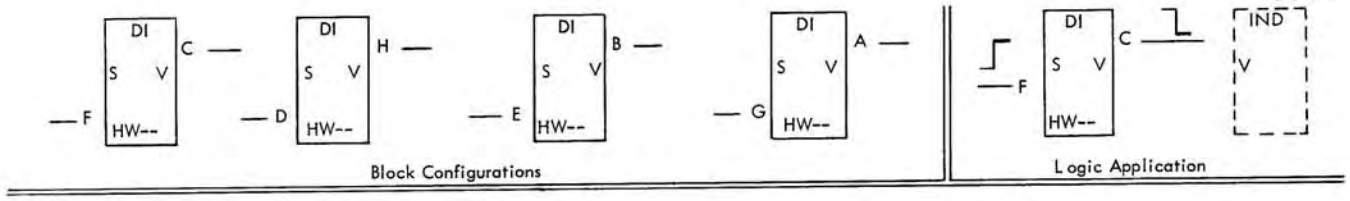
Circuit Description

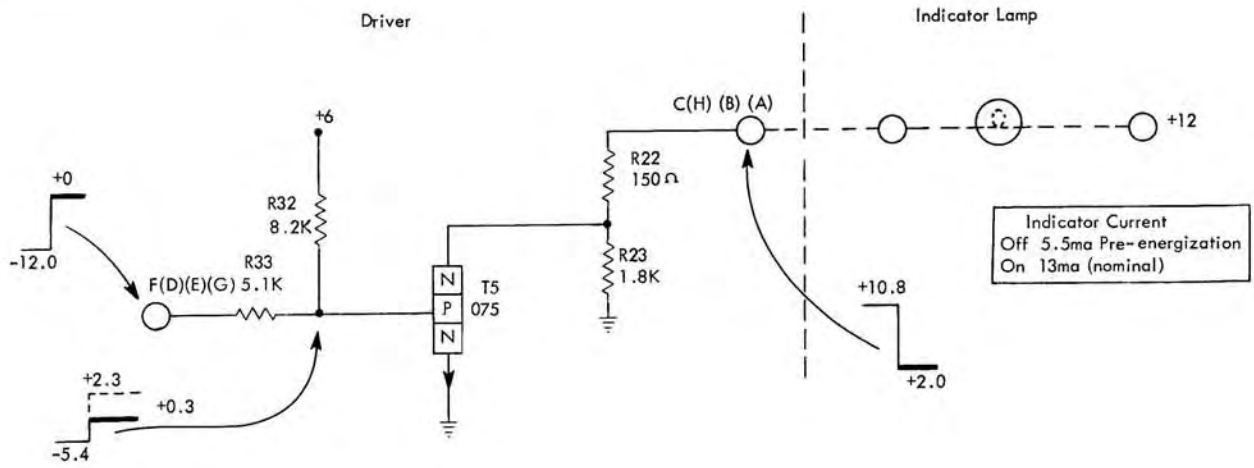
In the state shown, TX1 is forward-biased on and supplies input current (7.5ma) to the indicator driver. This current flow into the divider network decreases the base voltage of T4 below ground and provides a −N output from pin E. T4 is forward-biased on and appears as a low resistance in parallel with the indicator lamp. Saturation current flows through T4 and limits the current to the indicator to about 5ma; this pre-energization current is not sufficient to light the lamp. The voltage that exists at pin D at this time is −8.0v.

When the input to TX1 drops to −6.8v, TX1 is cut off and TX2 is biased on. The input current to the indicator driver drops to near 0ma (a small I_{CO} would flow). Decreasing current flow into the divider network raises the base voltage of T4 to +0.9v and the output at pin E to a +N level. T4 is reverse-biased off and now appears as a relatively high resistance in parallel with the indicator lamp. Current flow into the lamp increases to 15.0ma and lights the lamp.

Application

Each circuit supplies the necessary current to light one incandescent lamp and drive 2 N type logic blocks. A typical logic application is shown.





Card Code	Part Number	Input Levels		Current Output (ma)		
		Min	Max		Nominal	Max.
HW--	371048	-0.3 / -5.46	+6.24 / -12.48	On	13	15
				Off	5.5	—

Voltage Mode Indicator Driver

The HW - - card consists of four voltage mode indicator driver circuits. Each circuit supplies up to 15ma to an incandescent lamp connected to its out-of-phase output pin. A positive input level is required to turn on the transistor and light the lamp. The indicator drivers can be driven by CTDL, CTRL, or voltage trigger circuits that provide the input levels noted in the chart.

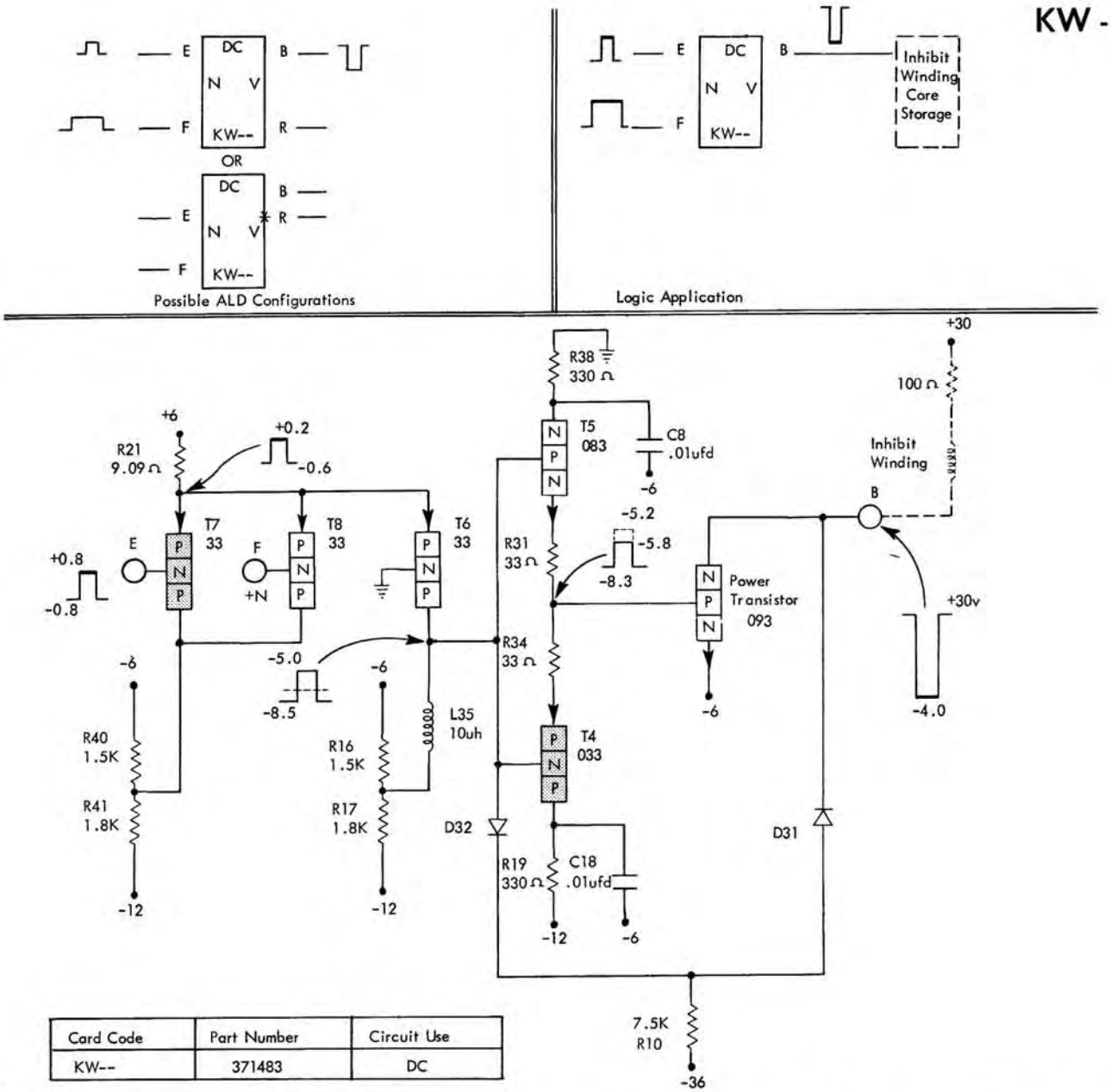
Circuit Description

With a −S input at pin F, the base voltage of T5 drops to −5.3v and holds the transistor reverse-biased off. Only a pre-energized current of 5.5ma flows through R23, R22, and the lamp to the +12v supply; this current is not sufficient to light the lamp. A voltage output of 10.8v exists at pin C.

When the input increases to the +S level, the base of T5 increases towards +2.3v but clamps at +0.3v when T5 is forward-biased on. T5 appears as a low resistance in parallel with R23. The output at pin E increases toward ground potential and supplies 13ma to the lamp.

Application

Each circuit provides the current necessary to light one incandescent lamp. A typical logic application is shown.



Card Code	Part Number	Circuit Use
KW--	371483	DC

Core Driver

The KW--card is a core driver circuit that drives the inhibit windings used in the core storage area. This driver circuit is made up of a basic + AND circuit, a complementary emitter follower, and a power diffused transistor. Coincidence of + N levels is required at both inputs to permit output current to flow.

Circuit Description

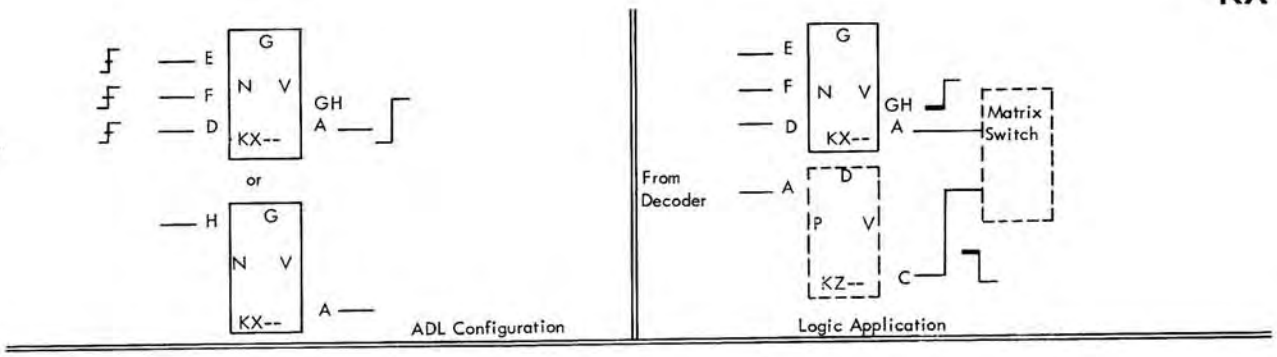
Assume the starting condition noted. With a −N input at pin E, the base of T7 becomes more forward-biased than the reference transistor T6. T7 turns on and current flow through R21 clamps the emitter voltage of T7 to −0.6v. T8 and T6 are reverse-biased off. With T6 held off, its collector voltage nears −8.5v set by current flow from the −36v supply through R10, D32 and L5 into the collector coupling network. T4 is forward- biased on, and T5 is reversed-biased off. The base of the power transistor follows this swing (−8.3v) and holds the power transistor off as its emitter is returned to −6v.

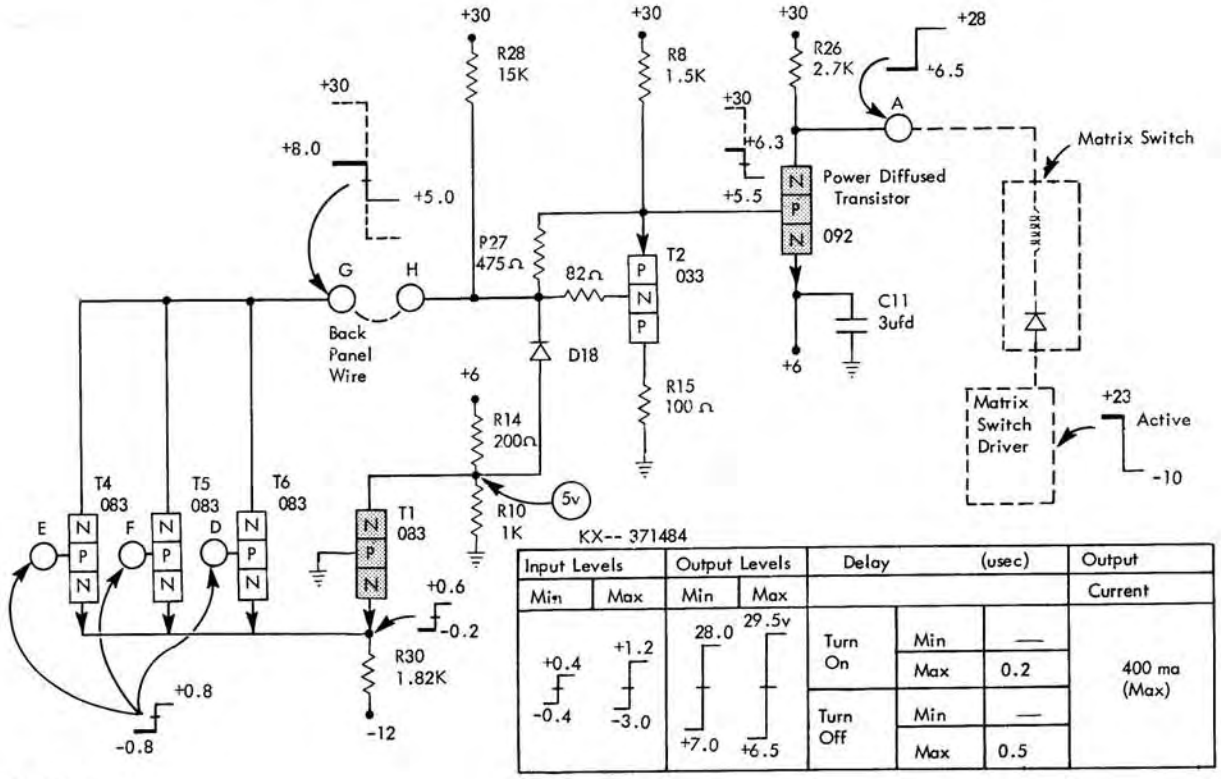
No current flows into the inhibit winding, and the output seen at pin B at this time is near 30v.

When coincidence of +N levels occurs at both input pins, T7 and T8 become reverse-biased off and T6 is biased on. Current flow through T6 causes the base voltage of the complementary emitter followers to increase to −5.0v. T5 now becomes forward-biased and T4 is reverse biased. Conduction through T5 quickly raises the base voltage of the power transistor toward −5.2v. When the base voltage reaches −5.8v, the power transistor turns on and supplies current (up to 400ma) to the inhibit windings. D32 and D31 clamp the output voltage swing to about −4v. This prevents the power transistor from operating in saturation and results in faster switching of the output current pulses. The complementary emitter follower is used to provide sharp rise and fall characteristics of the voltage signal controlling the power transistor, which also reduces the switching time.

Application

This driver is used in the core storage area of the IBM 7070 Data Processing System.





Input Levels		Output Levels		Delay		(usec)	Output
Min	Max	Min	Max				Current
+0.4 / -0.4	+1.2 / -3.0	28.0 / +7.0	29.5v / +6.5	Turn On	Min	—	400 ma (Max)
					Max	0.2	
				Turn Off	Min	—	
					Max	0.5	

Power Gate

The power gate circuit on the KX--card is used in conjunction with the matrix switch driver card (KZ--) for correct addressing of the X and Y drive lines in core storage operation. This circuit is made up of a basic — AND circuit, a modified emitter follower and a power diffused junction inverter. Coincidence of —N levels at all the inputs is required for the circuit to be active. When the circuit is active, the power gate output is at +6.5v and allows a large current to flow in a selected primary winding of a matrix switch. Selection of a particular primary winding is accomplished by activating its matrix switch driver (+23v). When the power gate is inactive, only the small back-current flows through the matrix switch windings.

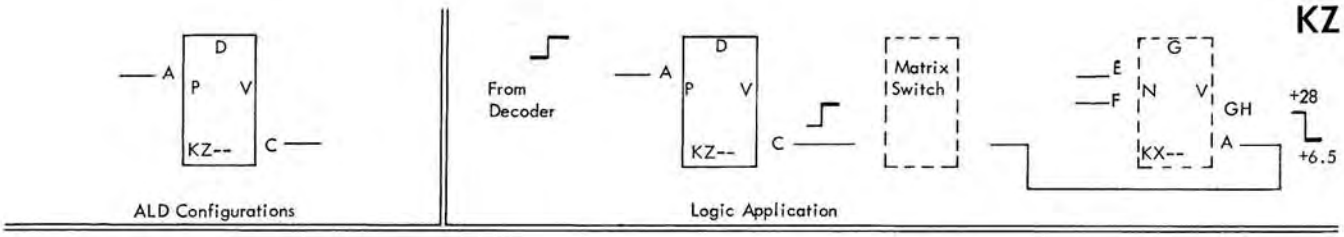
Circuit Description

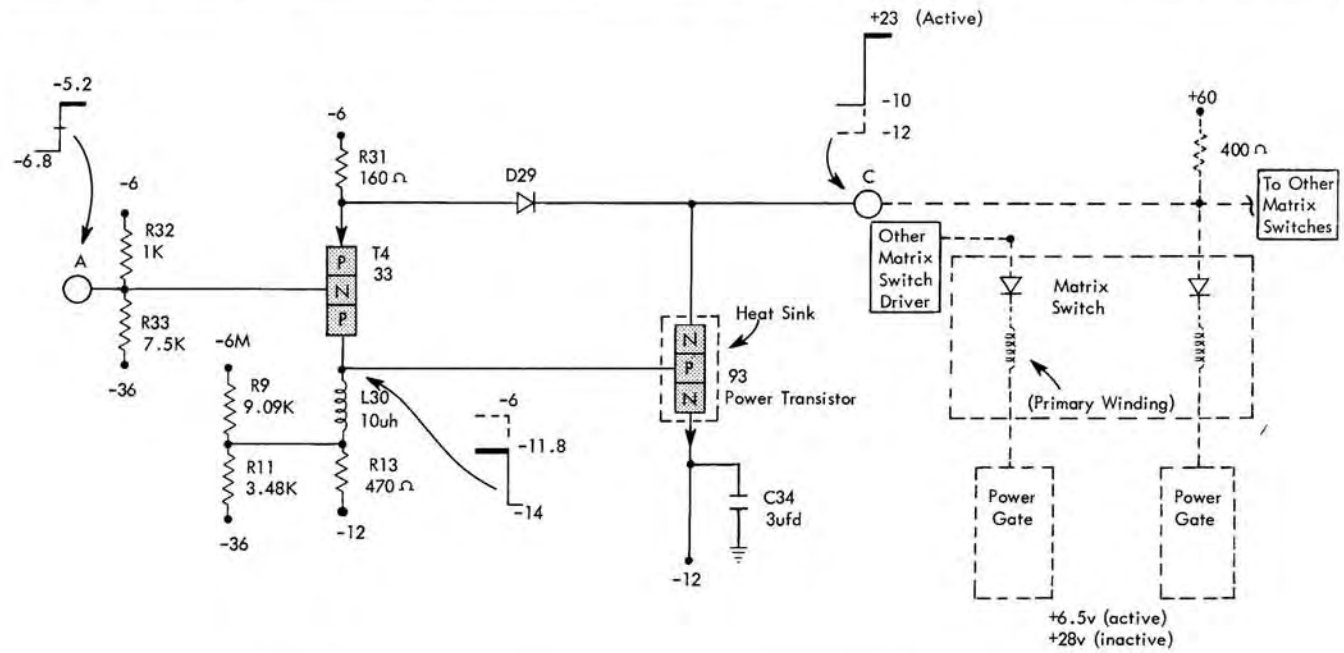
Active Status: With a —N input at pins E, F, and D, the transistors T4, T5, and T6 are reverse-biased off and T1 is forward-biased on. The emitter voltage of T1 is clamped at —0.2v. At this time, the voltage at pin H attempts to increase toward +30v, but the power diffused transistor becomes forward-biased into conduction; base current from the power diffused transistor through R8, R27 and R28 to +30v sets the voltage at pin H near +8.0v and holds T2 reverse-biased off. Conduction through the power transistor quickly drops the output at pin A to +6.5v and, depending on the status of the matrix switch drivers, permits current to flow in a selected primary winding.

Inactive Status: When a +N level is applied to pin E (or to any of the input pins), T4 becomes forward-biased on and T1 is reverse-biased off. Additional current flow through R28, R27, and R8 causes the voltage at pin H to drop 5v. T2 becomes forward-biased and conducts, quickly dropping the base voltage of the power transistor to about 5.5v. The power transistor is reverse-biased off and the output at pin A increases toward +30v. The purpose of D18 is to clamp the inactive output of T1 and T2 to the +5v set by the coupling network of R10 and R14. The clamping action limits the drive to T2 which in turn prevents the power transistor from being biased too far in the off direction. This reduces the switching time of the output seen at pin A.

Application

The KX--card is used in the core storage section of the IBM 7070 system. Typical circuit usage is noted above. Back panel wiring of pins G and H is required in most applications.





KZ---371482

Input Levels		Output Levels		Delays			Current		
							Input		Output
Min	Max	Min	Max			(usec)	On	Off	
-5.4 / 0 / -6.4	-3.0 / -7.1	+23 / -10	+23 / -11.5	Turn On	Min	—	150 ma (Max)	≅0	+23 / -10
					Max	0.05			
				Turn Off	Min	—			
					Max	0.05			

Matrix Switch Driver

The KZ--card consists of a special driver used in the X and Y line address circuitry of core storage. Each driver controls the status of a matrix switch used with power gates to properly select or address a X or Y line. A +P input to the driver is required to place the circuit in the active condition and to allow current to flow through the gated primary winding. A −P input inhibits the flow of current in the X or Y primary windings of the matrix switch.

Circuit Description

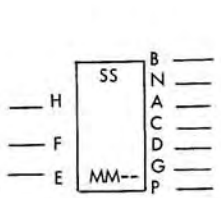
In the quiescent state, conduction from −12 volts through R13 to the coupling network of R9 and R11 sets the bias level of the power transistor to approximately −14 volts.

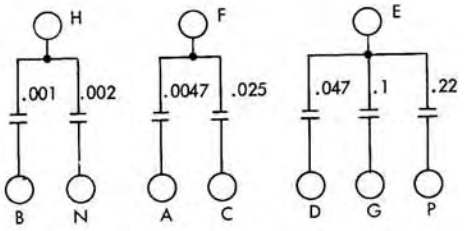
Inactive State: A −P input (−6.8v) applied to pin A forward-biases T4 on. Conduction through T4 causes the base voltage of the power transistor to increase toward −6v, but this voltage clamps at −11.8v when the power transistor is forward-biased on. Current flows through the 400 ohm resistor to the +60v supply and provides an output at pin C near −10v. The isolation diodes in the matrix switch are reverse-biased regardless of the status of the power gates, and prevent current from flowing in the primary windings. Dropping the voltage at pin C to −10v, causes D29 to be forward-biased and allows current to flow through R31. This action results in a degenerative feedback that reduces the forward bias of T4, which in turn causes a decrease in the forward bias of the power transistor. Because of this action, the power transistor is prevented from operating in saturation and faster switching action from the inactive to the active status results.

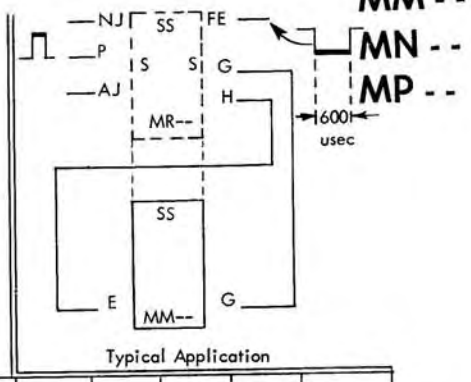
Active Status: If a +P input (−5.2v) is applied to pin A, T4 is reverse-biased off. The base voltage of the power diffused transistor drops to −14v. The power transistor is reverse-biased off; its collector output increases toward +60v and permits the matrix switch to be in an active state. Assume that one of the power gates is on (+6.5v): current then flows through the primary winding, the isolation diode, and the 400 ohm resistor to +60v to give an output at pin C of about +23v.

Application

This driver is used in core storage of the IBM 7070 system. Typical circuit application for the driver is shown.



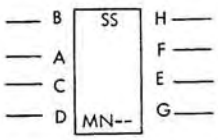




Typical Application

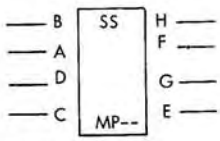
MM-- 371624

Timing (Pulse Duration) (usec)	From (± 23%)	6.1	10.5	15.1	20.2	28.8	63.3	114	152	205	310	426	617	925	1,360	1,660
	To (± 17%)	9.4	17.6	25.6	36.5	51.8	114	190	265	365	555	765	1,100	1,650	2,420	2,980
Back Panel Wiring	Connect to Pin H*	H	H	H	F	FH	F	F	F	F	EF	E	E	E	E	EF
	Connect to Pin G*	B	N	BN	A	NA	A	C	C	D	CD	G	DG	P	GP	CDGP
	Other Connection	-	-	—	-	—	G*to C*	—	G*to C*	-	-	-	-	-	-	—



MN-- 371625

Timing (Pulse Duration) (msec)	From (± 23%)	2.29	2.99	3.37	4.02	4.87	7.23	10.7	13.1	15.7	18.0	22.8	28.0	33.9	38.8	
	To (± 17%)	3.02	3.96	4.48	5.38	6.45	9.60	14.3	17.5	20.7	23.9	30.4	37.2	45.0	51.5	
Back Panel Wiring	Connect to Pin H*	E	H	F	H	G	EG	F	FE	FG	FEG	H	HG	HF	HFG	
	Connect to Pin G*	C	D	D	D	D	CD	A	AC	AD	ACD	B	BD	BA	BAD	
	Other Connections	-	BFAG	AG	BG	-	—	-	-	-	-	-	-	-	-	



MP-- 371638

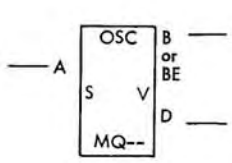
Timing (Pulse Duration) (msec)	From (± 23%)	49.2	64.0	82.2	108	124	207	270	339	389	600	833	990	1,570	1,910	2,300
	To (± 17%)	65.2	84.5	109	143	163	274	359	450	516	795	1,100	1,610	2,090	2,530	3,040
Back Panel Wiring	Connect to Pin H*	H	-	F	F	H	H	F	E	HE	F	E	G	G	GE	HFGE
	Connect to Pin G*	B	A	C	A	BA	B	AD*	C	BC	AB*	CB*	D	DB*	DCB*	ABCD B* D*
	Other Connections	-	F to D*	AE	-	F to D*	G*to B	-	-	—	—	—	-	—	-	—

*Indicates Pins on MR-- Card.
(Note. All CapacitorsValues in MFD.)

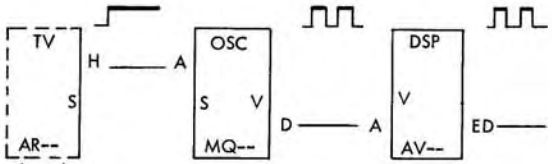
Single-Shot Timing Cards

This group of single-shot timing cards consists of different capacitor values arranged in various configurations. These capacitors are connected to the coupling pins of the single-shot 2 card (MR - -) and permit a wide selection of output pulse timings. A typical ALD application is given.

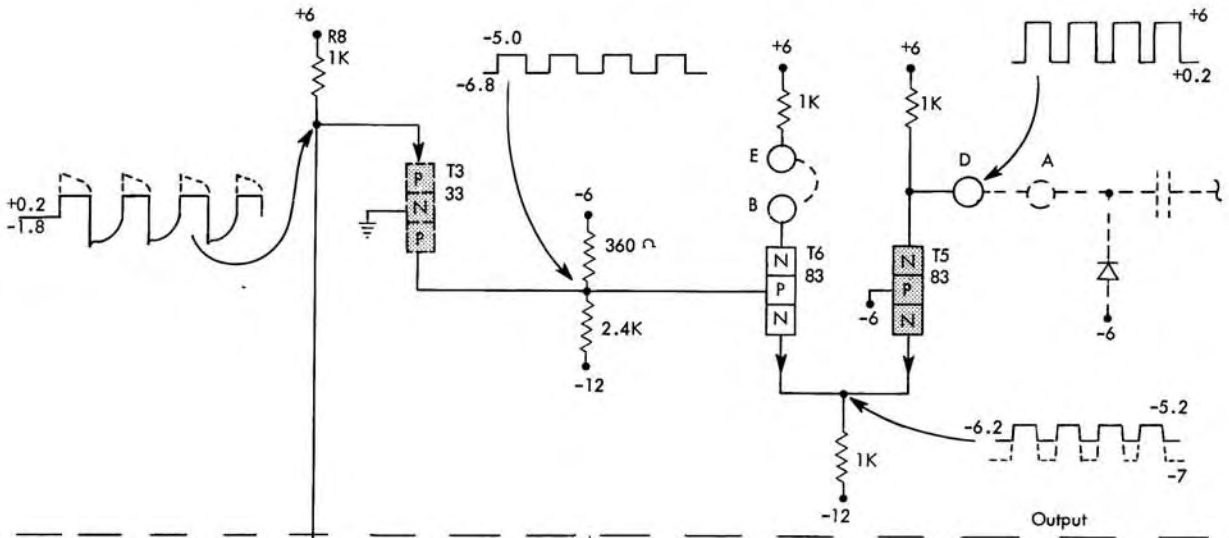
The available timings for each card when used with the MR - - single-shot card are summarized in the chart. Refer to the MR - - card for circuit description and application of these cards.

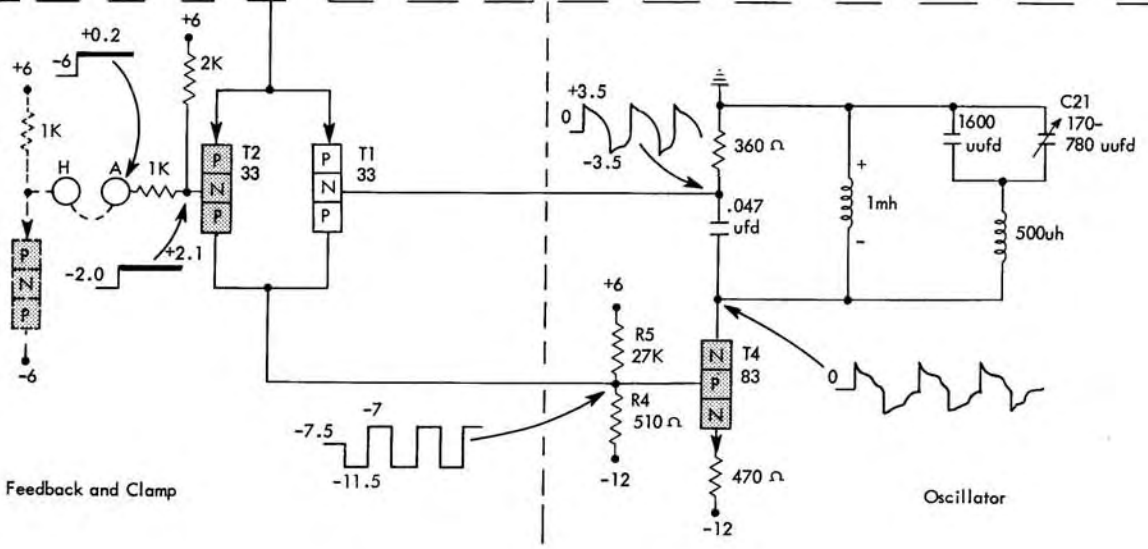


ALD Configuration



Typical Application





Card Code	Part Number	Circuit Use
MQ--	371646	OSC

The MQ - - card is a clamped oscillator circuit that provides a square wave output at intervals of about 13μs. Each card configuration consists of an oscillator circuit, a feedback and clamp circuit, and an output circuit. A +S input to the feedback and clamp circuit allows the oscillator to operate and provides the square wave output. This card is used mainly in timing and pulse forming circuits. In the typical application shown, the oscillator is controlled by a voltage mode trigger and drives into the sample pulse driver.

Circuit Description

Assume the circuit conditions as noted on the schematic. The dash-line circuitry indicates input and output loading.

Oscillator Off. With a −S input at pin A, transistors T2, T4 and T5 are partially conducting and T1, T3 and T6 are off. The output at pin D is at +0.2v. Current flow from the divider network of R4 and R5 through T2 and R8 to +6v holds the common T1 and T2 emitters at −1.8v and the base of T4 near −7.5v. T3 is reverse-biased off and current through its collector divider network sets the base of T6 at −6.8v. T6 and T5 common emitters attempt to follow the base input of T6 to −7v. However, T5 goes into conduction and clamps the common T5 and T6 emitters at −6.2v and establishes the output at pin D to +0.2v.

With the base of T4 held at −7.5v, a constant current flows through T4 and the 1mh inductor. Little voltage is dropped across the low resistance inductor and T1 base is set near ground potential. T1 is reverse-biased off as conduction through T2 keeps the common emitters of T1 and T2 at −1.8v.

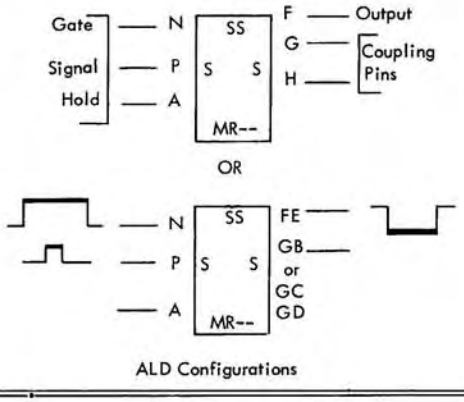
Oscillator On. A positive shift at the clamp input (pin A) reduces the forward bias on T2. Reduced current flow in T2 allows the common emitters of T2 and T1 to become less negative and the common collectors to become more negative. T4 conducts less and the current through the 1mh inductor tries to drop. This change is resisted with a counter-EMF that reflects a positive potential onto T1 base and prevents T1 from going into instant conduction. As soon as the counter-EMF dissipates, T1 does conduct, drawing the common emitters of T1 and T2 negative and the common collectors positive. T4 conducts more current, charging the network capacitors and driving T1 base more negative. T4 continues to conduct harder until the capacitors are charged and a constant current again flows through the inductor. T1 base starts to become less negative, and T4 starts to conduct less. Again counter-EMF drives T1 base positive, and a cycle is complete.

The frequency is determined by the values of inductance, capacitance, and resistance in T4 collector circuit. Charge and discharge time of the LC network are the determining factors. Therefore, the frequency can be changed by adjusting the variable capacitor (C23). Oscillations can continue as long as the common base and common collector of T1 and T2 are not restricted by any conduction in T2.

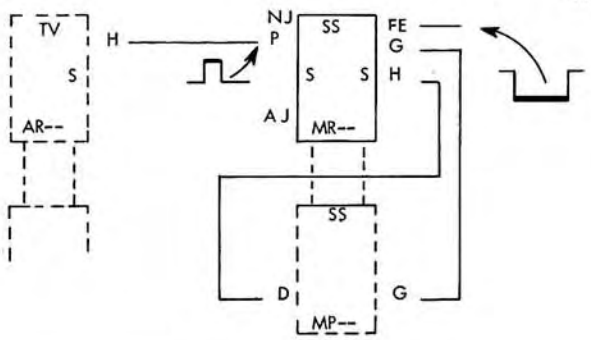
Square Wave Output. Each time the common emitters of T1 and T2 seek a positive level, T3 becomes forward biased and conducts. T3 collector becomes less negative and T6, an emitter follower, conducts. As soon as T6 emitter (common with T5 emitter) rises to −6v, T5 cuts off because of emitter-base reverse bias. The output at pin D rises to +6v.

T1 and T2 emitters again go negative as the oscillator cycle progresses. T3 cuts off, T6 cuts off, and T5 returns to partial conduction. Output pin D returns to ground.

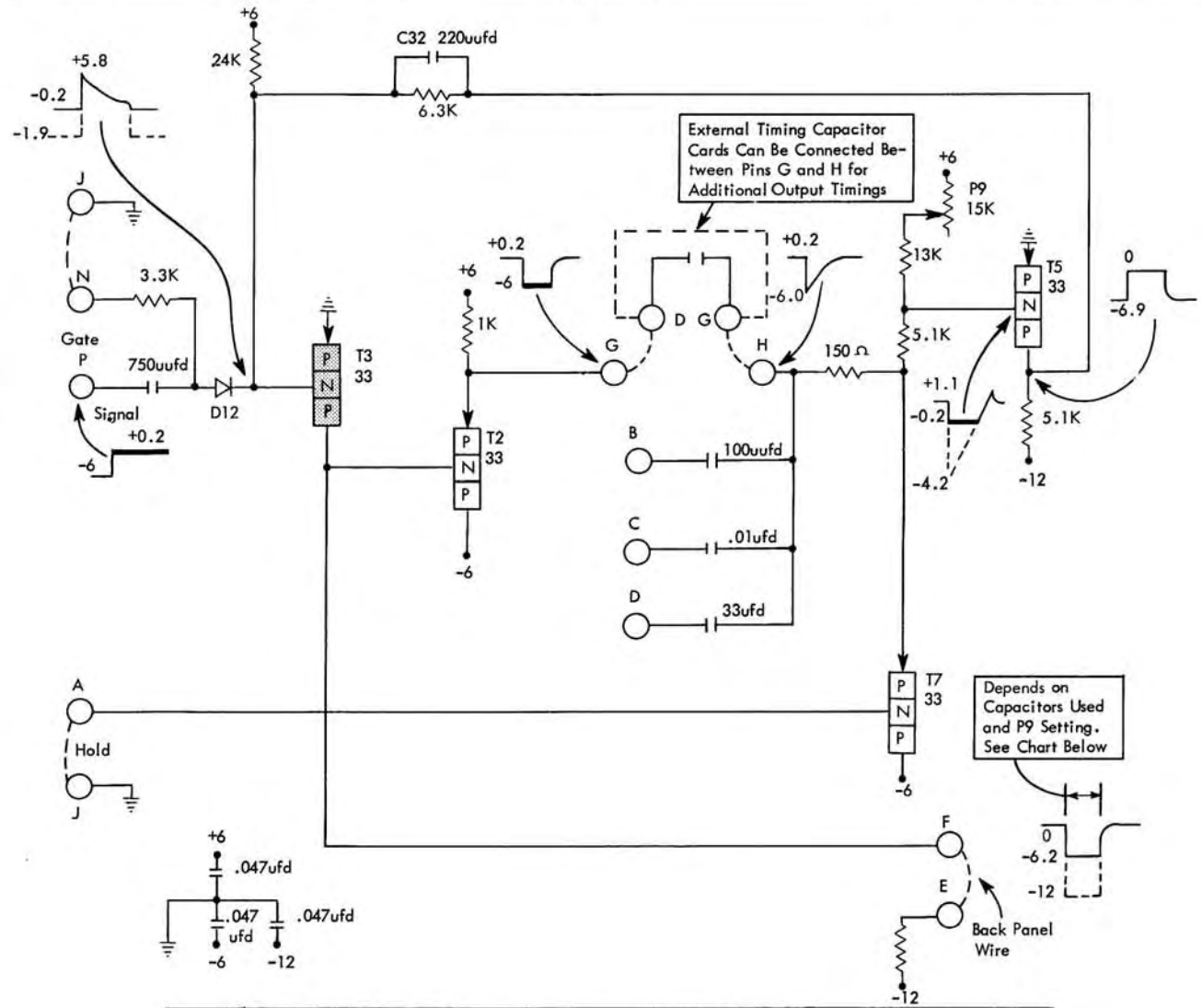
The overall circuit operation can be summarized: T4 is the oscillator transistor, with the frequency-determining resonant circuit at its collector. Feedback to T4 base from the resonant circuit is done through T1. This feedback can be cut off, or clamped, by T2. T3 detects the oscillations, which are amplified by T6 and clipped by T5. The output is approximately 6v in amplitude with a frequency of about 13μs.



ALD Configurations



Typical Application



Card Code	Part Number	Input Requirements			Output		Output Pulse Duration		
		Signal Input	Gate, Hold Inputs		Voltage Level		Connect Pin G to	(msec)	
			Min	Max	Min	Max		From	To
MR--	371623	10.8 usec Min; 5.6v Min; 1.0 usec; Max	-0.2	+0.2	-0.2	0	Pin C	.0457	.0812
			-5.56 Depends on Driving Circuit		-5.56	-6.54	Pin D	160.0	215.0
							Pin B	452.0	735.0
							Pin B and D	610.0	960.0

The MR - - card is a gated single-shot trigger circuit that produces output pulses of a fixed time duration. The circuit consists of four PNP transistors and three capacitors of different values used in the time-out network. By changing the back panel wiring to the various capacitors on the card, different output pulse durations are possible. A positive shift to a gated input starts the single-shot action and provides a negative output pulse of a fixed time duration. This output pulse duration does not depend on the input staying up. A −S level at the gate input prevents the positive shift from starting the single-shot action. Additional control of the circuit is possible with a special hold input. This input can be used to initially start or maintain the single-shot active output (−S) regardless of the other input levels. The output remains active for the selected pulse duration after the hold input is released.

A typical application of the single-shot using an external timing capacitor is shown. Both the gate and hold inputs are returned to ground.

Circuit Description

With the input gate (pin N) at +S and the input hold (pin A) at +S, the status of the circuit is: T3 fully conducting, T2 and T7 partially conducting, T5 cut off, and output pin F at the +S level. The positive shift at input pin P, through the input capacitor and the input diode, reverse biases T3. T3 cuts off and T2 base seeks −12v. Output pin F falls to a −S level and T2 reaches full conduction. The negative shift at T2 emitter, through the selected timing capacitor and 150 ohm resistor, appears on the emitter of T7. T7 cuts off. This negative voltage shift, developed across the resistor network of 150 ohm, 5.1K, 13K,and the 15K potentiometer also appears at the base of T5. T5 base seeks the −4.2v and forward-biases the transistor on.

The positive shift at T5 collector is coupled back to T3 base, maintaining T3 cut off. This action is instantaneous through the coupling bypass capacitor C32. The circuit remains in this status while the timing capacitor charges through the resistor network toward +6v. As soon as T5 base reaches ground, T5 cuts off and the coupling voltage to T3 base is lost. The input shift has long since dissipated to ground through the input gate pin N. Therefore, T3 resumes conduction and output pin F rises to its former +S level. T2 and T7 resume partial conduction and the timing capacitor discharges through T7. The circuit is back to normal.

If the hold input is used, pin A is not returned to ground. An active output level can be maintained by establishing pin A at a −S level. T7 is biased to full conduction, lowering T5 base below ground; T5 conducts, and through the coupling to T3 base, T3 is cut off; and T2 goes to full conduction. Causing T7 to conduct drives the entire circuit to the same status as an input signal does. When the hold input is released (pin A rises to +S), the timing capacitor must again charge through the resistor network toward +6v. The output at pin F will remain active until T5 is cut off by the rise in its base level, and T3 again conducts.

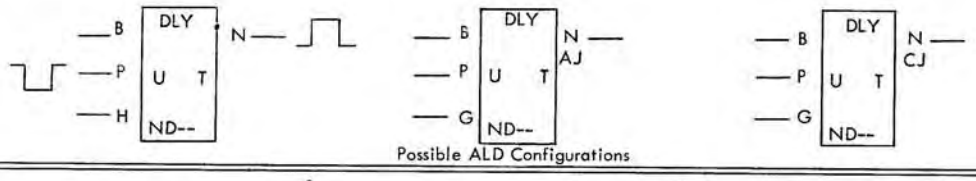
The repetition rate of this circuit is 1.3 times the selected output pulse duration,if 0.3 of the output pulse duration is used for recovery of the circuit. Turn-off delays are a function of the input rise time, and circuit loading. Delay values vary from 0.16μs to 0.8μs.

Application

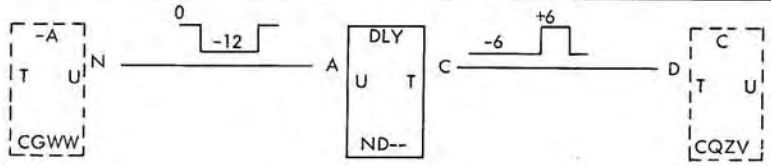
The pulse durations for the capacitor values on the single-shot card are summarized in the chart. An exact timing within the range noted is obtained by adjusting the 15K potentiometer. If additional timings are desired, external timing capacitor cards can be connected to the coupling pins. Refer to the MM - -, MN - -, and MP - - timing cards for other possible single shot timings.

Gate inputs are normally driven from CTRL logic circuits or from a voltage mode trigger. The gate input must be conditioned before the set input is applied. Levels and timings for the gated AC input operation are:

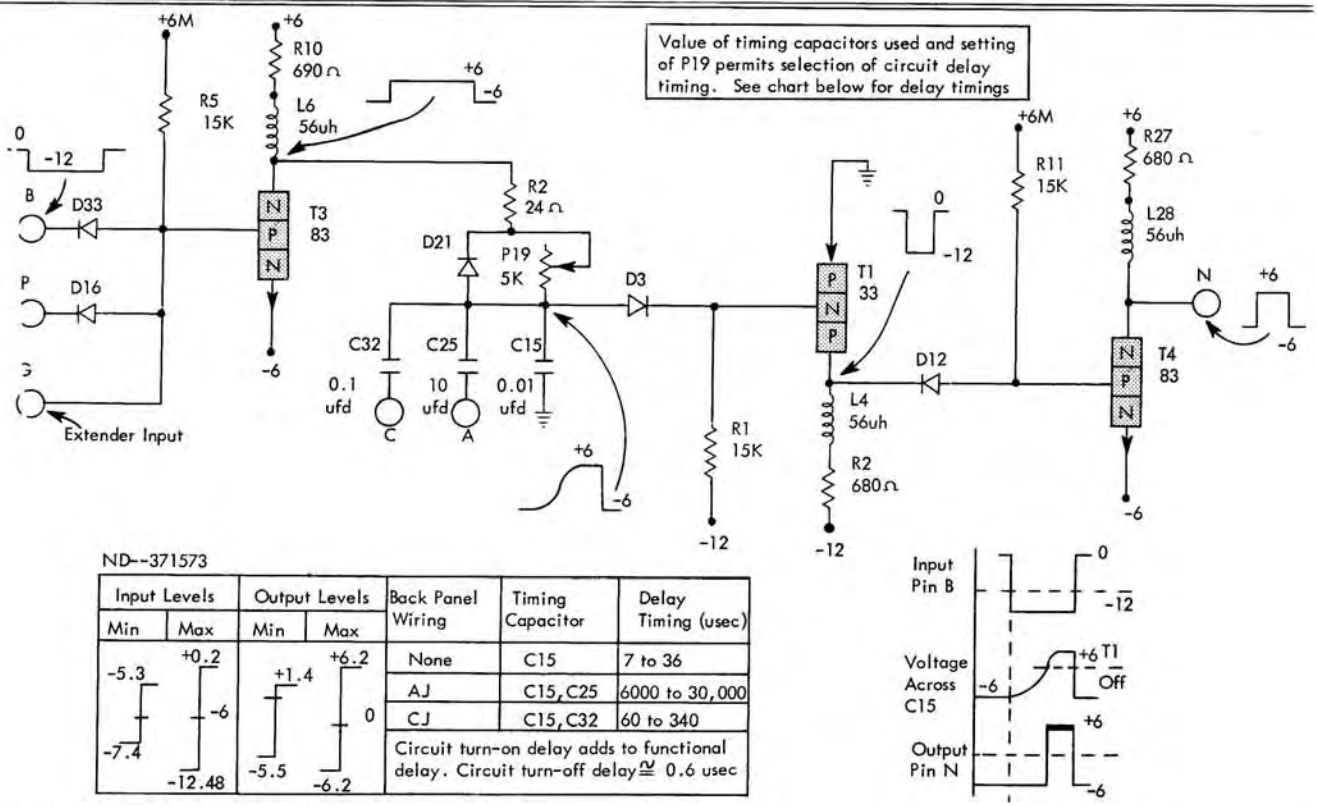
AC Set Input	Gate Level Before Conditioning	Gate Condition Time	Minimum Gate Level
6v	−12.48v	8.75μs	−0.5v
6v	−13.2v	8.90μs	−0.5v
6v	−6.24v	6.85μs	−0.5v
12v	−12.48v	5.00μs	−2.0v
12v	−13.2v	5.15μs	−2.0v



Possible ALD Configurations



Logic Application



ND--371573

Input Levels		Output Levels		Back Panel Wiring	Timing Capacitor	Delay Timing (usec)
Min	Max	Min	Max			
-5.3 to -7.4	+0.2 to -12.48	+1.4 to -5.5	+6.2 to -6.2	None	C15	7 to 36
				AJ	C15, C25	6000 to 30,000
				CJ	C15, C32	60 to 340
				Circuit turn-on delay adds to functional delay. Circuit turn-off delay ≅ 0.6 usec		

CTDL Universal Delay Circuit

The universal delay circuit provides an output pulse which begins at a definite time after the start of the input pulse. Only one delay circuit is on each card. The delay offered by the circuit is controlled by an RC network and is selected by back panel wiring to various capacitor values and by varying a 5K potentiometer.

A −U level at any of the input pins starts the delay timing and provides an out-of-phase T output. The output pulse duration is a function of the input signal duration and the circuit variables. This circuit is self-recycling, but requires a definite off period to insure the discharging of the timing capacitor(s).

Circuit Description (Circuit as Shown):

Assume all inputs in the up level; T3, T1, and T4 forward-biased and conducting. The CTDL output at pin N is near −6v and C15 is discharged to −6v through T3, R2, and the forward-biased D21.

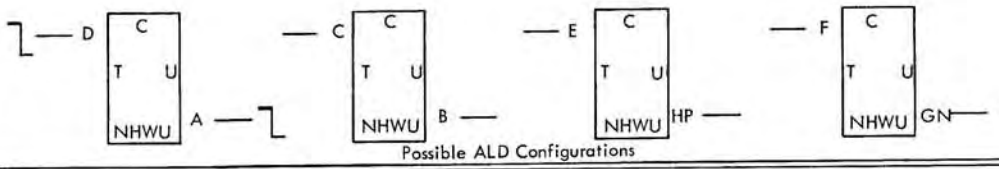
When a −U level appears at pin B (or P or G), T3 is reverse-biased off and the collector of T3 increases to +6v. D21 is no longer forward-biased, so C15 must now charge through the 5K potentiometer, R2, L6, and R10 toward the +6v collector supply.

T1 remains in conduction until the charge on C15 is positive enough to reverse-bias T1. When T1 is cut off, its collector voltage drops to −12v and cuts off T4. The collector output of T4 increases toward +6v. This +T output (pin N) remains up until all inputs again are at the +U level. The RC charging time controls the cut off of T1 and delays the start of the positive output swing for the desired time interval.

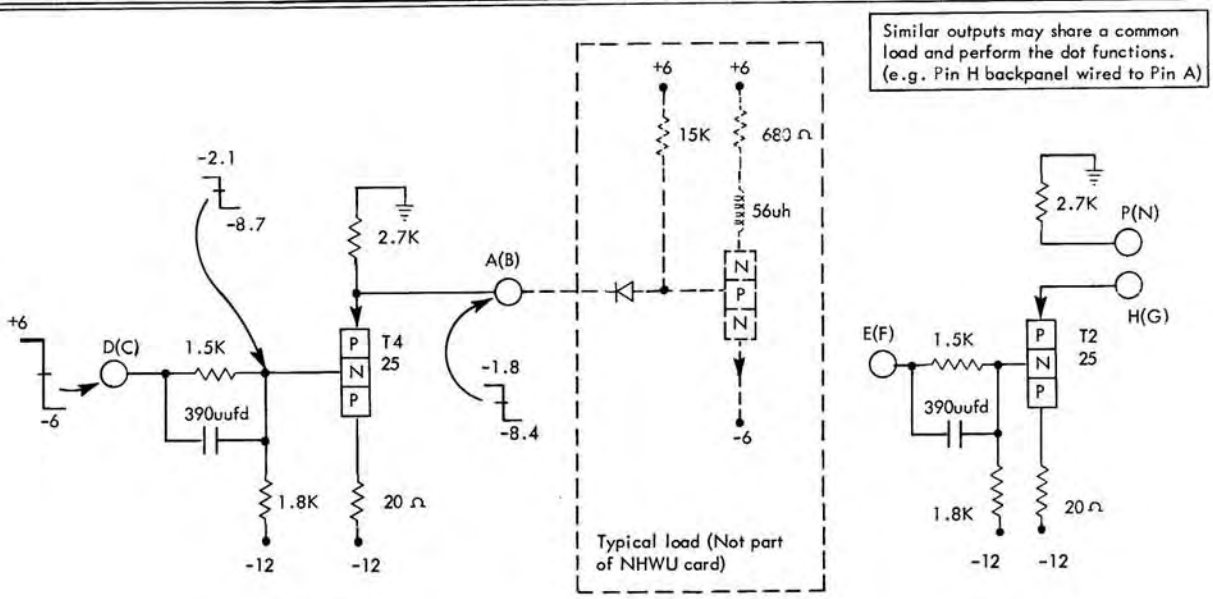
Repetition Rate: The input must remain in the up level long enough to insure that the timing capacitor is fully discharged.

Application

The range of delay timings available for the various capacitor values used is noted in the chart. Specific timings within each range can be obtained by adjusting the 5K potentiometer. Loading considerations are similar to the standard CTDL logic block.



Possible ALD Configurations



Circuits 1 and 2

Circuits 3 and 4

NHWU 371629

Input Levels		Output Levels		Delays * (usec)				Circuit Use
Min	Max	Min	Max		Load	1 CTDL Block	10 CTDL Blocks	
+1.44 / -5.46	+6.24 / -6.24	-5.2 / -7.4	-0.8 / -9.2	Turn On	Min	0.17	0.20	C
					Max.	0.52	0.53	+CA
				Turn Off	Min	0.14	0.25	-TC
					Max	0.26	0.56	-TCO

* Function of Capactive Loading and the Number of CTDL Blocks Driven

CTDL, T to U Converter

The NHWU card consists of four one-way PNP emitter follower circuits used for current amplification. Each circuit translates a T input to a U in-phase output and provides the current amplification required to drive branching circuits. This card differs from the CPWU card in that 025 transistors are used instead of the 034 transistors. The 025 transistors have lower specifications than the 034.

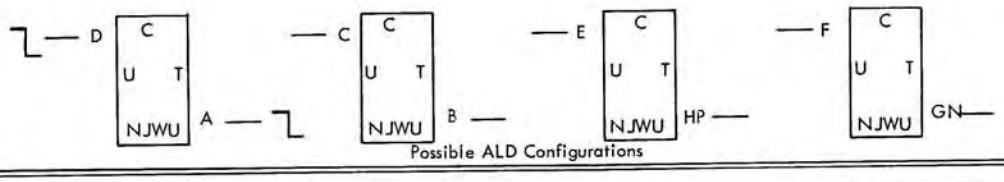
Circuit Description

The input voltage divider network sets the base voltage of T4 so that it is always in conduction. When the T input is up, the base level of T4 is at −2.1v. T4 is forward-biased on and clamps the output at pin A to −1.8v. The small drop (0.3v) exists between the base and the emitter of the conducting transistor. Decreasing the input to −6v causes the base voltage to drop to −8.7v. Conduction through T4 increases and the output at pin A becomes −8.4v. Typical circuit loading is noted above. Capacitive loading and the number of blocks driven affect the circuit delays given in the chart.

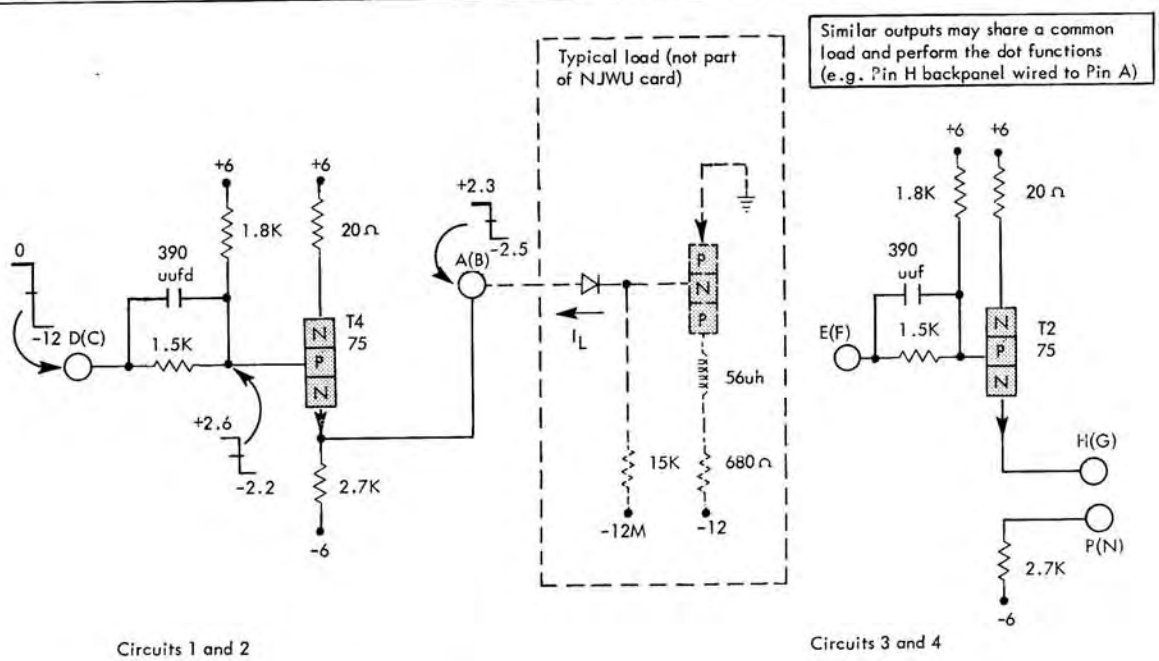
Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. These circuits normally provide current amplification to negative-going signals. They are also used as buffer devices to match impedances or to provide isolation without inversion.

Additional flexibility is provided on the card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. For example, in the circuit illustrated the CA function is performed if pin H is wired to pin A. Considering positive logic, a +T level is required at both pins D and E to obtain a +U output level and to perform the CA functions. Circuits 3 and 4 also function as standard convert circuits by back-panel wiring to their respective emitter resistors.



Possible ALD Configurations



Circuits 1 and 2

Circuits 3 and 4

NJWU 371630

Input Levels		Output Levels		Delays * (usec)				Circuit Use
Min	Max	Min	Max		Load	3 CTDL Blocks	10 CTDL Blocks	
-0.5	+0.2	+1.44	+3.1	Turn On	Min	0.21	0.25	C -CA +CO +TC +TCO
					Max	0.70	0.70	
-7.4	-12.48	-0.74	-5.1	Turn Off	Min	0.19	0.28	
					Max	0.34	0.60	

* Function of Capactive Loading and the Number of CTDL Blocks Driven

CTDL, U to T Converter

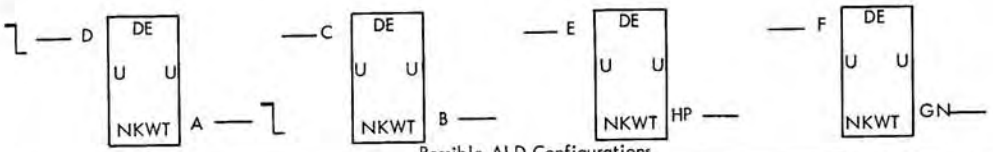
The NJWU card consists of four one-way NPN emitter follower circuits. Each circuit converts a U line input to an in-phase T line and provides the current amplification required to drive branching circuits. This card differs from the CNWU card in that 075 transistors are used instead of the 083 transistors. The 075 transistors have lower specifications than the 083.

Circuit Description

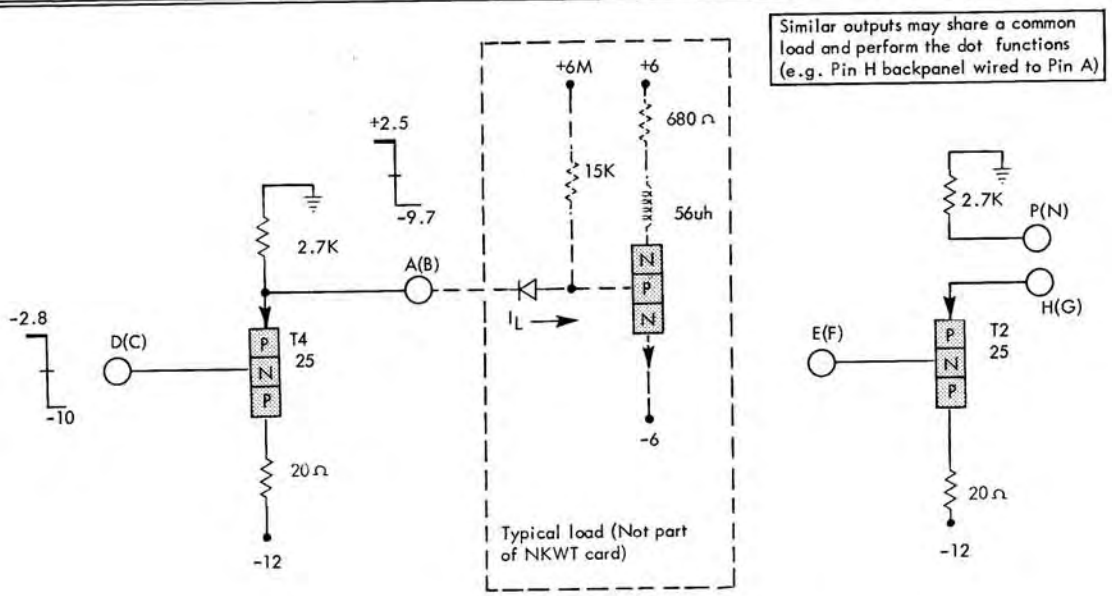
Operation is similar to the basic emitter follower. The input voltage divider network sets the base level so that T4 is always in conduction. When the input is up, the base voltage of T4 is near +2.6v. The output at pin A is set to approximately this voltage minus the base-emitter drop of 0.3v. Decreasing the U input at pin D to −12v causes the base voltage of T4 to drop to −2.2v. The conduction through T4 decreases and the output at pin A follows the input swing minus the slight base-emitter voltage drop. Typical circuit loading is noted above. Capacitive loading and the number of blocks driven affect the circuit delays noted in the chart above.

Applications

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. These circuits provide current amplification of positive-going signals, serve as buffer devices to match impedances or provide isolation without inversion. Additional flexibility is provided on this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connection for sharing a common emitter load is easily made by back-panel wiring. For example, in the circuits illustrated above, the CO function is performed if pin H is wired to pin A. Considering positive logic, a +U level at either pin D or E provides a +T output level. Circuits 3 and 4 also function as standard convert circuits by back-panel wiring to their respective emitter resistors.



Possible ALD Configurations



Circuit 1 and 2

Circuits 3 and 4

NKWT 371631

Input Level		Output Level		Delays * (usec)				Circuit Use
Min	Max	Min	Max		Load	3 CTDL Blocks	15 CTDL Blocks	
-5.46 +0.24 -7.6 -6.74 -6		-5.2 +0.2 -7.4 -12.48 -6 -6		Turn On	Min	0.18	0.27	DE
					Max	0.48	0.62	-DEO
				Turn Off	Min	0.08	0.12	+DEA
					Max	0.17	0.33	

* Function of Capactive Loading and the Number of CTDL Blocks Driven

CTDL Emitter Follower PNP

The NKWT card consists of four one-way PNP emitter follower circuits that provide sufficient current to drive into branching circuits. Each circuit serves as a non-translating current amplifier, accepting a U input from CTDL logic blocks and providing an in-phase U output. A slight DC shift occurs between the input and output voltage levels. This card differs from the CPWT card in that 025 transistors are used instead of the 034 transistors. The 025 transistors have lower specifications than the 034.

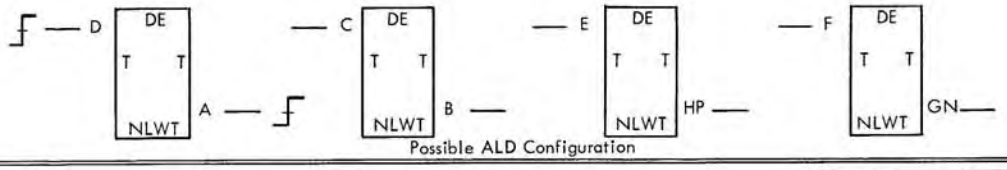
Circuit Description

A +U line input allows a minimum of current to flow through the emitter follower T4. The output at pin A clamps to this input value (minus the base-emitter drop of 0.3v). When the input drops to −10v, T4 is forward-biased more and conduction through T4 increases. The voltage at pin A follows the voltage swing at the base of T4 (minus the base-emitter drop). Typical loading is shown for the emitter follower. Capacitive loading and the number of blocks driven affect the circuit delays noted above.

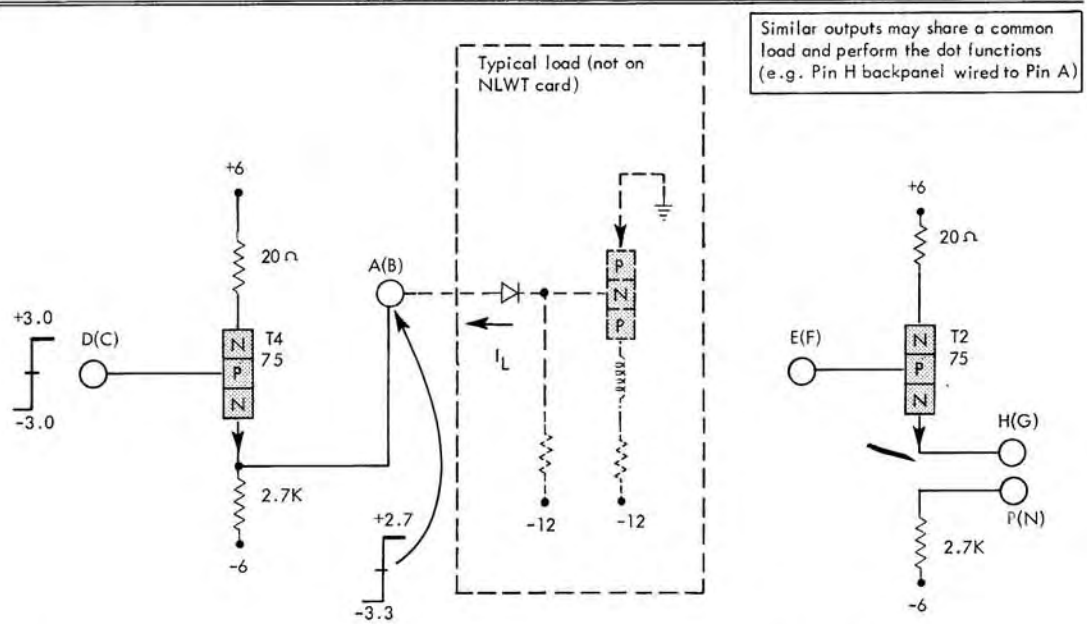
Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The PNP emitter follower circuit is normally used for current amplification of negative going U lines and to furnish additional drive to P type branching circuits. These circuits are also used for impedance matching or for isolation without inversion.

Additional flexibility is provided on this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. For example, in the circuit illustrated above, the DEA function is performed if pin H is wired to Pin A. Considering positive logic, a +U input is required at both pins D and E to obtain a +U output at pin A and satisfy the DEA function. Circuits 3 and 4 also function as standard emitter followers by back-panel wiring to their respective emitter resistors.



Possible ALD Configuration



Circuits 1 and 2

Circuits 3 and 4

NLWT--371632

Input Levels		Output Level		Delays * (usec)				Circuit Use
Min	Max	Min	Max		Load	3 CDTL Blocks	15 CTDL Blocks	
+1.8 to -0.7	+6.24 to -6.24	+1.44 to -0.7	+6.24 to -6.24	Turn On	Min	0.23	0.32	DE
					Max	0.68	0.68	-DEA
				Turn Off	Min	0.05	0.09	+DEO
					Max	0.13	0.25	

* Function of capacitive loading and number of CTDL blocks driven.

CTDL Emitter Follower NPN

The NLWT card consists of 4 one-way NPN emitter follower circuits that provide sufficient current to drive into branching circuits. Each circuit serves as a non-translating current amplifier that accepts a T input from a CTDL logic block and provides an in-phase T output. A slight DC shift occurs between the input and output voltage levels. This card differs from the CNWT card in that 075 transistors are used instead of the 083 transistors. The 075 transistors have lower specifications than the 083.

Circuit Description

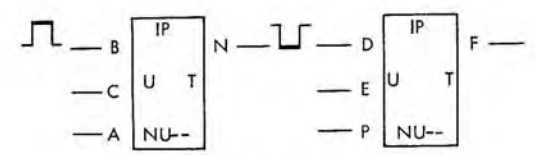
A-T level input allows a minimum of current to flow through the emitter follower T4. The output at pin A clamps to this input value (minus the base-emitter voltage drop of approximately 0.3v). When the input increases to +3v, conduction through T4 increases and the output at pin A clamps to the input voltage. Typical loading is noted above for the emitter follower. Capacitive loading and the number of blocks driven affect the circuit delays.

Application

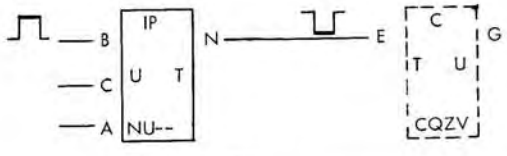
The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use.

These circuits are normally used for power amplification of positive-going T lines, for impedance matching, or for isolation without inversion of a signal.

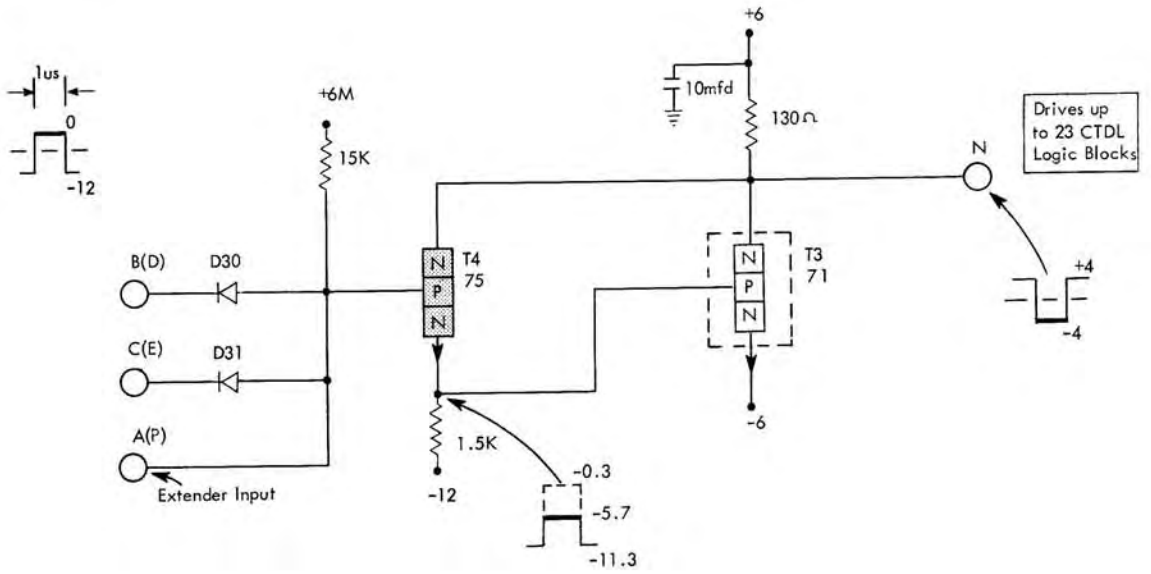
Additional flexibility is provided by this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. For example, in the circuits illustrated above, the DEO function is performed if pin H is wired to pin A. Considering positive logic, a +T input at either pin D or pin E will give a +T output at pin A, and satisfy the DEO function. Circuits 3 and 4 can also function as standard emitter followers by back-panel wiring to their respective emitter resistors.



Possible ALD Configurations



Logic Application



Input Levels		Output Levels		Delays (usec)			Output Current	
Min	Max	Min	Max					
-4.65 to -7.44	+2.4 to -12.48	+1.44 to -5.46	+6.24 to -6.24	Turn On	Min	0.09	Up Level	Down Level
					Max	0.38		
				Turn Off	Min	0.11	23.5 ma	4.5 ma
					Max	0.13		

CTDL Power Inverter

The NU--card consists of two power inverter circuits capable of driving 23 CTDL logic blocks. Each circuit is basically a modified emitter follower driving an inverter. A relatively small input signal develops a large power output for driving into the CTDL loads. The input circuit is similar to the CTDL logic block and has two diode inputs and an extender input. A +U line of at least 1μs duration at all inputs is required to drive T4 into maximum conduction and provide a −T output from T3.

Circuit Description

When any of the inputs at pins A, B, or C are down (−U level), minimum current flows through the 1.5K resistor and the emitter follower T4. The emitter follower output holds T3 off and only the small current flow from T4 flows through the 130 ohm resistor. A +T output exists at pin N.

Coincidence of +U levels at all the input pins causes T4 to become more forward-biased. Increased current flow through the 1.5K emitter resistor, T4, and the 130 ohm resistor to +6v causes the base of T3 to rise above −6v. T3 becomes forward-biased on. When T3 turns on, additional current through the 130 ohm resistor quickly drops the output at pin N to a −T level. At this time up to 30ma is supplied.

The 130 ohm resistor relates the two collectors so that if T3 tends to become saturated, the current through T4 is decreased, which in turn reduces the base current to T3. This degenerative action prevents T3 from operating in saturation and provides medium current outputs with minimum turn-on and turn-off delays.

Application

Typical loading is shown in the circuit.

Glossary

ACCESS TIME. The time required to call a number from storage and make it available to the arithmetic section.

ALTERNATION. Half of a complete cycle.

AMPLIFIER, CLASS A. An amplifier in which the swing of the input signal is always on the linear portion of the characteristic curves of the amplifying device.

ANODE. A positive electrode (the receiver of electrons).

ASTABLE MULTIVIBRATOR. A multivibrator that can function in either of two semistable states, switching rapidly from one to the other (referred to as free running).

BINARY COUPLED TRIGGER. A trigger with a common input so arranged that two successive negative pulses will turn the trigger on, then off.

BINARY NUMBER SYSTEM. A number system using the base two. There are only two symbols; one or zero (ON or OFF).

BIT. The name for a binary digit (one or zero). It may be represented by magnetized spots on tape or drum, magnetized cores, or a particular state of an electron tube.

CARRIER. A conveyor of charges through a semiconductor. In transistors, two types of carriers of charges are present: holes and electrons.

CHARACTER. A decimal digit 0 to 9, a letter A to Z, or a special symbol.

CHARACTERISTIC IMPEDANCE (Z_0). The ratio of the voltage to the current at every point along a transmission line on which there are no standing waves.

CLAMPING CIRCUIT. A circuit that maintains either or both amplitude extremities of a waveform at a certain level or potential.

CLOCK. A source of timed pulses used to sequence events in the machine (similar to a timing index on card machines).

CLOSED RING. A ring of triggers in which the last trigger feeds the first trigger to allow the ring to operate continuously.

COMMON-BASE (CB) AMPLIFIER. A transistor amplifier in which the base element is common to the input and the output circuit. This configuration is comparable to the grounded-grid triode electron tube circuit.

COMMON-COLLECTOR (CC) AMPLIFIER. A transistor amplifier in which the collector element is common to the input and the output circuit. This configuration is comparable to the electron tube cathode follower circuit.

COMMON-EMITTER (CE) AMPLIFIER. A transistor amplifier in which the emitter element is common to the input and the output circuit. This configuration is comparable to the conventional electron tube amplifier circuit.

COMPLEMENTARY SYMMETRY CIRCUIT. An arrangement of PNP-type and NPN-type transistors that provides push-pull operation from one input signal.

CONFIGURATION. The relative arrangement of parts (or components) in a circuit.

COUPLING. The association of two circuits in such a way that energy may be transferred from one to the other.

CROSSTALK. Distortion introduced from one circuit to another circuit.

CUTOFF FREQUENCY. The frequency at which the gain of an amplifier falls below .707 times the maximum gain.

CYCLE. One complete positive and one complete negative alternation of a current or voltage.

DAMPED WAVES. Waves which exponentially decrease in amplitude.

DIFFERENTIATING CIRCUIT. A circuit that produces an output voltage proportional to the rate of change of the input voltage.

DISTORTION. The production of an output waveform which is not a true reproduction of the input waveform. Distortion may consist of irregularities in amplitude, frequency, or phase.

DOT FUNCTIONS. Under certain conditions, outputs of similar levels are tied together and share a common load. This condition provides a second level of logic in some circuits within one block of delay.

DRUM. A constantly rotating cylinder with a magnetic surface on which data is stored by magnetizing spots on this surface.

ERASE. To destroy the information stored on the surface of a magnetic tape, magnetic drum, or cathode ray tube to make this storage space available for new information.

FALL TIME. The time when the amplitude of a pulse decreases from 90 percent to 10 percent of its maximum value.

FORWARD BIAS. In a transistor, an external potential applied to a PN junction so that the depletion region is narrowed and relatively high current flows through the junction.

GATING CIRCUIT. A circuit operating as a switch, making use of a short or open circuit to apply or eliminate a signal.

HARMONIC. An integral multiple of a fundamental frequency. (The second harmonic is twice the frequency of the fundamental or first harmonic.)

HEAD. A writing and sensing device containing coils around a laminated core of high permeability material.

HOLE. A mobile deficiency, in the atomic structure of a semiconductor material, that acts as a positive charge.

IMPEDANCE (Z). The total opposition offered to the flow of an alternating current. It may consist of any combination of resistance, inductive reactance, and capacitive reactance.

IMPULSE. Any force acting over a comparatively short period of time, such as a momentary rise in voltage.

IN PHASE. The condition that exists when two waves of the same frequency pass through their maximum and minimum values of like polarity at the same instant.

INPUT-OUTPUT. Unit(s) responsible for sending information into a computer and for receiving processed information from a computer.

INSTANTANEOUS VALUE. The magnitude, at any particular instant, of a value that is continually varying with respect to time.

INTEGRATOR CIRCUIT. One which sums up and produces an output voltage substantially in proportion to the frequency and amplitude of the input pulse.

KILO (K). A prefix meaning 1,000.

KILOCYCLE (KC). One thousand cycles; conversationally used to indicate 1,000 cycles per second.

LATCH. A flip-flop device composed of two or more circuits. The output of a latch is looped or latched back to the input to hold the device in one of its two possible states. The latch is turned off by breaking this closed feedback loop at any point.

LOAD. The impedance to which energy is being supplied.

LOGIC. The process of determining, by deductive reasoning, the means for obtaining a desired result from a given set of conditions.

MAJORITY CARRIERS. The holes or free electrons in P-type or N-type semiconductors respectively.

MINORITY CARRIERS. The holes or excess electrons found in the N-type or P-type semiconductors respectively.

MEMORY. A term used to denote any internal storage devices of a machine.

OSCILLATOR. A circuit capable of converting direct current into alternating current of a frequency determined by the constants of the circuit.

PARALLEL OPERATION. A machine operation where all the bits or characters of a word are handled at the same time.

PERMEABILITY. The property of a magnetic material that indicates its relative ability to accept magnetism.
Permeability = Flux Density ÷ Ampere-Turns (MU = B/H).

POTENTIOMETER. A variable voltage divider; a resistor having a variable contact arm so that any portion of the potential applied between its ends may be selected.

PULSE. A change, relatively short in time, in voltage applied to a circuit.

PULSE REPETITION FREQUENCY. The number of nonsinusoidal cycles (square waves) that occur in 1 second.

PUNCH THROUGH. The condition where a transistor has exceeded its limit of control and acts as a low resistance device. Punch through results when the reverse-bias supply completely ionizes the base region.

PYRAMIDING FACTOR. The maximum loading (number of transistor bases) that can be driven by a particular circuit.

QUIESCENCE. The operating condition of a circuit when no input signal is applied to the circuit.

READ. To take information or data out of a storage medium.

REGENERATE. To read information out of a storage unit and, after amplification, to read it back into the same storage location.

RESONANCE. The natural frequency of vibration of a physical or electrical system.

REVERSE-BIAS. An external potential applied to a PN junction such as to widen the depletion region and prevent the movement of majority current carriers.

RISE TIME. The time when the leading edge of a pulse increases from 10 percent to 90 percent of its maximum value.

SATURATION. The condition occurring when a transistor is driven so hard that its base becomes forward-biased in respect to its collector.

SATURATION (LEAKAGE) CURRENT (I_{CO}). The current flow between the base-collector or between the emitter and collector measured with the emitter lead or the base lead, respectively, open.

SEMICONDUCTOR. A conductor, whose resistivity is between that of metals and insulators, in which electrical charge carrier concentration increases with increasing temperature over a specific temperature range.

SERIAL OPERATION. A type of machine operation where information is handled one digit or character at a time.

SHIELDING. A metallic covering used to prevent magnetic or electrostatic coupling between adjacent circuits.

SKEW. A term used to indicate a non-symmetrical condition of two waveforms that results in a changed time relationship. One waveform may be developed more on one side or in one direction than the other.

STABILITY. Freedom from undesired variation.

STABISTOR. A semiconductor diode having a constant forward-voltage drop over a wide range of forward current.

STORAGE. A general term given equipment having the ability to hold and store information.

STORAGE TIME. The time during which the output current or voltage of a pulse is falling from maximum to zero after the input current or voltage is removed.

STORED BASE CHARGE. The phenomenon associated with the storage of minority charge carriers in the base region under conditions of saturation.

STRAY CAPACITANCE. The capacitance introduced into a circuit by the leads and wires that connect circuit components.

SWITCH. Diode or transistor circuitry that requires coincidence of two or more signals to produce an output signal.

THERMISTOR. A type of varistor that changes electrical resistance with changes in temperature. Thermistors provide a constant AC voltage drop for reference purposes.

TRANSISTOR. A semiconductor device capable of transferring a signal from one circuit to another and producing amplification.

TRIGGER CIRCUIT. A circuit requiring an input signal (trigger) to produce a desired output that is determined by the characteristics of the circuit (also known as a flip-flop or bi-stable multivibrator circuit).

TURN-ON DELAY. The finite time delay between the start of the input and the start of the output signals when the transistor is forward biased on. The delay results from the difference in velocities and path lengths taken by the carriers when passing through the transistor.

TURN-OFF DELAY. The finite time delay between the end of the input and the end of the output signals when the transistor is reversed-biased off. The delay results from differences in the path length, velocity, and the base storage of the carriers in passing through the transistor.

VALIDITY CHECK. A check of information within the machine to insure valid digit representation.

VARISTOR. A component whose resistance varies with the applied voltage.

VOLTAGE DIVIDER. An impedance connected across a voltage source. The load is connected across a fraction of this impedance so that the load voltage is substantially in proportion to the resistance of this fraction.

VOLTAGE GAIN. The ratio of incremental values of output voltage to input voltage of an amplifier under load conditions.

WRITE. The process of placing information or data in a storage medium.

ZENER DIODE. A PN junction diode reverse-biased into the breakdown region (used for voltage stabilization).